9400/9400A
DIGITAL OSCILLOSCOPE

SERVICE MANUAL

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SERVICE MANUAL for the LeCROY 9400 DSO

INTRODUCTION

The present Service Manual applies to both the 9400 and the 9400A DSOs. Both models are called 9400 when the information applies equally to both oscilloscopes. Where the two models have distinct features, the model number 9400 or 9400A is explicitly stated.

The chief purpose of this manual is to provide information for technicians, mainly authorized LeCroy repair office personnel, who are responsible for repairs and modifications to the LeCroy 9400/9400A DSOs.

To this end, the descriptions provided are intended to be of sufficient depth to enable faults to be diagnosed to the level of the relevant board, so that the customer can be quickly supported by exchange of boards. In many cases the fault may be corrected at the local LeCroy office, but there are several areas of the circuitry where replacement of a part would need to be followed by calibration which could be done only with specialized equipment available at the main LeCroy establishments. Calibration procedures are given in this manual only for those areas which could be serviced locally.

A DSO repair intervention at board exchange level can only be done by qualified technicians who have followed the basic 9400/9400A service training. LeCroy also offers these courses to customers. In addition, there is a very comprehensive 9400 Adjustment and Calibration Software Package CALSOFT (order codes CS01/CS02) based on the IBM PC or a compatible computer. This software package is also available to customers, as well as all the hardware making up the 9400 Automated Calibration System (order code CS-S) which is used in all LeCroy service offices to ensure full performance of the instrument. This system provides Calibration Certificates traceable to NBS. LeCroy also offers training classes on DSO calibration.

This manual could be improved by the inclusion of useful information resulting from detection and correction of faults in 9400/9400A DSOs at any LeCroy office. Each time a DSO is opened, an official LeCroy repair report should be sent to LeCroy S.A., attention Customer Service. The information is entered into a centrally maintained DSO data base for failure analysis and engineering feedback.

Before undertaking any work on the 9400 DSO you should read the next sections - WARNINGS and VALID RANGE of FIELD MAINTENANCE.

WARNING

Please read all of this section and the next section, (Valid Range of Field Maintenance), before attempting any work on the 9400.

The LeCroy 9400 oscilloscope uses a cathode ray tube which operates with a stabilized high voltage supply, capable of delivering a very unpleasant electric shock, the reaction to which could be damaging to the recipient, or to anything struck by his involuntary movements. Although no danger should result from the handling of this equipment by an experienced person taking the normal precautions, LeCroy recommends that inexperienced personnel avoid working inside this equipment.

Care is necessary when working inside equipment which contains a CRT, because of the relative weakness of the stem.

The line power switch is at the lower right corner of the front panel, and in some DSOs, when the bottom cover is off, the live wire is exposed.

The 9400 contains numerous preset controls which are set in optimal positions in the factory, using specially designed test gear. Very few of these trimmers can be set correctly without these facilities; therefore care is needed in handling boards which carry such parts. Trimmers should be adjusted only as shown in this manual, or as otherwise authorized by LeCroy SA or its agents.

Do not operate the 9400 with the top cover off for a longer time than is necessary for the work in hand, because the normal circulation of cooling air will not be obtained.

Do not use any Freon or Freon-based liquid to clean parts while they are in the 9400, because Freon can damage the screen printing of the front and rear panels, and can cause electrical problems if there is penetration into potentiometers on the front panel.

The LeCroy 9400 is of sound construction, but contains parts which may be damaged by incorrect handling, including effects due to static electricity, high voltages and mechanical mishandling. The oscilloscope should not be opened by unqualified personnel. Repairs and modifications should be attempted only by authorized LeCroy personnel.

Any unauthorized work by a customer or his agent on the 9400 may invalidate any warranty, extended warranty, service contract or other contract entered into with LeCroy, who reserve the right to charge for any work which is needed as a consequence of such action.

Note that many of the diagrams of waveforms in this manual were prepared using a 9400, because this was the most convenient method. It will be appreciated that the risetimes of logic waveforms will be increased, but this should not impair the value of the data. Be careful to inspect the diagrams to see whether a X10 probe was used.

VALID RANGE of FIELD MAINTENANCE

Because the LeCroy 9400 contains electronic circuits which are exactly set up to achieve the excellent performance specifications of this equipment, there is need for circumspection in maintenance.

Generally, it should be assumed that any adjustment which is not specifically referred to in this manual is one which can be performed correctly only with specialized test equipment which is not available at small LeCroy offices.

In particular the following operations should not be attempted without authorization:

- Adjustment of the ADC circuits on the 9400-3 boards (1.3.2-6)
- Replacement of any parts in those areas of the 9400-3 boards

The following areas are critical also, but can be adjusted or repaired provided that the equipment listed in (2) is available for calibration and tuning:

- Front-end circuits (1.1.31) trigger circuits (1.1.33) and TDC trigger circuit (1.4.8).

An attempt has been made to simplify the problem of relating different parts of the instrument, by providing some cross-references. The use of these without some guidance may be rather frustrating if all are used without distinction, and a good way to filter them is to know the chapter headings on the first page of the contents. The contents pages of all the chapters are grouped together at the start of the manual, as well as being placed in their chapters, for the same purpose.

The section numbers do not run consecutively. This allows them to be correlated with board numbers and allows new sections to be inserted as required.

SERVICE MANUAL for the LeCROY 9400 DSO

Table of Contents

Note: Throughout this manual the following notation will be used:

- (5.6.7) Refer to Section 5.6.7
- <2.1.4> Refer to Figure 2.1.4
- <3.1.5.B> Refer to the item labeled B in <3.1.5>

Note: The schematics used in this manual correspond to one particular ECO for each board; before doing any repairs or modifications look at the schematic for the relevant ECO.

Note: Section numbers correspond to board numbers:

- m.n 9400-n
- m.9 9400-9 and power supplies
- m.11 9401-1
- m.12 9401-2

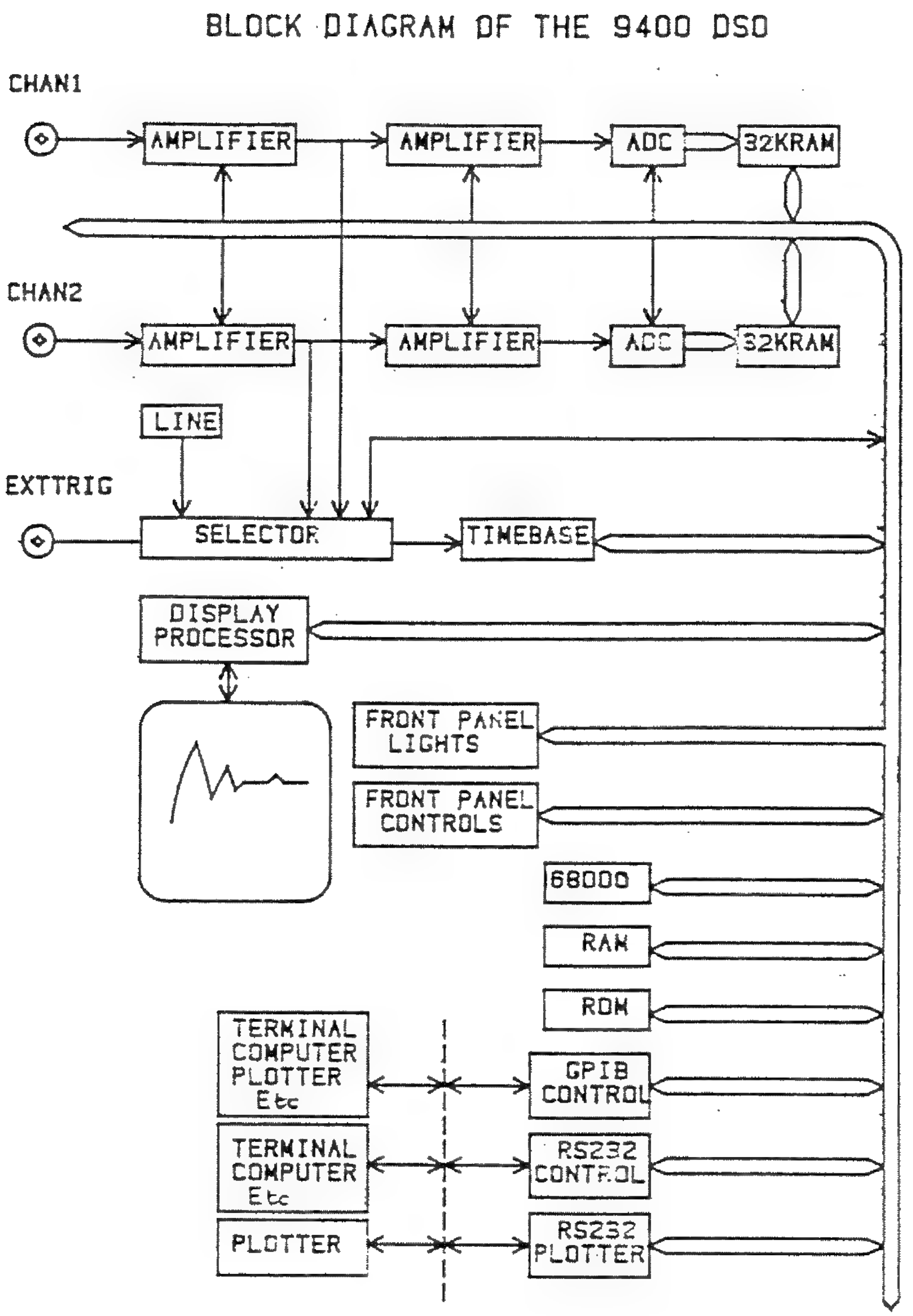
Index of Subjects | Section of Manual

CHAPTER 1

FUNCTIONAL DESCRIPTION

Table of Contents

Each section is further subdivided into functional units using the point notation.



BLOCK DIAGRAM OF THE 9400 DSO

Figure 1.0.1

1.0 Functional Description - Overview

1.0.1 Main Functions of the 9400 DSO

The main functions of the 9400 are <1.0.1>:

- Input 2 channels of analog information
- Input 1 channel of trigger information
- Convert analog information to digital data
- Store digital data in 32K memories
- Present stored information on viewing screen
- Present stored information at RS-232-C ports
- Present stored information at GPIB port
- Accept control information at RS-232-C port
- Accept control information at GPIB port

Note that the functional blocks in <1.0.1> do not correspond to the circuit boards of the 9400. The blocks are located on the boards as follows:

- Attenuate and Amplify	9400-1
- Sample and Hold	9400-3
- ADC	9400-3
- 32K Memory	9400-3
- Trigger Select	9400-1
- Time base	9400-4
- Display Processing	9400-2
- 64K Storage Memory	9400-1
- Plotter Control	9400-1
- RS-232-C Control	9400-1
- GPIB Control	9400-6 or 9401-2

The boards in numerical order are:

- Main Board	9400-1		
- Display Control Board	9400-2		
- ADC Boards	9400-3		
- TDC Board	9400-4		
- Front-panel Board	9400-5A	9400-5B	
- GPIB Control Board	9401-2		
- CRT Board	9400-7		
- Clock Bus Board	9400-8		
- Power Supply Board	9400-9A	9400-9B	9400-9D
- GPIB+extra DRAM	9401-2/1		

Note that 9400-6 and 9401-2 are alternative occupants of the same slot, depending on the date on which the DSO was made. Earlier DSOs have the 9400-6 board; later ones have versions of the 9401-2 board.

1.0.2 Introduction to the Functional Description

The functional description is given at a level which is intended for those who need to repair or modify a 9400 DSO. Internal details of LeCroy hybrids are not consistently given; nor are details of software and other details which do not in any way assist in maintenance. Wherever possible, this chapter is sectioned in a way which corresponds closely with functional areas of the 9400 DSO. Since it is not possible to understand the function of any part of the 9400 DSO in isolation, every section of the description is provided with references to other sections of the manual which describe parts which directly interact with the part being described.

Note that in order to create context for some of the pieces of schematic, it has been necessary to join pieces of schematic which are on different sheets. Each schematic in the functional description bears a legend giving the origin in the main schematic (8), and the ECO for which it is relevant. Before undertaking any repair or modification make sure to examine the relevant area of the schematic pertaining to the ECO level of the actual unit on which work is being done, because it is not practicable to update this manual for each ECO.

1.0.3 Overview

The seat of control is the 68000 CPU, on the 9400-1. The hardware peripherals are memory mapped, and are selected by a decoder (1.1.6). Some peripherals generate interrupts (1.1.7) to the 68000, while others use control lines with handshake.

The main function of the 9400 DSO, namely the acquisition of waveforms, is executed by the 9400-3 ADC boards, under the control of the 9400-4 TDC board during acquisitions, and the 9400-1 for reading out the ADC memories. The 9400-4 includes the main sampling clock and a number of derived clocks which control the timing of the sampling and storage into the ADC memories, in the various available modes, such as pre- and post-trigger, roll and normal modes. The control information for the 9400-4 is generated by the software on the 9400-1, in response to information generated by the user at the front panel or one of the interfaces.

The 9400-1 also controls main functions such as controlling the display, which is generated by the 9400-2 board, and acquiring data from, and sending data to, the front panel, via the 9400-5 board.

The frontend analog parts of the 9400 DSO are all situated at the front right corner of the 9400-1, behind the input sockets. This section includes the frontend amplifier hybrids, and all the input selection circuits, gain and attenuation controls, etc.

1.1 9400-1 Main Board Table of Contents

Logic Section

Analog Section

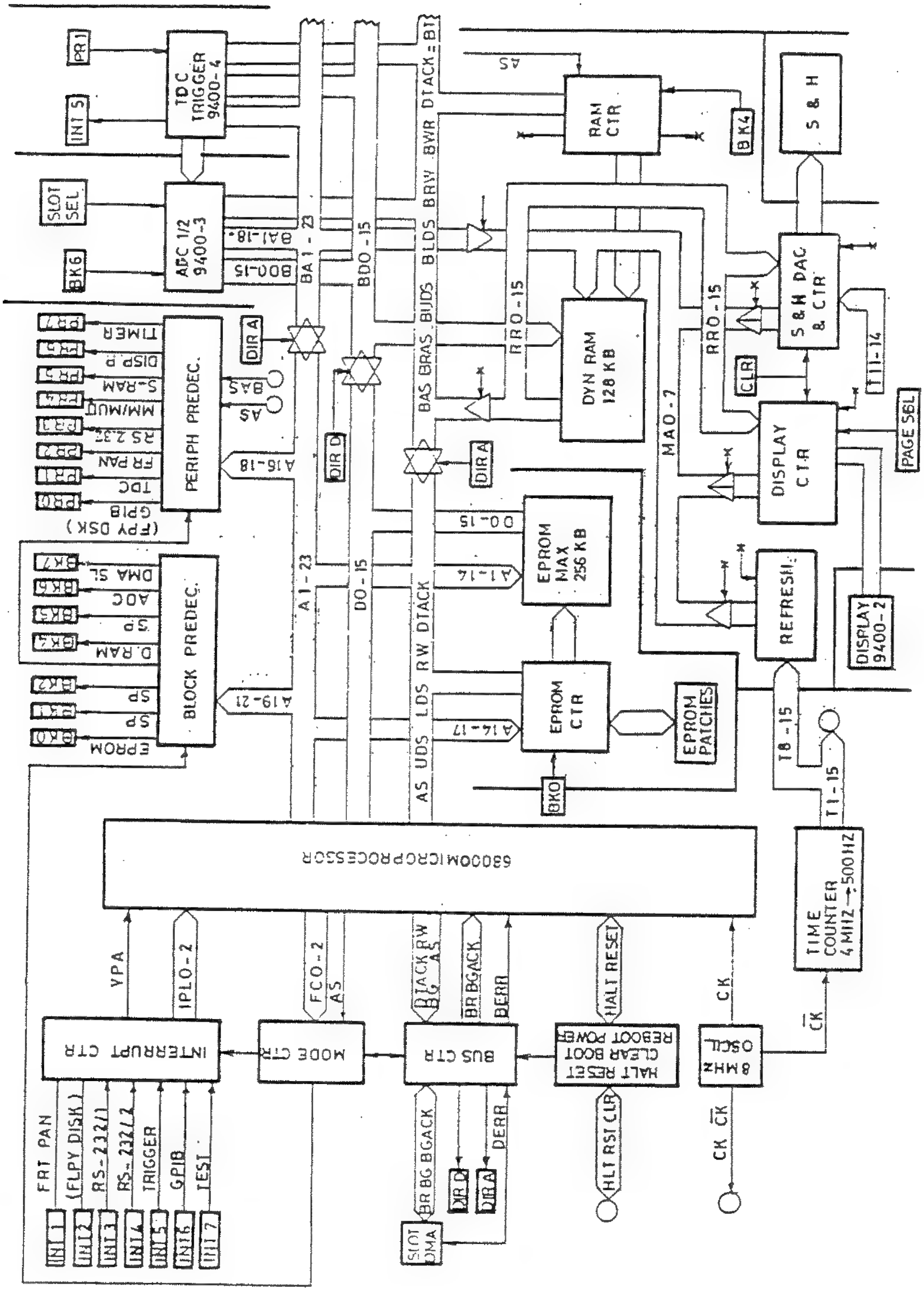
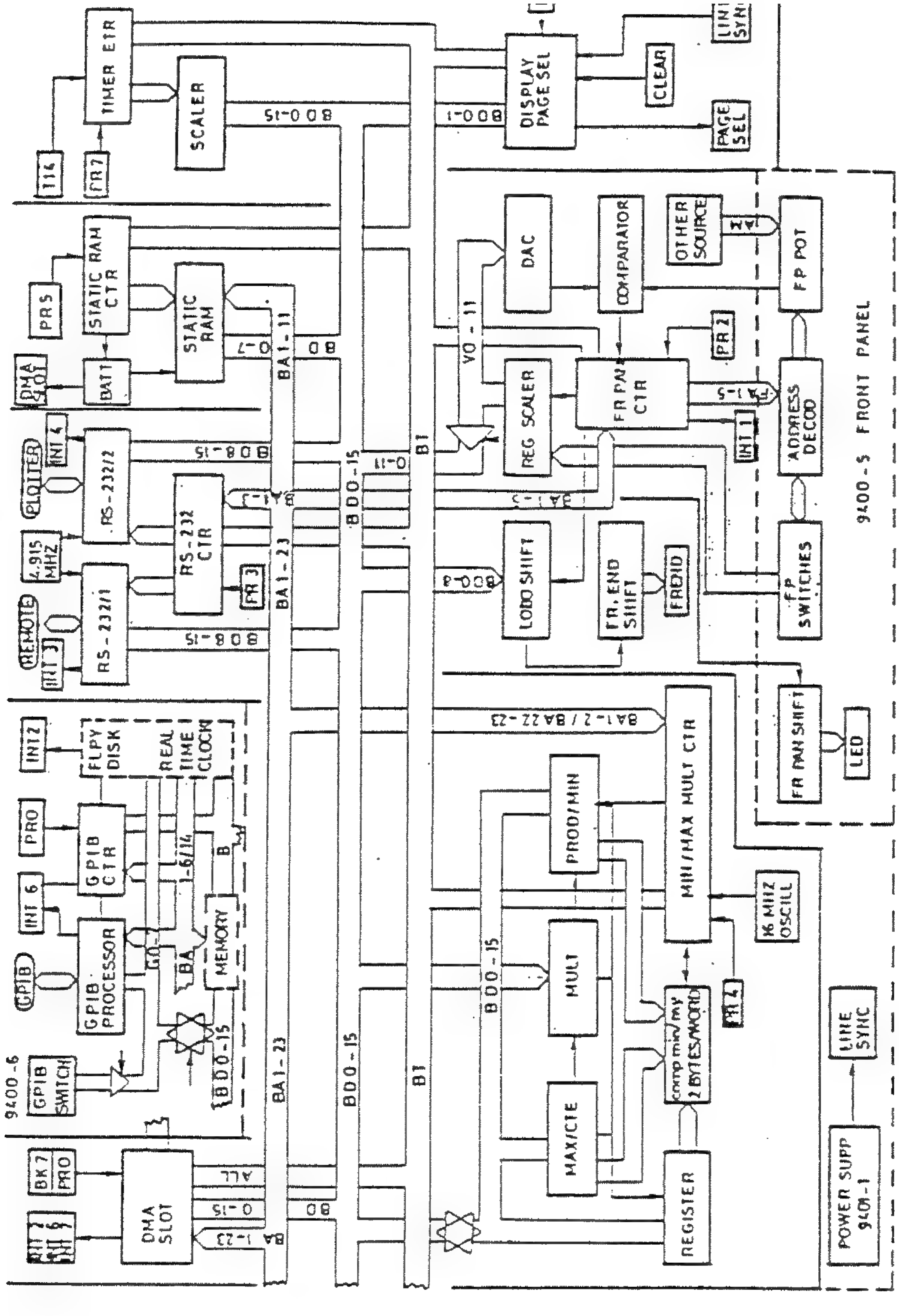

TDC TRIGGER 9400-4
ADC 1/2 9400-3
PERIPH PREDEC.
BLOCK PREDEC.
RAM CTR
DYN RAM 128 KB
EPROM MAX 256 KB
EPROM CTR
EPROM PATCHES
S & H
S & H DAC & CTR
DISPLAY CTR
REFRESH
DISPLAY 9400-2
TIME COUNTER
INTERRUPT CTR
MODE CTR
BUS CTR
HALT RESET CLEAR BOOT REBOOT POWER
8 MHz OSCIL

Figure 1.1.1.1



BLOCK DIAGRAM OF 9400-1 BOARD

Figure 1.1.1.1

1.1.1 9400-1 Main Board - Introduction

1.1.1.1 General Remarks

This board, which covers the underside area of the 9400 DSO, carries the micro-computer system which is the seat of control for the entire system, and also contains a number of ancillary functions which do not need extra boards. The sections will be described in approximately the order in which they appear in the schematic (8.1). The block diagram <1.1.1.1> shows the main functions which are served by the 9400-1 board.

1.1.1.2 Analog and Digital Functions

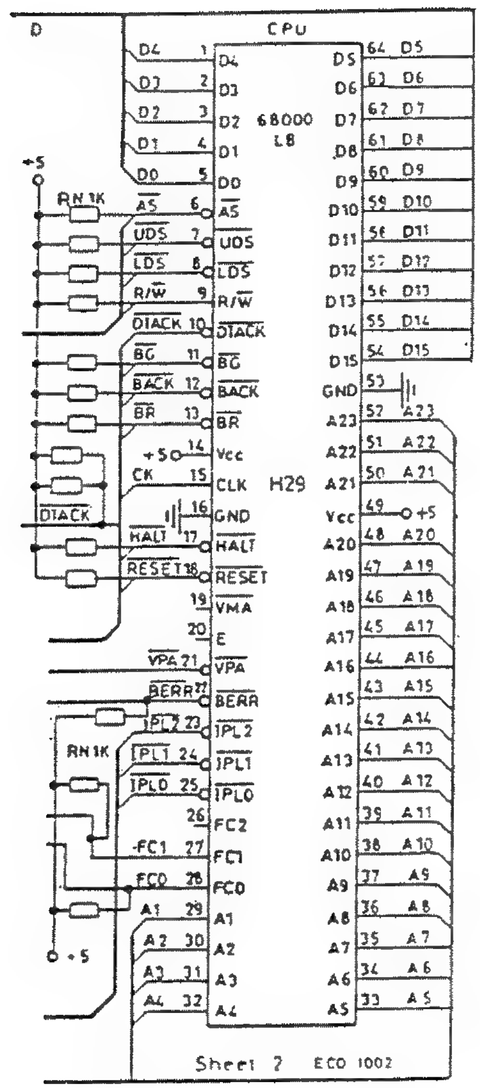
It is important to know that the 9400-1 board carries not only the main control logic of the 9400 DSO, but also the analog frontends and associated functions; this is for reasons of high speed circuit layout.

1.1.1.3 Microprocessor

The micro computer system is based on the powerful and versatile Motorola 68000 <1.1.1.2> which provides 23 address lines, byte control lines, and 16 data lines. The system is too complex to describe in great detail here; an account of its capabilities will be found in the Motorola User's Handbook, sections of which will be referred to like this - (68000 2-3). Motorola does not accept any responsibility or liability for any consequence of the use of information in this document, concerning Motorola products.

1.1.1.4 68000 Data Organization

Operands and data can be specified as byte (8 bits), word (16 bits), or long word (32 bits) (68000 2-3). Words and long words can begin only on even addresses, the high order byte of a pair being stored at the even address. That is why the 68000 has no A0 line; addressing is by word, not byte, and the A0 function is performed by UDS and LDS, the upper and lower byte select strobes.



MICROPROCESSOR MC68000

Figure 1.1.1.2

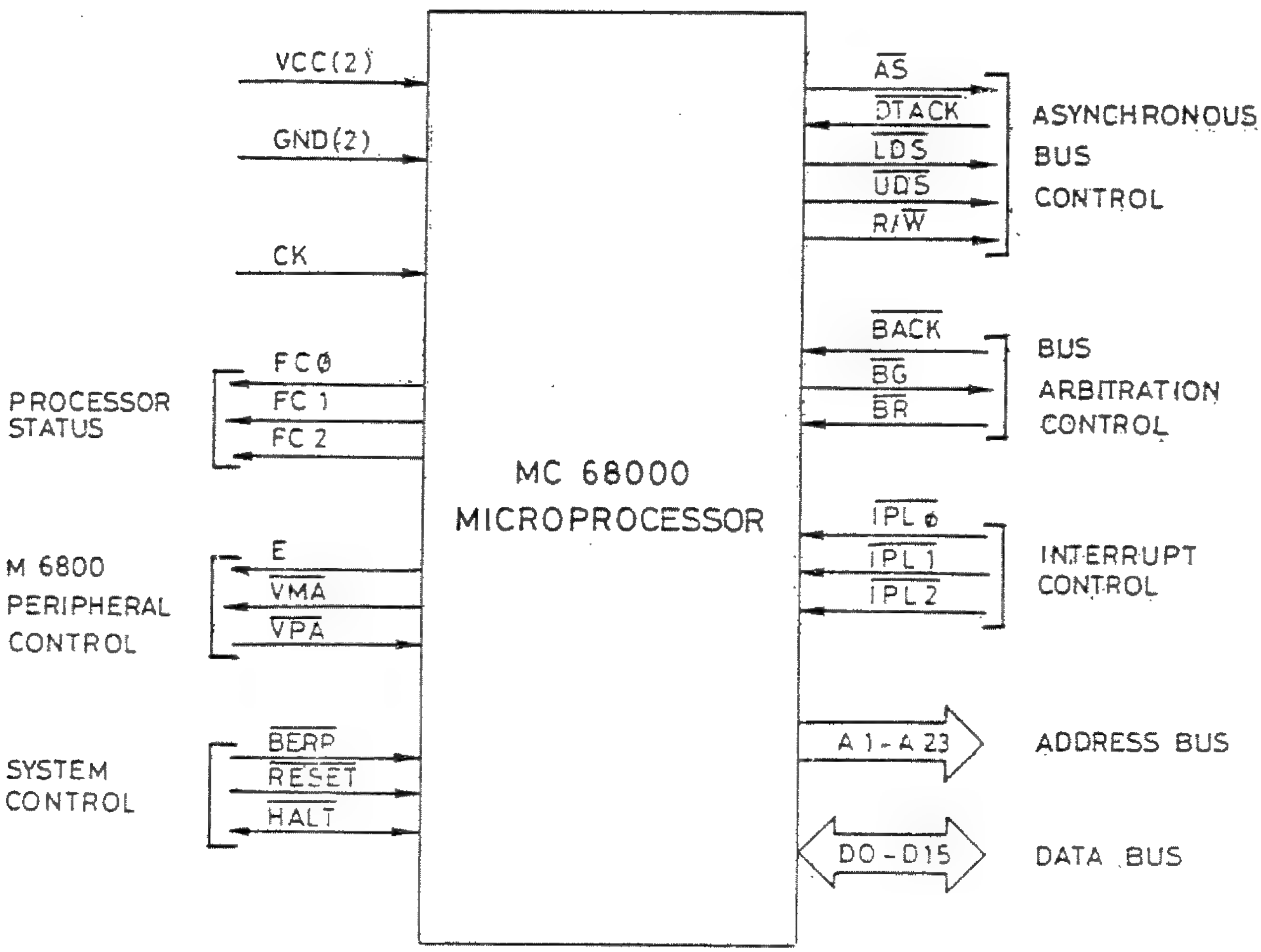
1.1.1.5 Interrupts

The Motorola 68000 has a powerful system of interrupts, providing seven priority levels (68000 5-8). In the 9400 DSO the interrupt system is used in the simple auto vector mode (68000 6-7), which is compatible with the 68000, and provides seven interrupt vectors; see (1.1.7) for hardware implementation.

1.1.1.6 Nomenclature

Throughout this manual, all descriptions involving the 68000 or its control and data lines will use the standard Motorola nomenclature.

The architecture of the computer system of the 9400 DSO was designed with the aim of optimizing the system for controlling a measuring device, rather than for general computing efficiency.



MICRO PROCESSOR MC68000 - PINOUT GROUPINGS

Figure 1.1.1.3

1.1.1.7 Signal and Bus Connections

This is only a brief introduction; see (68000-4) for more details. The lines can be functionally grouped as in <1.1.1.3>.

A - Address Bus A1 - A23

This is a 23 bit, unidirectional tri-state output bus, which is used in word or byte mode. It can address 8 Mwords of 16 bits. It provides addressing for the bus except during interrupt cycles. During interrupt cycles, A1 - A3 describe the interrupt level, while A4 - A23 are held high.

D - Data Bus D0 - D15

This is a 16 bit, bidirectional tri-state bus, used in word or byte mode.

Asynchronous Bus Control

AS - Address Strobe. Indicates valid address is present.

R/W - Read/Write. Defines direction of data transfer.

UDS, LDS - Control upper and lower bytes on the bus.

DTACK - Data Acknowledge. Input indicates completion of data transfer.

Bus Arbitration Control

BR - Bus Request. Input wire ORed with all other potential bus masters which tells 68000 that another device requires to be bus master.

BG - Bus Grant. This output indicates to other potential bus masters that the 68000 will relinquish control after the current cycle.

BACK - Bus Grant Acknowledge. Input to show that another device has become bus master. BACK cannot be asserted unless:

	1	A bus grant has been received
AND	2	AS is inactive, i.e., 68000 is not using bus
AND	3	DTACK inactive, i.e., peripherals not using bus
AND	4	BACK inactive, i.e., no other device is master.

IPL0 - IPL2 - Interrupt Control

Encoded inputs indicating priority of device requesting an interrupt. Level 7 has highest priority, while 0 shows an absence of request. (68000-5).

System Control Lines

BERR - Bus Error, as a result of one of the following:

1 Non-responding device
2 Interrupt vector problem
3 Illegal access request
4 Device dependent errors

RESET - Bidirectional line. Input used to allow CPU reset from external device. Output allows CPU to reset all external devices using RESET instruction (4F70H). External RESET and HALT together will reset entire system.

HALT - Bidirectional line enabling external device to stop CPU at end of cycle. Can be driven by CPU to give signal of CPU stoppage to external devices.

68000 Peripheral Control

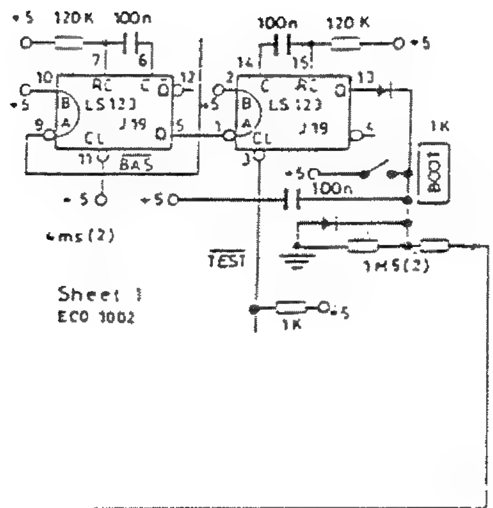
FC0 - FC2 - Processor Status. Function codes indicating current mode of CPU.

CLK - Clock. Internally buffered clock input.

1.1.1.8 Notes

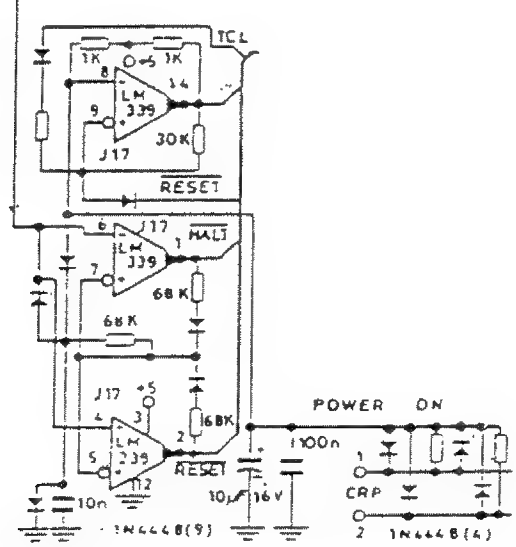
Peripherals are all memory mapped. The addresses are not fully decoded; which means that each peripheral can be addressed modulo n, where n depends on the space used by the peripheral.

The lines FC are used in the 9400 DSO only during interrupt requests at levels 7 and 3. User/supervisor modes are not decoded.



AUTO REBOOT CIRCUIT

Figure 1.1.2.1



POWER ON RESET

Figure 1.1.3.1

1.1.2 Auto Reboot Circuit

In the event of a hangup of the computer system, the 74LS123 dual monostable, J19 <1.1.2.1>, will no longer receive a train of pulses from BAS (1.1.15), and will, if the interruption lasts more than about 4 ms, supply a positive pulse to the boot circuit (1.1.3). If the 9400 DSO is in test mode, the clear line, pin 3, is held down by the TEST signal, and reboot does not take place. Note that if the fault condition is not cleared, reboot will recur continually, and the DSO will never become usable.

1.1.3 Power On Reset Circuit

In order to provide an orderly succession of events, and initialization into a standard configuration, the power on reset circuit provides the necessary signals <1.1.3.1>. This circuit can be triggered by the auto reboot (1.1.2).

The time constants controlling HALT, RESET and CLEAR can be seen in <1.1.3.1>, where they hold down the relevant inputs of the LM339 comparators, J17.

After power on the following sequence occurs:

1.1.3.1 For at Least 100 ms:

- RESET, HALT and CLEAR are held low
- The 68000 is initialized
- Interrupts are disabled
- The CRT beam deflections are held at zero (1.2.5)
- The CRT beam current is held off (1.2.5)
- The sample-and-holds are disabled (1.3)
- The backup RAM is connected to the bus (1.1.22)

1.1.3.2 After Less than 500 ms from Power On:

- RESET and HALT go high, booting the processor
- The DSO initialization begins
- The dynamic RAM refresh is turned on
- Interrupts are enabled
- The display remains disabled
- Sample and holds remain disabled

1.1.3.3 The CLEAR Line Goes High

- The processor tests various functions
- It sets up the display functions
- It sets up the acquisition functions
- Set 1st word of display page 1 = End of Page

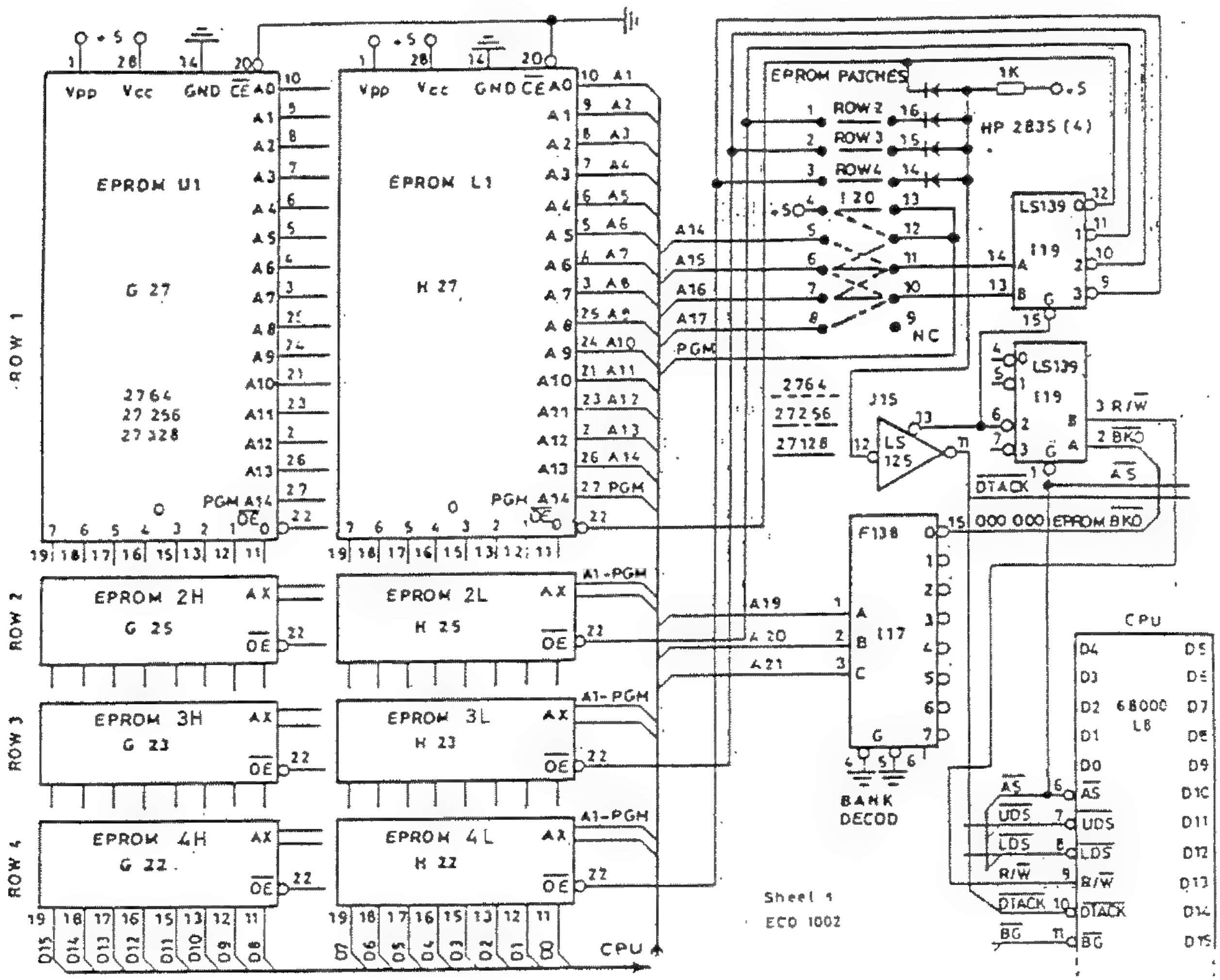
1.1.4 EPROM Addressing

The EPROM sockets <1.1.4.1> are addressed by part of I19, a 74LS139 dual 2-to-4-line decoder/multiplexer, via the EPROM patch jumpers <5.23.2>. The following configurations can be supported:

2, 3 or 4 pairs of:

EPROM type	IC capacity	Total capacity with 8 ICs
2764	8 K bytes	64 K bytes
27128	16 K bytes	128 K bytes
27256	32 K bytes	256 K bytes

The access cycle takes 4 clock cycles at 8 MHz, i.e., 500 ns.



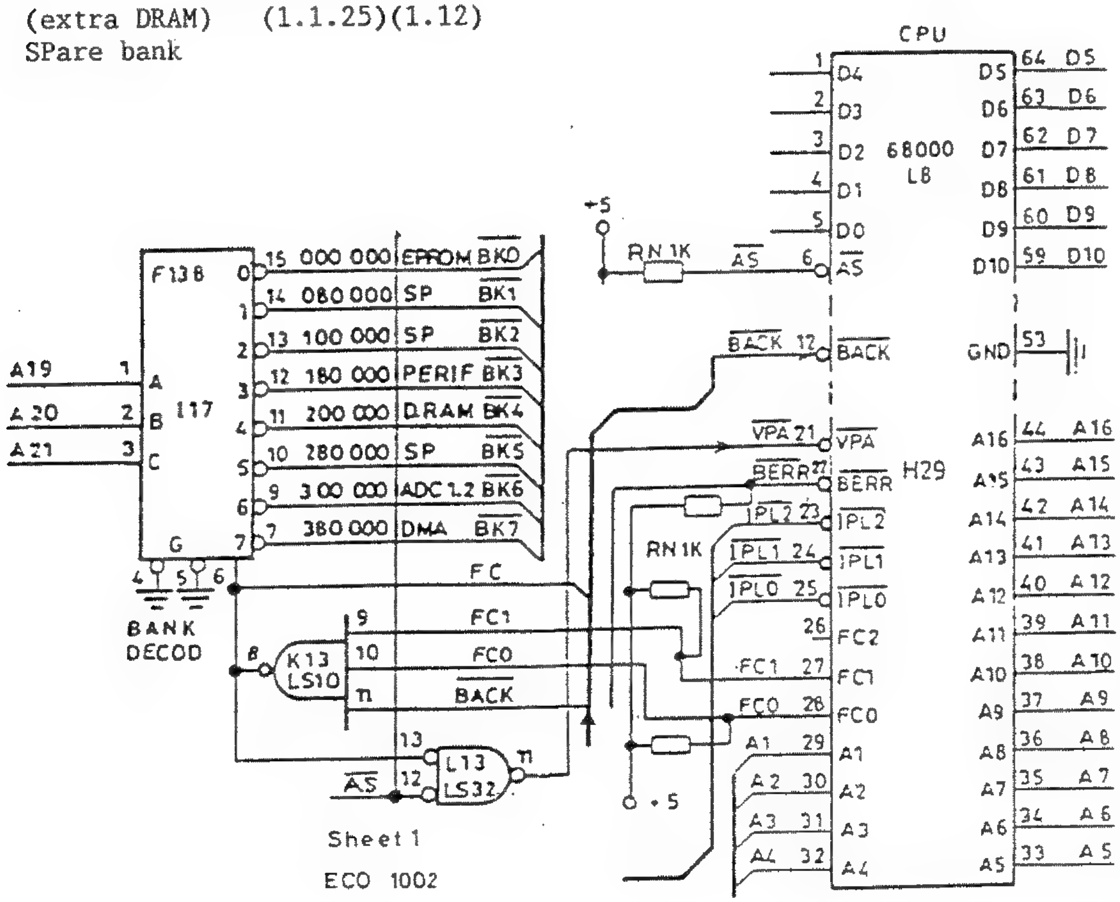
EPROM ADDRESSING CIRCUITS

Figure 1.1.4.1

1.1.5 Address Space Bank Decoder

The address space of the 68000 is organized into banks which correspond to different functions, which are decoded from address lines A19-21 by the 74F138 3-to-8 line decoder I17. The diagram <1.1.5.> shows the circuit and the start addresses of each bank. K13 enables I17 via FC except when FC0 and FC1 are high (interrupt acknowledge) and BACK is not asserted. When FC is low and AS is asserted then VPA, valid peripheral address, is generated. See:

EPROMS	(1.1.4)
Peripherals	(1.1.6)
Dynamic RAM	(1.1.12-14)
ADCs	(1.3)
DMA	(1.1.25)
(extra DRAM)	(1.1.25)(1.12)
SPare bank	



ADDRESS SPACE BANK DECODER

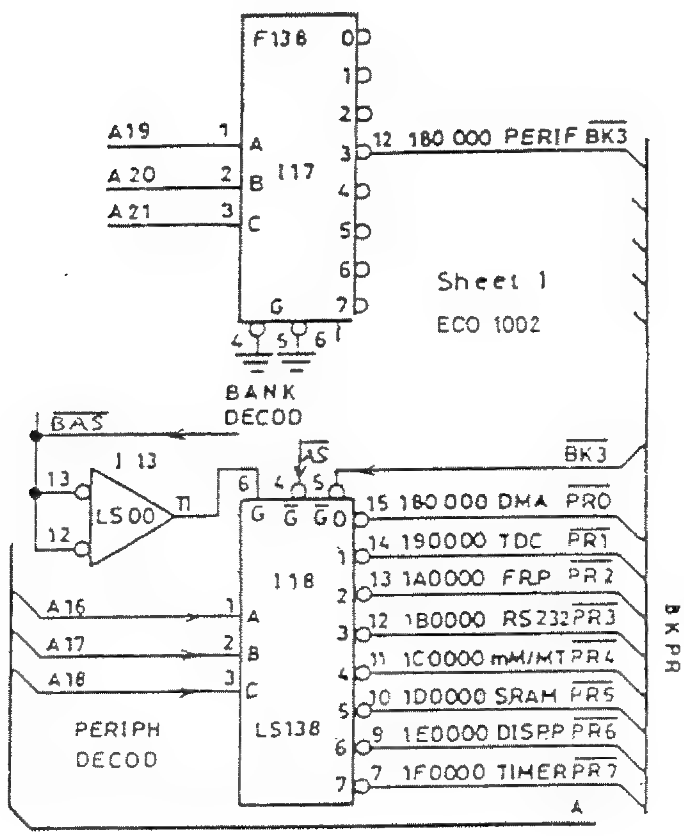
Figure 1.1.5.1

1.1.6 Peripheral Decoder

Each peripheral is allocated a section of the peripheral bank, the sections being decoded by I18, a 74LS138 3-to-8 line decoder/muliplexer, from A16-18 <1.1.6.1>. The eight sections are allocated as follows:

DMA	9401-2	DMA, GPIB, RTC, etc.	(1.1.25)(1.12)
TDC	9400-4	timebase board	(1.4)
FRP	9400-5	front panel board	(1.5) (1.1.21)
RS232	9400-1	RS232 ports 1,2	(1.1.18)
mM/MT	9400-1	min/max/multiply	(1.1.20)
SRAM	9400-1	static RAM	(1.1.22)
DISP.P	9400-1	display processor	(1.2) (1.1.16)
TIMER	9400-1	timer	(1.1.24)

The peripheral decoder is enabled by the simultaneous assertion of BAS, AS and BK3, the peripheral block.



PERIPHERAL DECODER

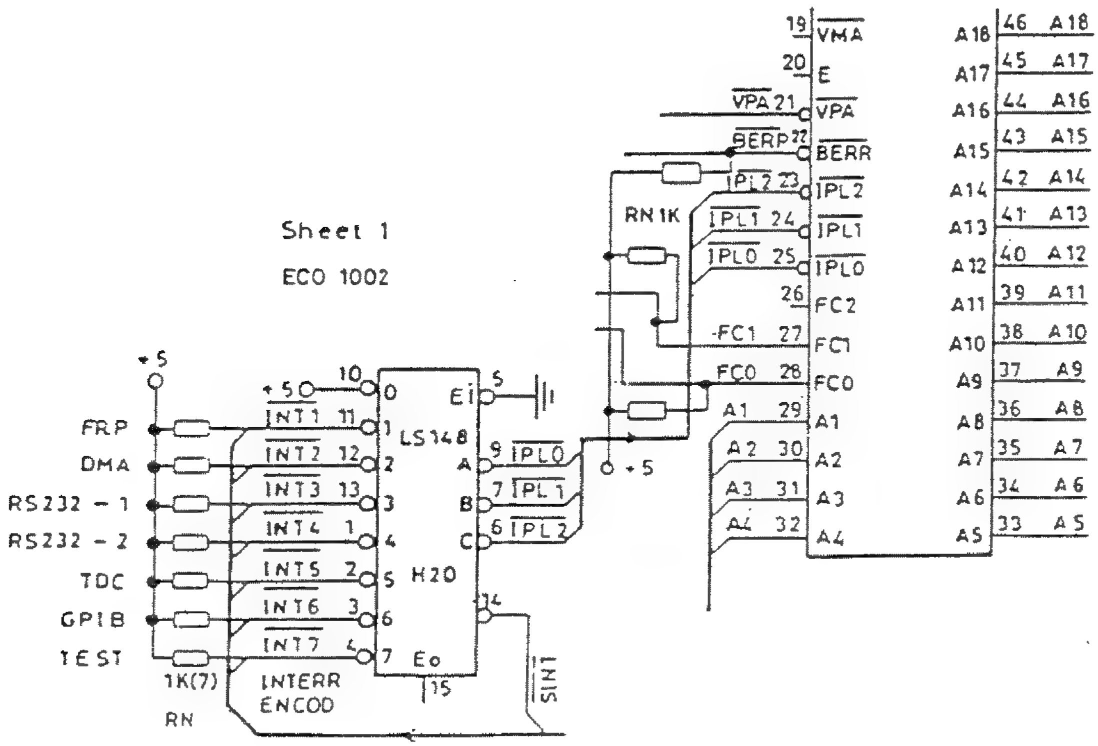
Figure 1.1.6.1

1.1.7 Interrupt Encoder

This circuit <1.1.7.1> uses a 74LS148 8-to-3 line priority encoder to service the seven interrupt lines used in the 9400 DSO. The IPL bus goes to the 68000 CPU (1.1.1). The seven interrupt sources are, in increasing order of priority:

Priority level	Addr	Function	Board
Lowest	64	Front panel	9400-5 (1.5)
	68	DMA slot	9401-2 (1.12), etc
	6C	RS232 p 1	9400-1 (1.1.18)
	70	RS232 p 2	9400-1 (1.1.18)
	74	Timebase	9400-4 (1.4)
	78	GPIB	9400-6 (1.6) older DSOs
			9401-2 (1.12) newer DSOs
Highest	7C	Test slot	4928 tester

If the CPU is blocked for more than 4 ms, the auto reboot circuit comes into play, except in test mode, where the test line clears the monostable (1.1.2). Note that level 7 cannot be inhibited by using the interrupt priority mask.



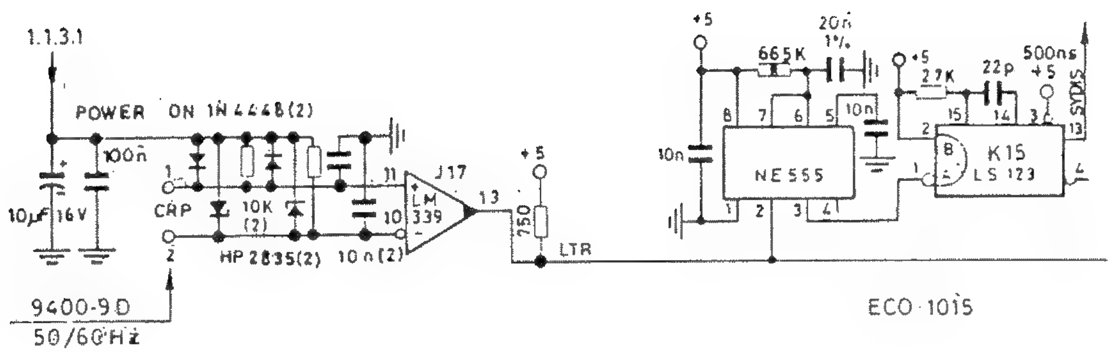
INTERRUPT ENCODER

Figure 1.1.7.1

1.1.8 Display Synchronization

The display is refreshed at the frequency of the public ac power supply, 50 Hz or 60 Hz, so that any stray magnetic fields at this frequency will give only a static distortion of the image, rather than a much more objectionable varying effect. Since both the grid and the waveforms are generated by the same mechanism, any small distortion will have a small effect on readings taken from the screen.

The circuit is based on a comparator, part of J17 <1.1.8.1>, fed with a 50 Hz/60 Hz signal, CRP, from the 9400-9B board (1.9). The comparator is disabled by the power up reset circuit (1.1.3), for a short period after power on. The comparator feeds a 74LS123 monostable, which produces the SYDIS signal for the 9400-2 display board (1.2). The line LTR goes to the front end for use by the trigger circuit (1.1.32) as the line trigger input.

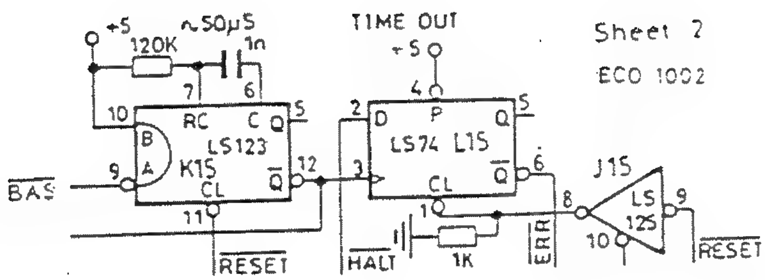


DISPLAY SYNCHRONIZATION

Figure 1.1.8.1

1.1.9 Time Out Circuit

In the event of a peripheral hangup, the time out circuit <1.1.9.1>, based on a 74LS123 retriggerable monostable, K15, produces a signal on the ERR line, feeding E28, a 74LS245 bus transceiver (1.1.10), which sends DERR to the DMA slot (1.1.25). This action occurs if, after initiation of a peripheral cycle, no response has occurred within 200 µs, and a trap is created at address 8. In DMA mode, the signal does not go to the CPU, only to the DMA slot (1.1.10.2).



TIME OUT CIRCUIT

Figure 1.1.9.1

1.1.10 Bus Buffering System

1.1.10.1 General Description

The buses of the 9400-1 board, and their relationships, can be seen in the block diagram <1.1.1.1>. The unbuffered 68000 buses, A1-23 and D0-15, are buffered to and from the buses BA1-23 and D0-15 respectively, by the five 74LS245 octal bus transceivers, F23, F26, F29, and J25, J28. The control lines AS, UDS, LDS, R/W and ERR are treated similarly, by E28. The data bus RR0-15, from the display (1.2) (1.1.16), calibration controller (1.1.17), and DRAM (1.1.14), is buffered by two 74LS244 octal buffers, J23 and J27. A list of labeled lines (1.20) and buses (1.21) can be found at the end of this chapter. The direct buses go only to the CPU, EPROM, DRAM, and the buffers to the amplified buses BA, BD. These buses go to all other peripherals. They can drive up to 20 TTL loads. Their timing is about 10 ns behind the direct bus.

The directions of the buffers are controlled as follows:

E28, E29, F23, F26 are in the direction BA to A, BAS to AS, etc, if BACK is asserted.

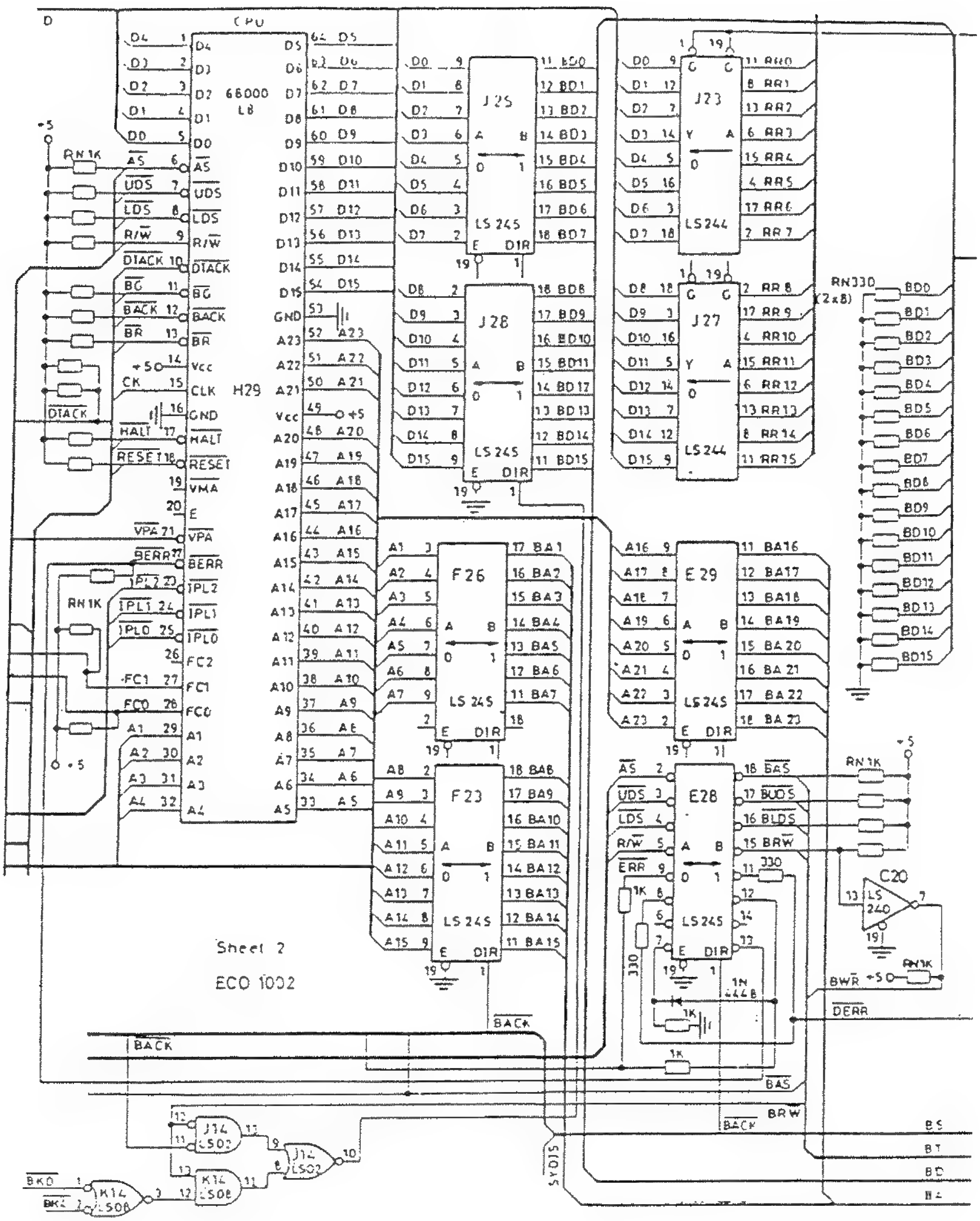
J25, J28 are controlled by a combination of BACK, BRW, BK0, BK4, at J14, K14.

J23, J27 are controlled by K10, K11 of the RAM select circuit <1.1.12.1>.

1.1.10.2 ERR, BERR, DERR

The circuit around E28 pins 7-13 enables the following functions to occur:

- Direction A to B — ERR produces DERR, and BERR to 68000, with the possibility that DERR and BERR can be pulled up, and therefore disabled, by Q2 on the 9401-2 and 9400-6 GPIB boards (1.12)(1.6).
- Direction B to A — ERR produces DERR, but does not produce BERR at the 68000, because the buffer is in the wrong direction.



BUS BUFFERING SYSTEM

Figure 1.1.10.1

1.1.11 Connections to Daughter Boards

There are five connectors on the 9400-1 board which serve the five vertically mounted boards <1.1.11.1>; these are listed below in left-to-right order in the DSO <5.0.2>:

– Display slot		9400-2	(1.2)	
– DMA slot		9400-6	(1.6)	
	or	9401-2	(1.12)	
	and	4928	(3.2)	tester
– Channel 1 ADC	slot	9400-3	(1.3)	
– Channel 2 ADC	slot	9400-3	(1.3)	
– Timebase slot		9400-4	(1.4)	

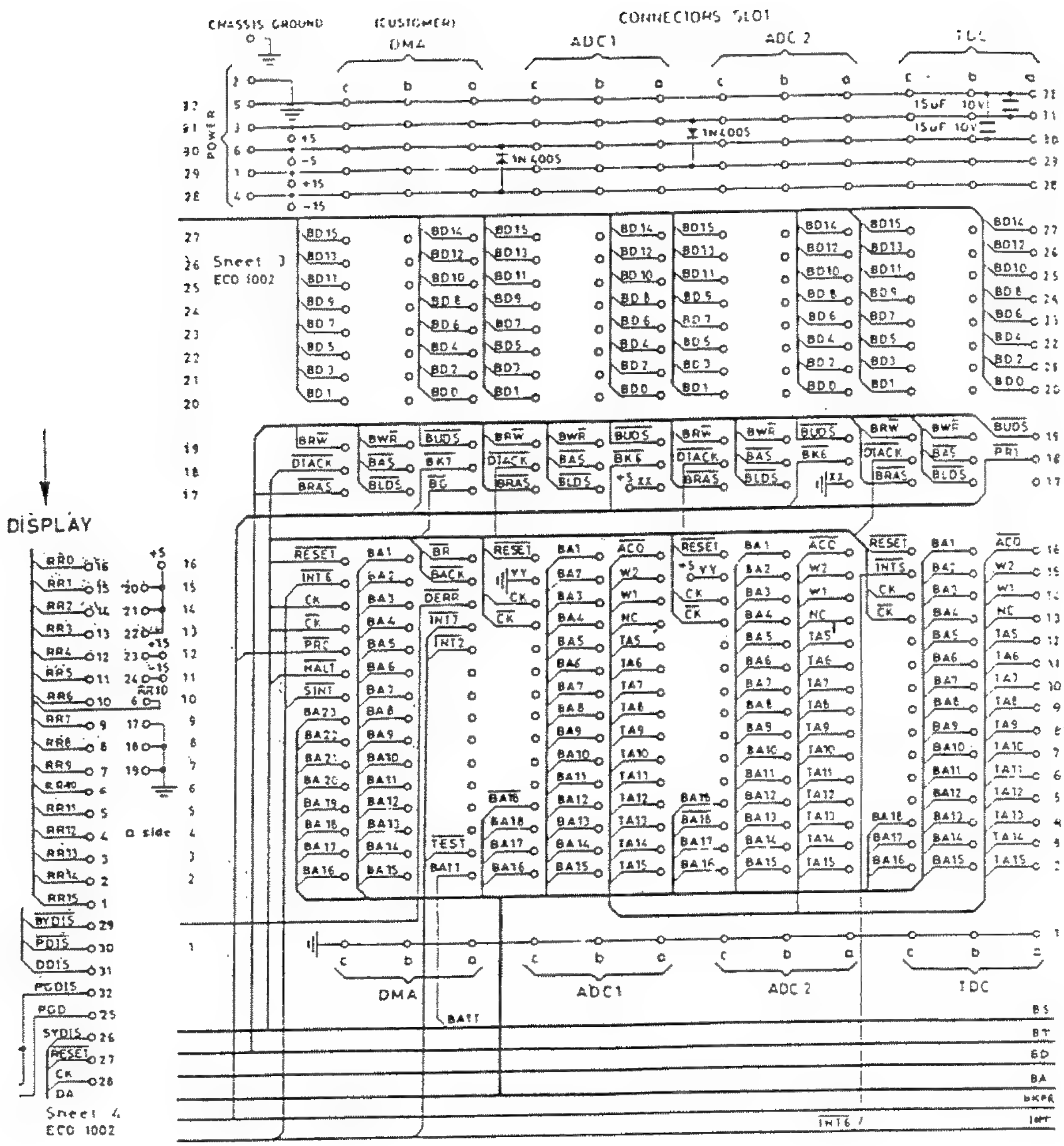
These slots supply:

– Power	+5 V	-5 V	+15 V	-15 V			
– Buses	BA	BD	TA	RR			(1.1.10)
– Controls	BAS	BUDS	BLDS	BRW	BWR	DTACK	(1.1.1.4)

– Special signals to and from each board

Timing diagrams can be found in the descriptions of the individual boards.

Note that the TA bus connects only the 9400-3 and 9400-4 boards.



CONNECTIONS TO DAUGHTER BOARDS

Figure 1.1.11.1

1.1.12 Dynamic RAM Controller

This section <1.1.12.1> controls access to the dynamic RAM (DRAM) (1.1.14) using the signals:

- AS	address strobe	(1.1.1)
- CLEAR	general clear	(1.1.3)
- DDIS	data request from disp.	(1.2)
- BRW	read/write select	(1.1.1)
- CK	8 MHz clock	(1.1.15)
- T8	16 µs clock	(1.1.15)
- T11	128 µs clock	(1.1.15)
- BK4	DRAM block select	(1.1.6)

- BYDIS	RAM busy
- DTACK	data acknowledge

- From these are generated:

- RAS	row address strobe
- CAS	column address strobe
- WEL	write enable lower byte
- WEU	write enable upper byte

CAS and RAS are needed to service the 8-to-16 line address multiplex in the 2164 DRAMs, allowing 64 K of addressing from eight lines.

WEL and WEU select lower or upper byte in the 68000 address scheme (1.1.1.4).

The following functions are listed in order of decreasing priority:

- GBUS	enable RAM for processor bus
- GDIS	enable RAM for display
- GCAL	enable RAM for calibration DAC samp/hold
- GREF	enable RAM refresh

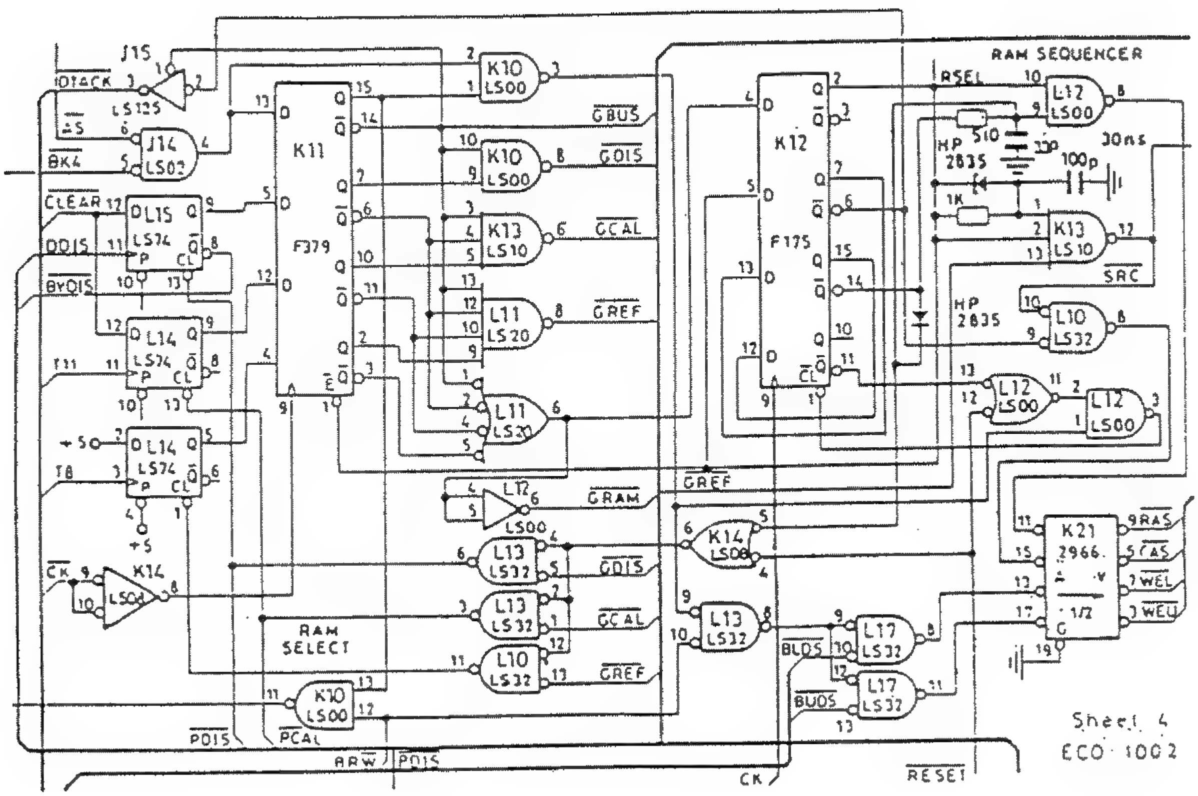
The 9400 DSO processor runs at a speed which allows refresh to occur at an adequate rate.

Occupation times are typically:

Display with 1000 vectors, about 2.5% at 50 Hz and 3% at 60 Hz.
Calibration sample and hold, about 4%.
Refresh, about 3%.

Thus the mean access time to the RAM is only slightly increased by these functions.

Note that pin 11 of K10 drives the direction control of J23 and J27 in the bus buffering system <1.1.10.1>.



DRAM CONTROLLER

Figure 1.1.12.1

1.1.13 RAM Address Selection

This section <1.1.13.1> uses the signals GBUS, GDIS, GCAL and GREF (1.1.12) to select the RAM function in the order of priority given in (1.1.12). The circuit uses four 74LS257 quad data multiplexers, a 2966 octal buffer and a 74LS244 octal buffer. T9-11 are binary divisions of the 8 µs clock, and T12-15 are binary divisions of the 128 µs clock (1.1.15). The addresses are buffered by K22, a 2966 octal buffer.

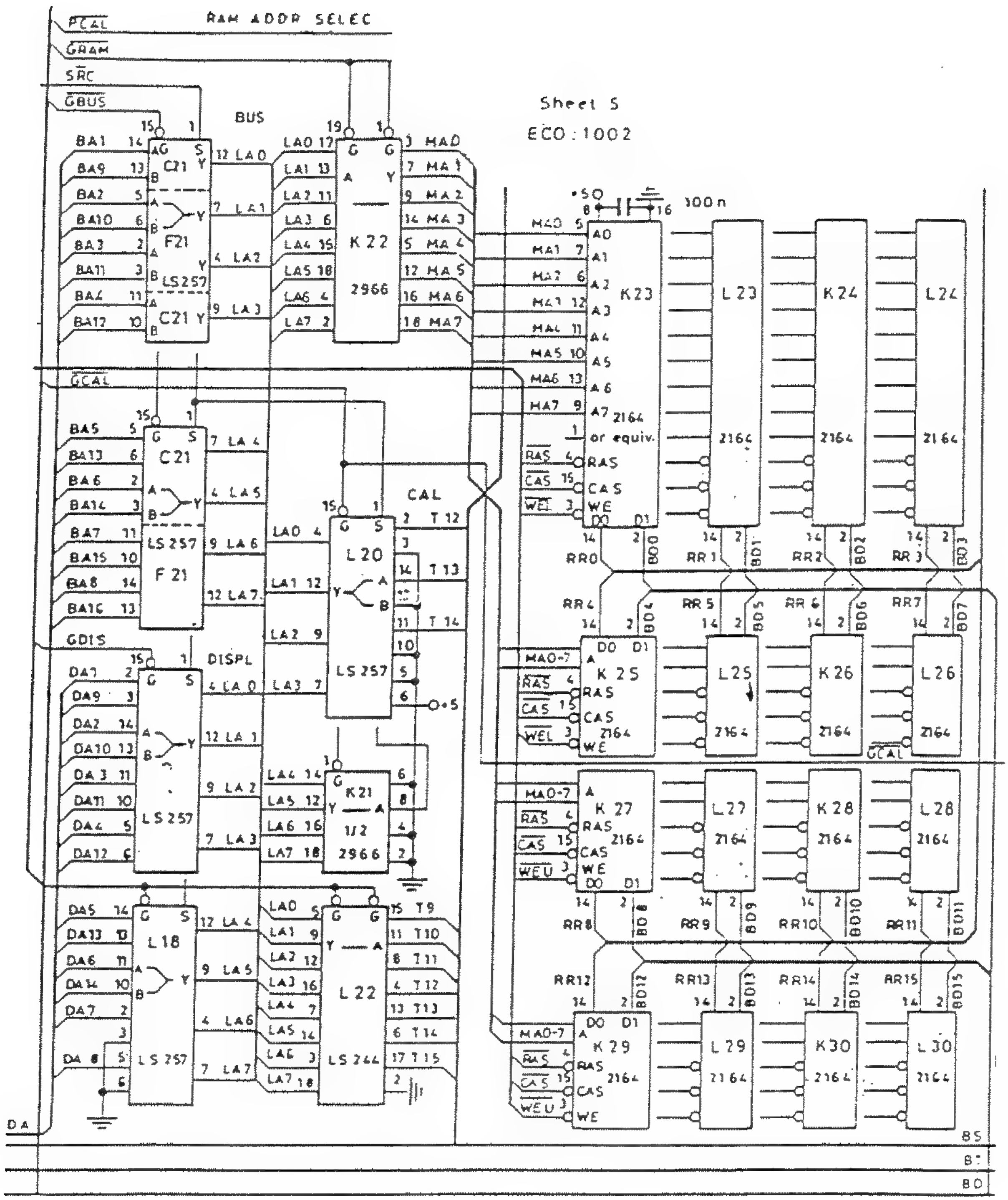
The RAM is allocated to hardware as follows:

200000 to	2027FE	1st page display	5 K words
202800 to	20FFFE	2nd page display	5 K words
205000 to	20500E	refresh cal S+H	8 words
205010 to	205014	jump for INT7	

Access time by CPU bus is 625 ns; access time by RAM is 500 ns.

1.1.14 Dynamic Random Access Memory (DRAM)

The RAM for the 68000 CPU uses 2164 64 K bit DRAMs, which are organized as single bit memories, so that a bank of 16 ICs makes a 64 K, 16 bit memory <1.1.14.1>. The lines A0-7 (9400 MA0-7) are demultiplexed in the DRAMs to 16 address lines, using RAS and CAS (1.1.12), which are activated in turn.



RAM ADDRESS SELECTION + DYNAMIC RAM

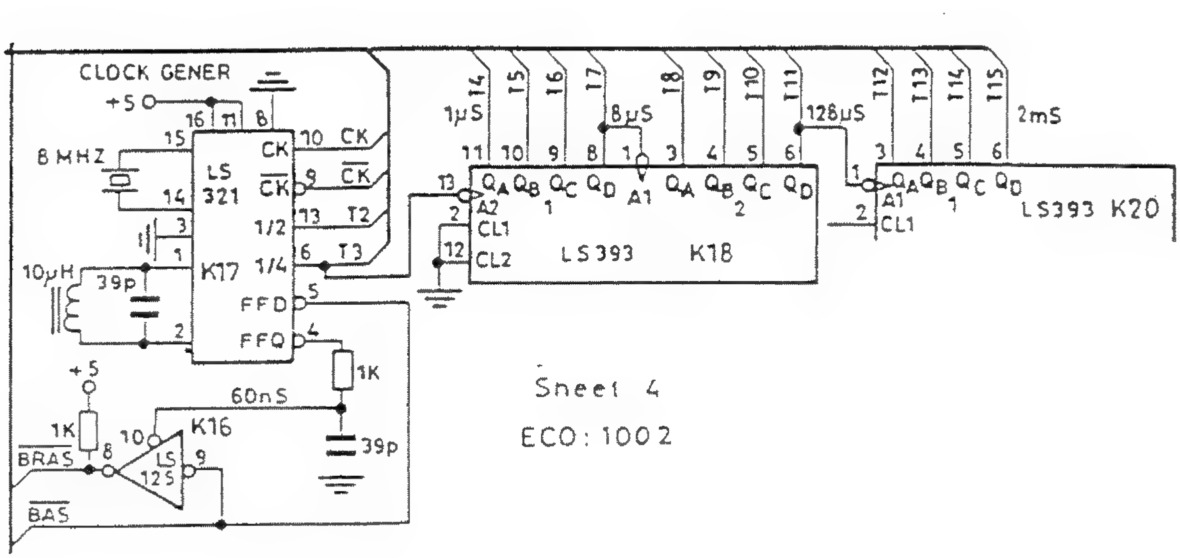
Figure 1.1.13.1 + Figure 1.1.14.1

1.1.15 Clock Generator

The clock generator <1.1.15.1> uses a tank circuit and a crystal, both tuned to 8 MHz, the basic clock frequency for the 68000 in the 9400 DSO. The clock is a 74LS321, giving complementery outputs, and the binary scaled frequencies, T2 and T3. Further binary division is done by K18 and K19, 74LS393 dual 4 bit binary counters, giving periods down to about 2 ms. The flip-flop of the 74LS321 is used to make BRAS at K16 (delayed BAS).

Clock periods and frequencies are - (c = circa)

CK	8 MHz	125 ns	T9	32.25 kHz	32 μs
T2	4 MHz	250 ns	T10	16.125 kHz	64 μs
T3	2 MHz	500 ns	T11	c8.062 kHz	128 μs
T4	1 MHz	1 μs	T12	c4.031 kHz	256 μs
T5	500 kHz	2 μs	T13	c2.016 kHz	512 μs
T6	250 kHz	4 μs	T14	c1.008 kHz	1.024 ms
T7	125 kHz	8 μs	T15	c500 kHz	2.048 ms
T8	62.5 kHz	16 μs			



CLOCK GENERATOR

Figure 1.1.15.1

1.1.16 Display Controller

This circuit <1.1.16.1> is responsible for the transmission of data to the 9400-2 display board (1.2), for conversion to analog signals representing:

- X   horizontal position of spot
- Y   vertical position of spot
- DX   horizontal velocity
- DY   vertical velocity

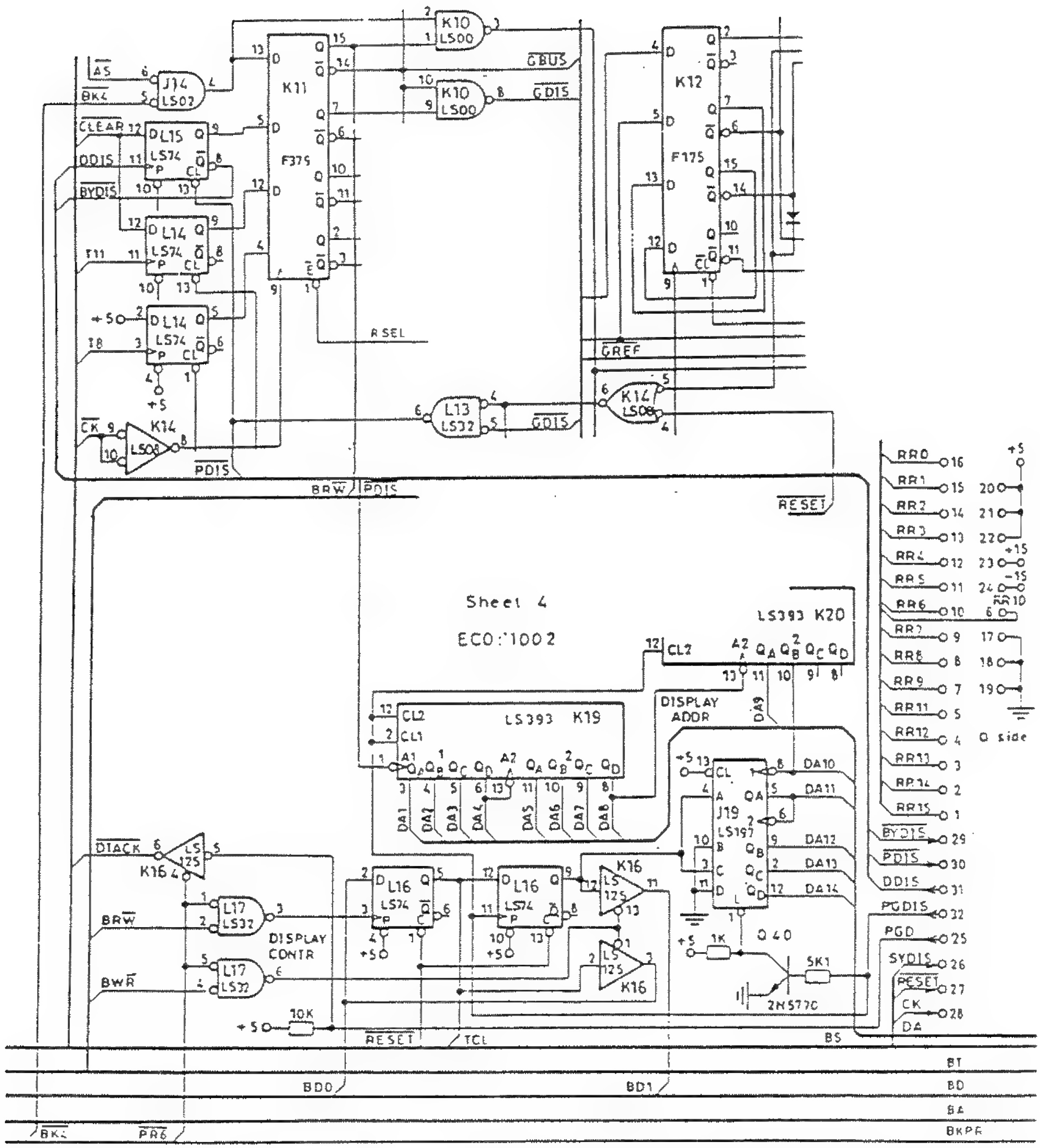
The display data are stored in a dedicated section of DRAM (1.1.13), which is divided into two pages, 0 and 1, one of which at any times holds the current display, while the other is available for the CPU to build up the next, it response to a demand from the front panel or remote control. The prospective and current page numbers are stored in bits 0 (W/R) and 1 (R only) at L16. At the end of scanning one display page, if the two bits differ, bit 0 is copied into bit 1, and the other page is displayed on the next scan, leaving the now unused page ready for the next time a change to the display is needed.

The control signals have the following functions:

- CK   8 MHz clock (1.1.15)
- SYDIS   50/60 Hz page synchronizing pulse (1.1.8)
- RESET   9400 general reset, turns spot off, centers beam (512,512) (1.1.3)
- BYDIS   0 RAM busy, 1 data ready
- PDIS   Load data clock

From 9400-2 to 9400-1:

- PGDIS   acknowledge End of page, wait next SYDIS
- DDIS   request next data
- PGD   0 display board present



DISPLAY CONTROLLER

Figure 1.1.16.1

The activity on the 9400-2 slot <1.1.16.2> is confined to the period between SYDIS and PGDIS.

The 16 bit word on the 9400-2 slot is built as follows:

Mode			Control			Data									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M2	M1	M0	B	I	-	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

These data are encoded as follows:

- B 0 spot off for positioning
  1 spot on for drawing

- I 0 compute only
  1 compute and draw

- M 0 to 3 control word
  0 end of page, spot centered, await SYDIS
  1 mode 0 and mode 3 together
  2 no operation
  3 load Z with D0-7

  M 4 to 7 coordinate word

4	DX=0	D0-9	absolute next Y
5	DY=0	D0-9	absolute next X
6	DX=1	D0-9	absolute next X
7		D0-4	relative next Y
		D5-9	relative next Y

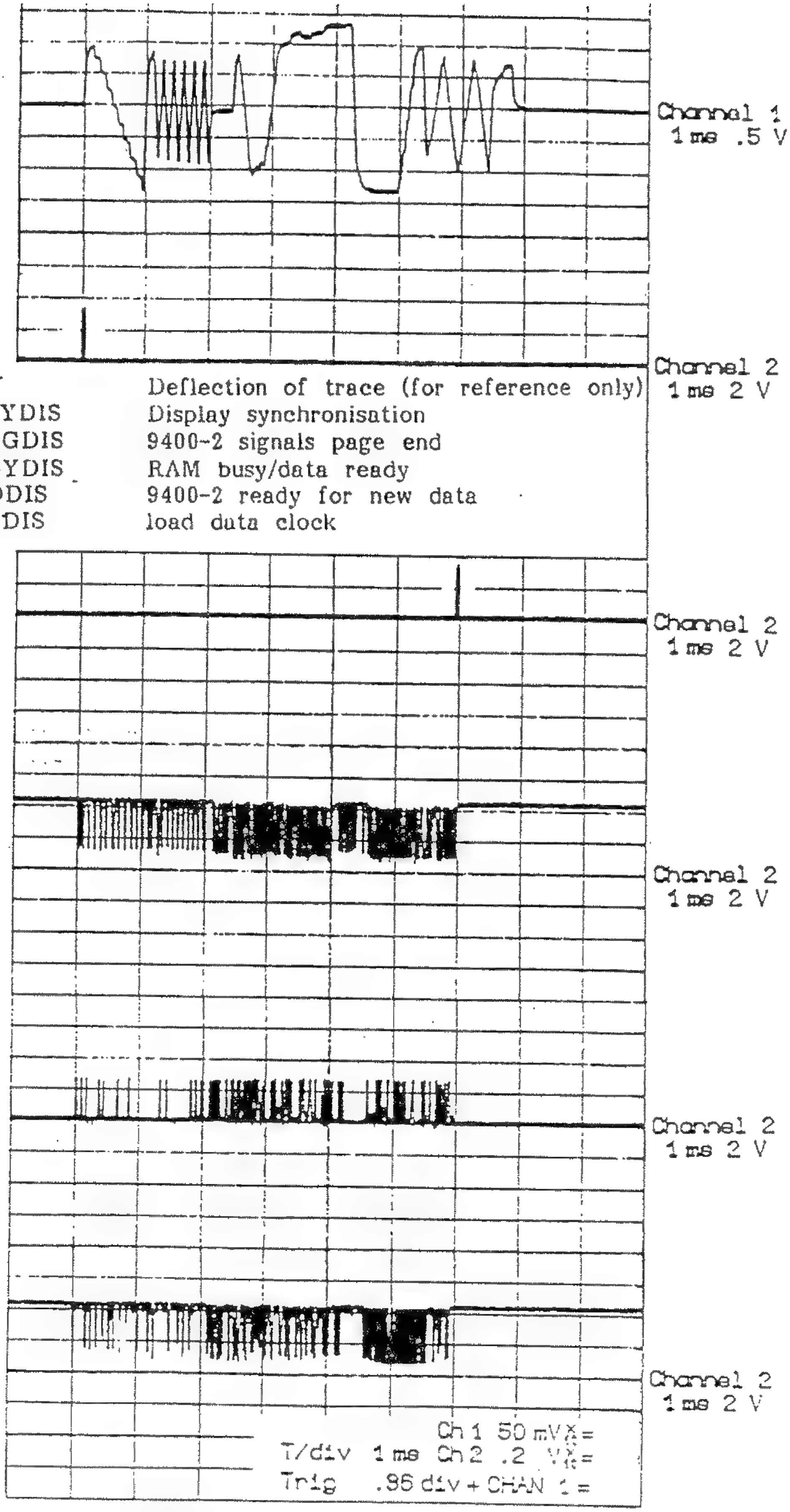
- D 0 to 7 coordinate data

See (1.2) for information on the display board, and (1.1.12)-(1.1.14) for information on the use of DRAM for transmission of data to the display.

Each complete scan, or page, of the display, is initiated by SYDIS, and the 9400-2 returns PGDIS at the end of the page, setting up the next page number to be displayed at L16, a D-type flip-flop, and loading the counters K19, K20, J19 to the first vector address.

Some of the control waveforms are shown in <1.1.16.2>; in order from top top bottom they are:

Y	Deflection of trace (for reference only)
SYDIS	Display synchronization
PGDIS	9400-2 signals page end
BYDIS	RAM busy/data ready
DDIS	9400-2 ready for new data
PDIS	load data clock



CONTROL WAVEFORMS FOR THE DISPLAY

Figure 1.1.16.2

1.1.17 Calibration Controller

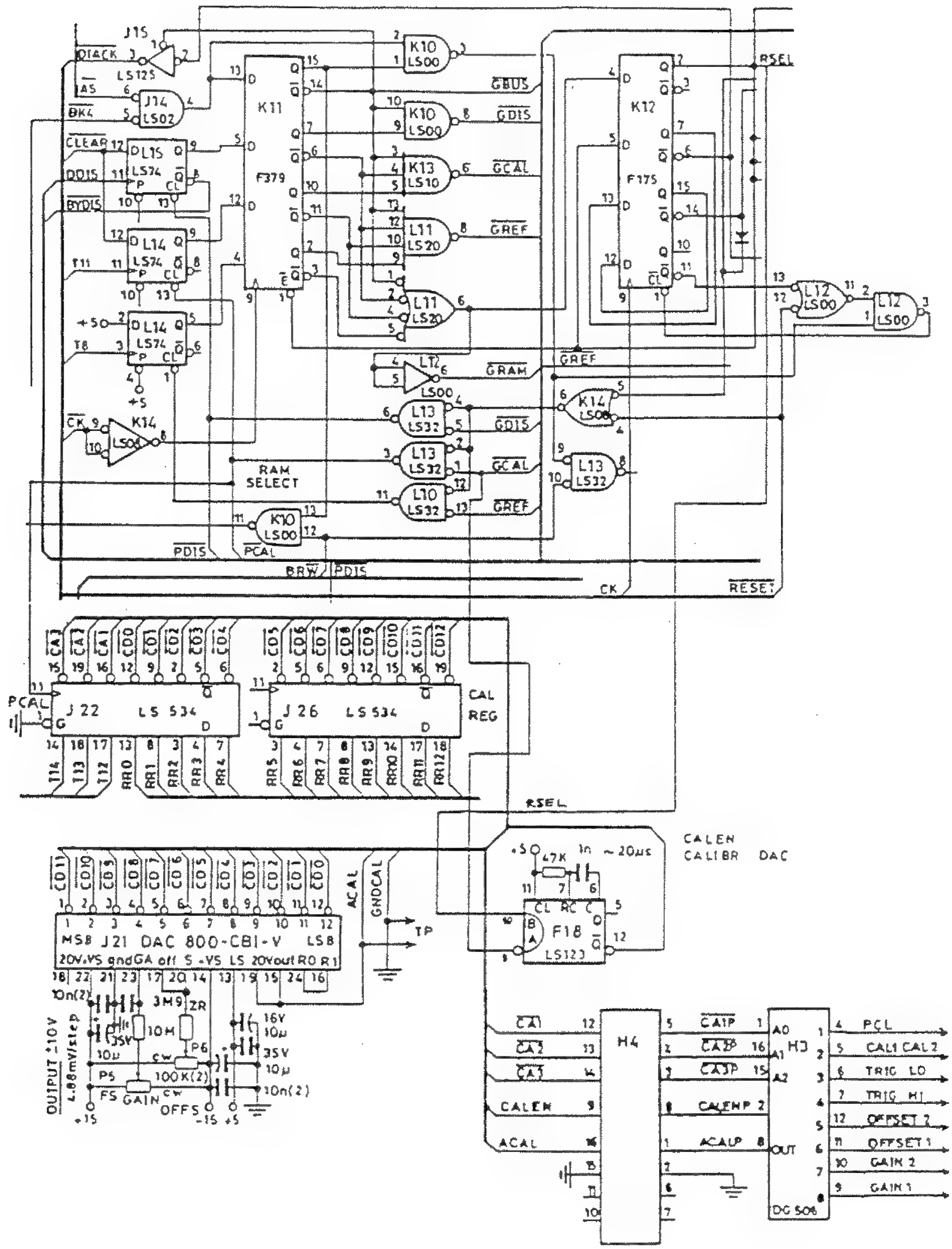
This circuit sends an analog data stream comprising eight levels, using a DAC 800 12 bit DAC <1.1.17.1>, supplied with 12 bit digital data, CD0 - CD11, from the RR bus, via J22 and J26, clocked by PCAL <1.1.12.1>. Three other channels of J22 transmit the clock lines <1.1.15.1> to the CA bus, which controls the eight way analog switch H3 <1.1.17.1> <1.1.31.3>. This switch is enabled by CALEN, which is initiated by GCAL and RSEL <1.1.12.1>.

The eight analog signals are generated in the following order <1.1.31.3>:

PCL	Probe calibrator level	<1.1.35.1>
CAL1, CAL2	Frontend calibration levels	<1.1.31.2>
TRIG LO	Low trigger threshold	<1.1.32.1>
TRIG HI	High trigger threshold	<1.1.32.1>
OFFSET 2	Channel 2 offset	<1.1.31.2>
OFFSET 1	Channel 1 offset	<1.1.31.2>
GAIN 2	Channel 2 gain control	<1.1.31.2>
GAIN 1	Channel 1 gain control	<1.1.31.2>

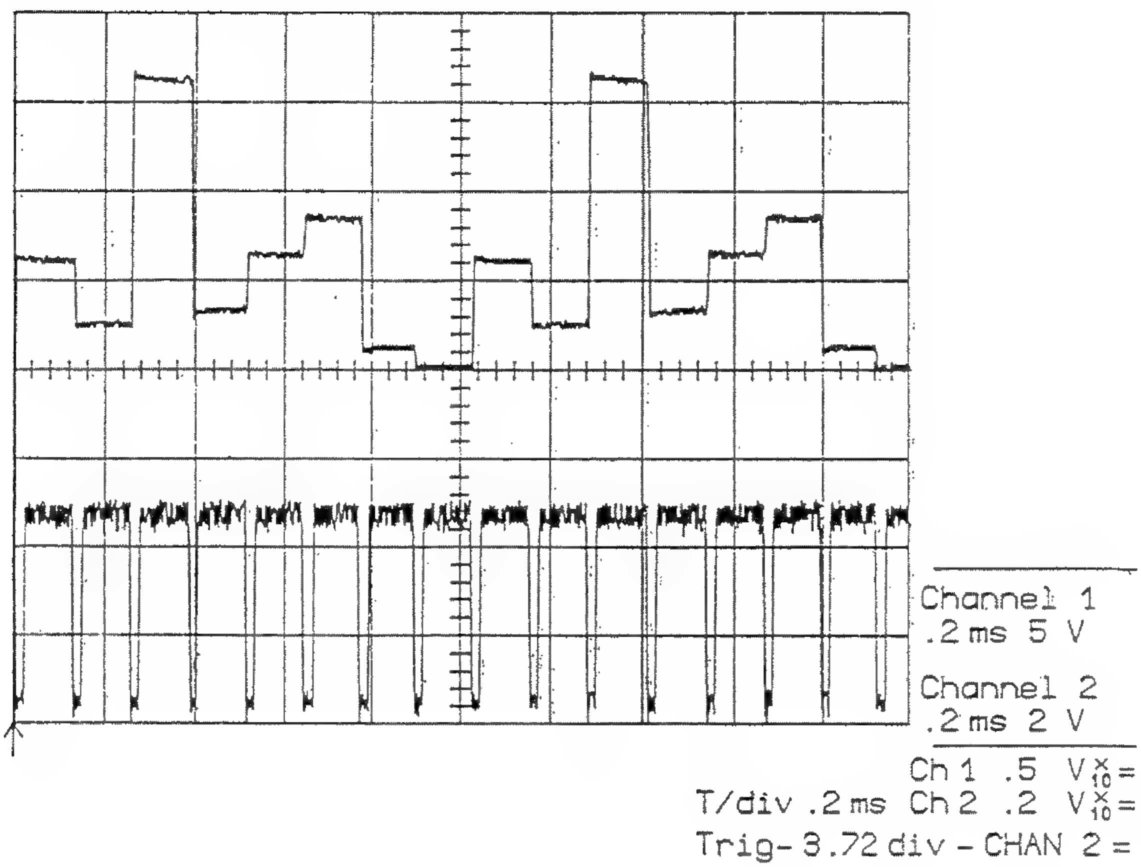
J22 and J26, 74LS534s, hold the sample and hold address and the digital data for conversion by the DAC, which has two preset controls, for gain and for offset.

The signals are shown in <1.1.17.2>, Channel 1 being ACAL, and Channel 2 being CALEN.



CALIBRATION CONTROLLER

Figure 1.1.17.1



SIGNALS FOR THE CALIBRATION CONTROLLER

Figure 1.1.17.2

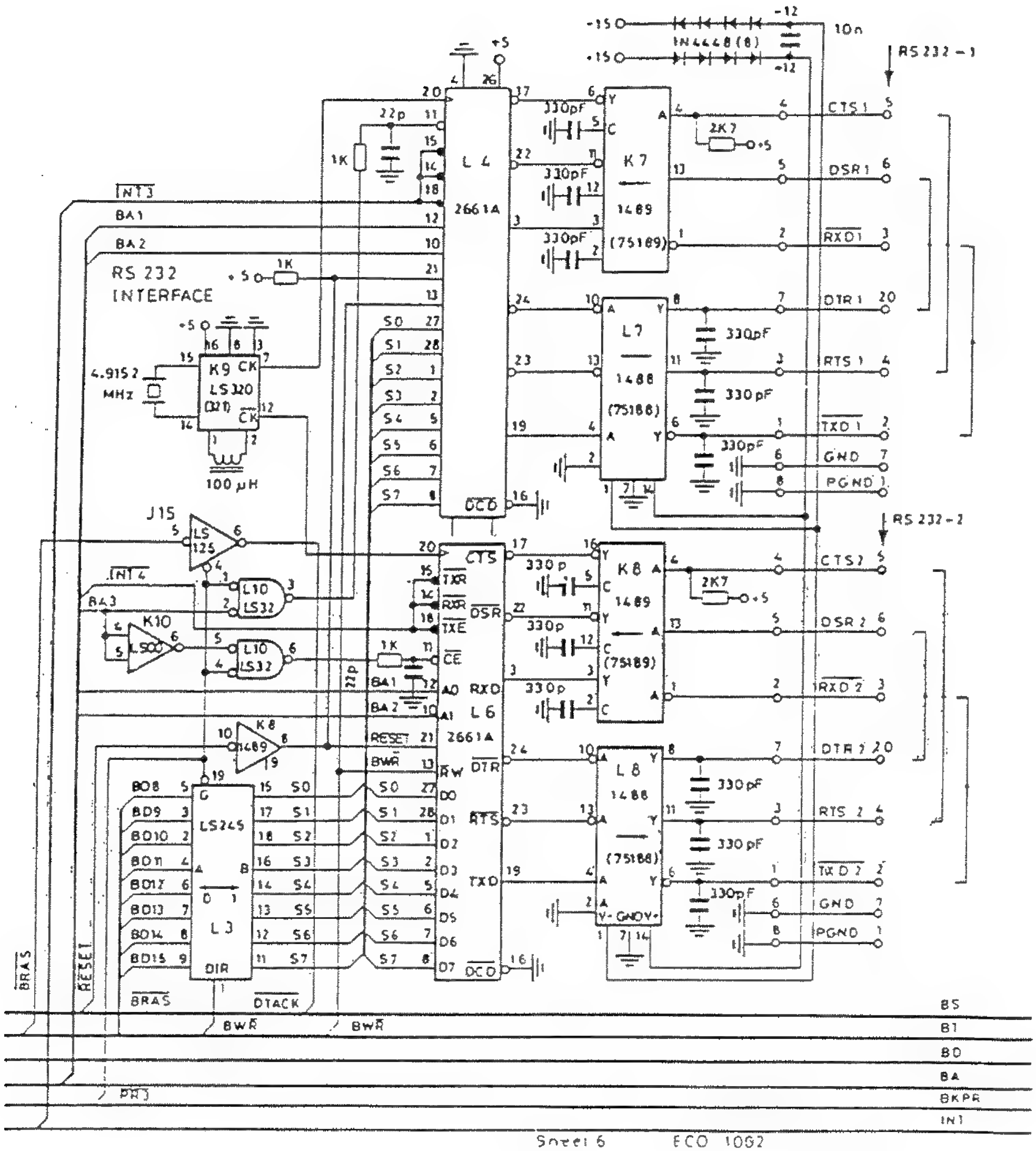
1.1.18 RS232 Interfaces

There are two identical interfaces, port 1 and port 2, the first dedicated to plotters, and the second to control and data transfer.

The bytes for transfer are buffered on the S bus by L3, a 74LS245 bus transceiver. The S bus is connected to D0-7 of two 2661A dedicated RS232 ICs, L4 and L6, selected by pin 11, CE. The 2661As are clocked at 4.9152 MHz by K9.

Each RS232 interface contains four 8 bit registers, addressed by BA1-2. Port 1(2) uses interrupt level 3(4). Access time is 5 clock cycles at 8 MHz, i.e., 625 ns, and cycle time is 9 clock cycles at 8 MHz, i.e., 1125 ns.

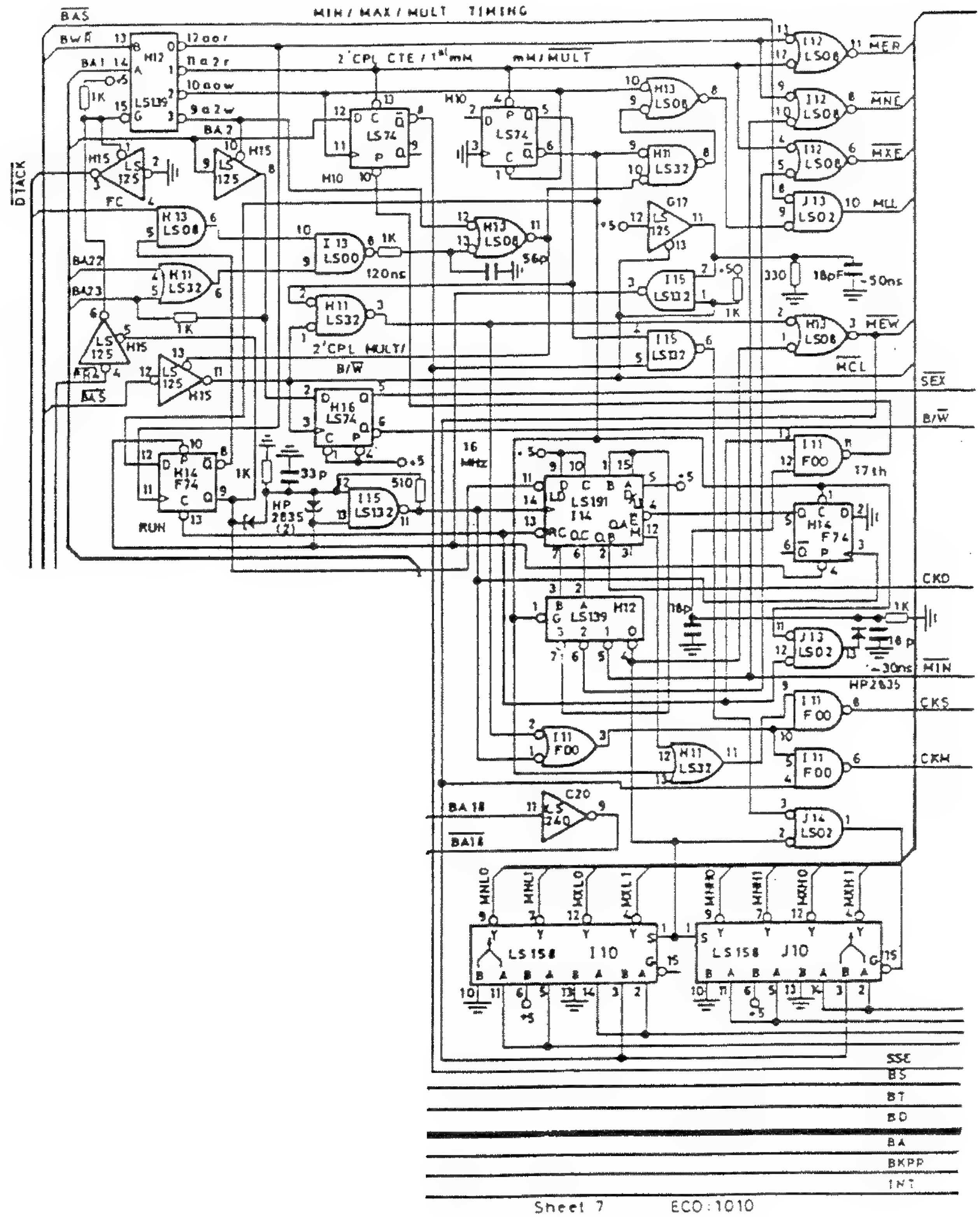
A diagram of the RS232 connectors is given in (4).



RS232 INTERFACES

Figure 1.1.18.1

1.1.19 Minimum-maximum/multiplier Timing



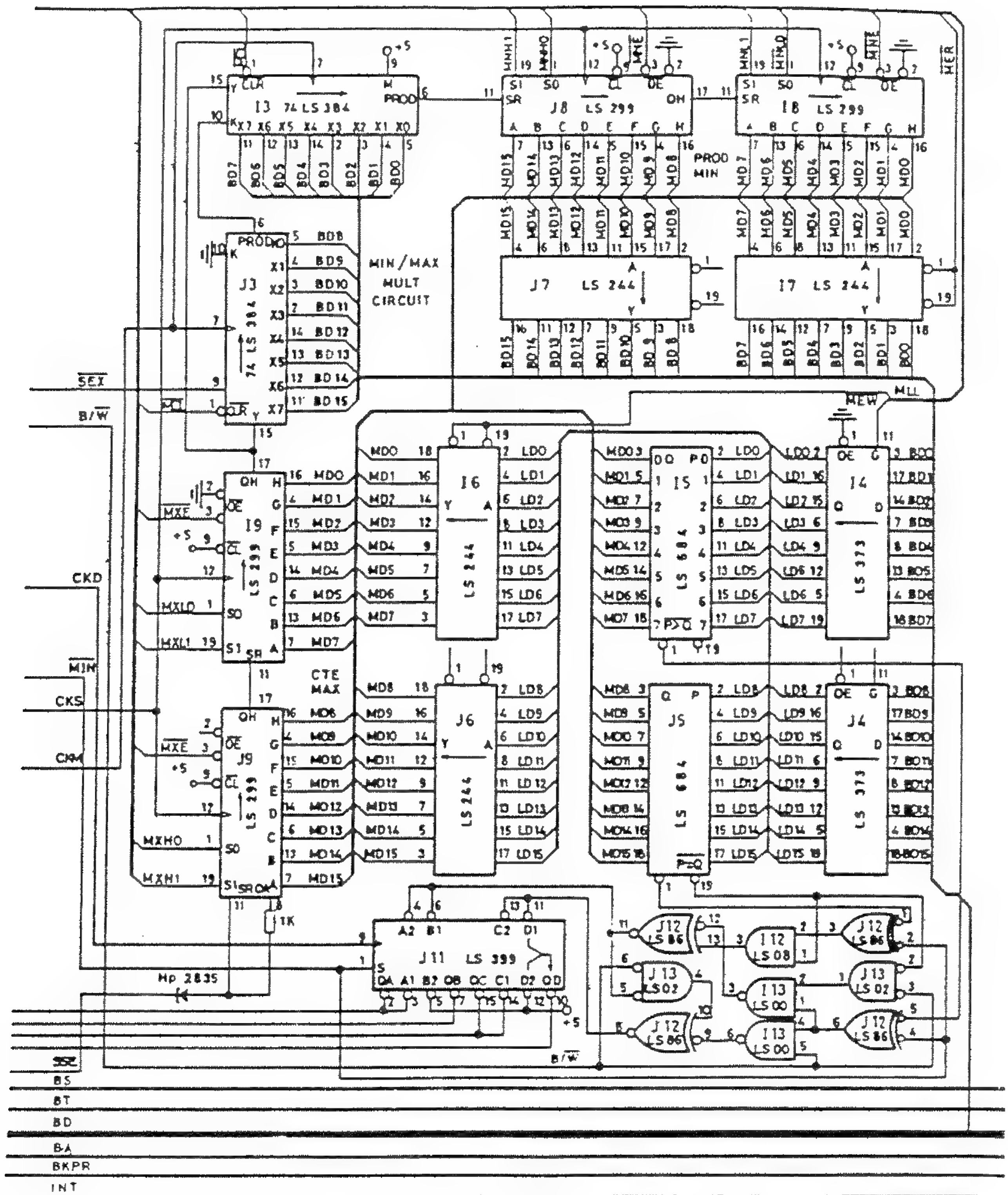
MINIMUM-MAXIMUM/MULTIPLY TIMING

Figure 1.1.19.1

1.1.20 Minimum-maximum/multiplier System

This provides <1.1.20.1>:

- Calculation of minimum and maximum of a series of 16 bit data.
- Calculation of minimum and maximum of a series of pairs of 8 bit data.
- Calculation of a 32 bit product from two 16 bit data, the 16 lsbs of the product read first, and the 16 MSBs by a second access. The product is performed by selectable signed or unsigned data. For both functions, min/max and multiply, the data can be loaded by direct addressing or kept for another bus cycle (selectable).



Sheet 8 ECO : 1010

MINIMUM-MAXIMUM/MULTIPLY CIRCUIT

Figure 1.1.20.1

1.1.21 Front Panel Control and Input Coupling Logic

1.1.21.1 Introduction

These circuits <1.1.21.1> <1.1.21.1A> have the following functions:

- Selecting the required couplings at the trigger and frontend.
- Illuminating the appropriate LEDs on the front panel to show the current function selections.
- Reading the positions of the front panel potentiometers.
- Reading the positions of the front panel rotary switches.
- Detecting any operations of the front panel push button switches.

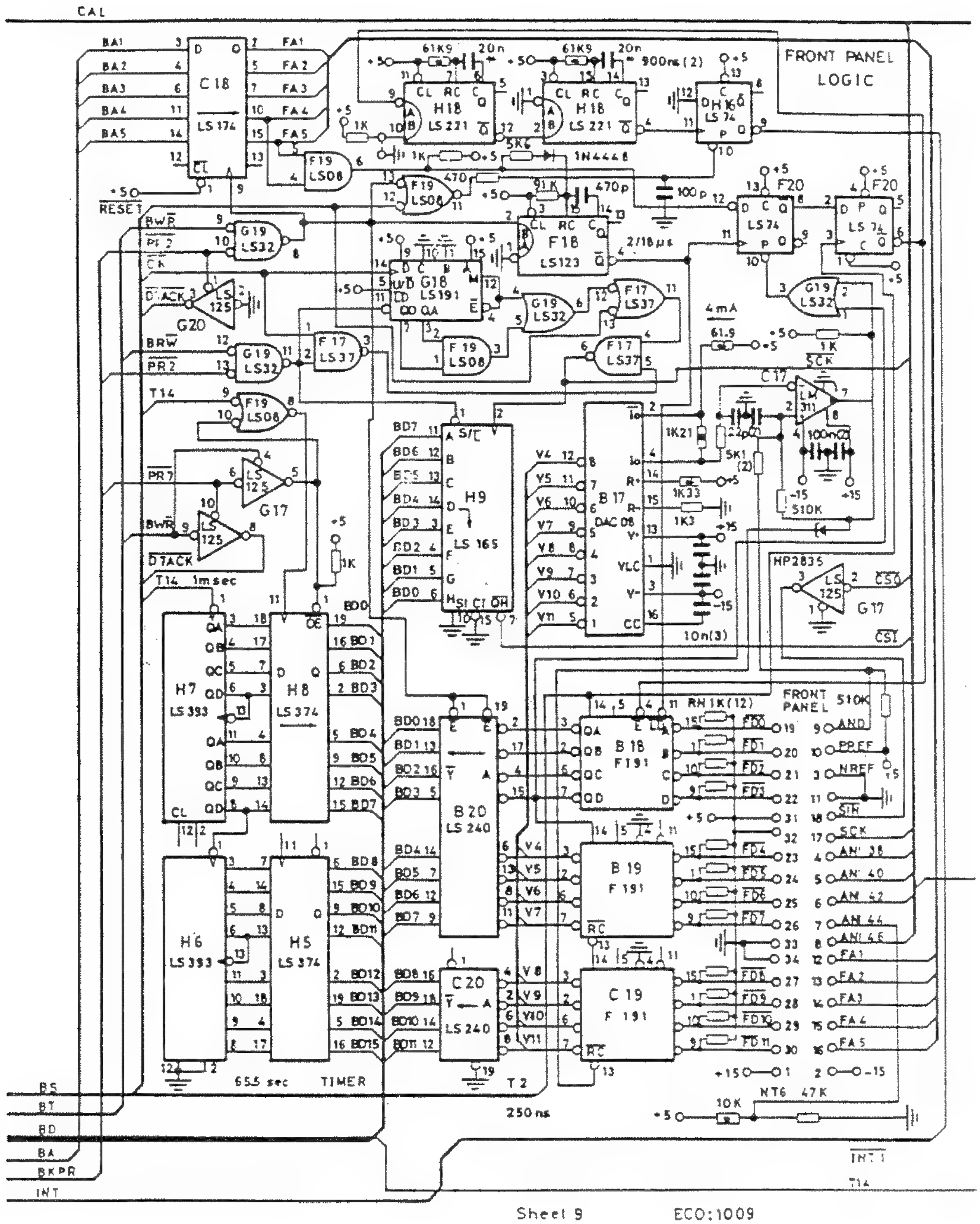
This section should be read in conjunction with (1.5), which describes the front panel controls, (1.1.31), which describes the front end, and (1.1.32), describing the trigger.

1.1.21.2 Input Coupling Selections and Front Panel LEDs

The LEDs and frontend couplings are set up by a serial bit stream feeding serial-to-parallel shift registers on the front panel <1.5.4.1>, on SIN, clocked by SCK; pins 17, 18 of the front panel connector. Signals are sent only when something needs to be changed; for example, on auto, or normal trigger with a repetitive waveform, the READY and TRIGGED lights toggle, so that a steady stream of data is sent on SIN, which carries four bytes for the couplings and four for the LEDs, with a pause after each byte.

The serial data are generated at H9 <1.1.21.2>, a 74LS165 parallel load shift register, taking its clock rate from the binary counter G18, fed by the 8 MHz clock CK, and loaded by PR2.BRW.

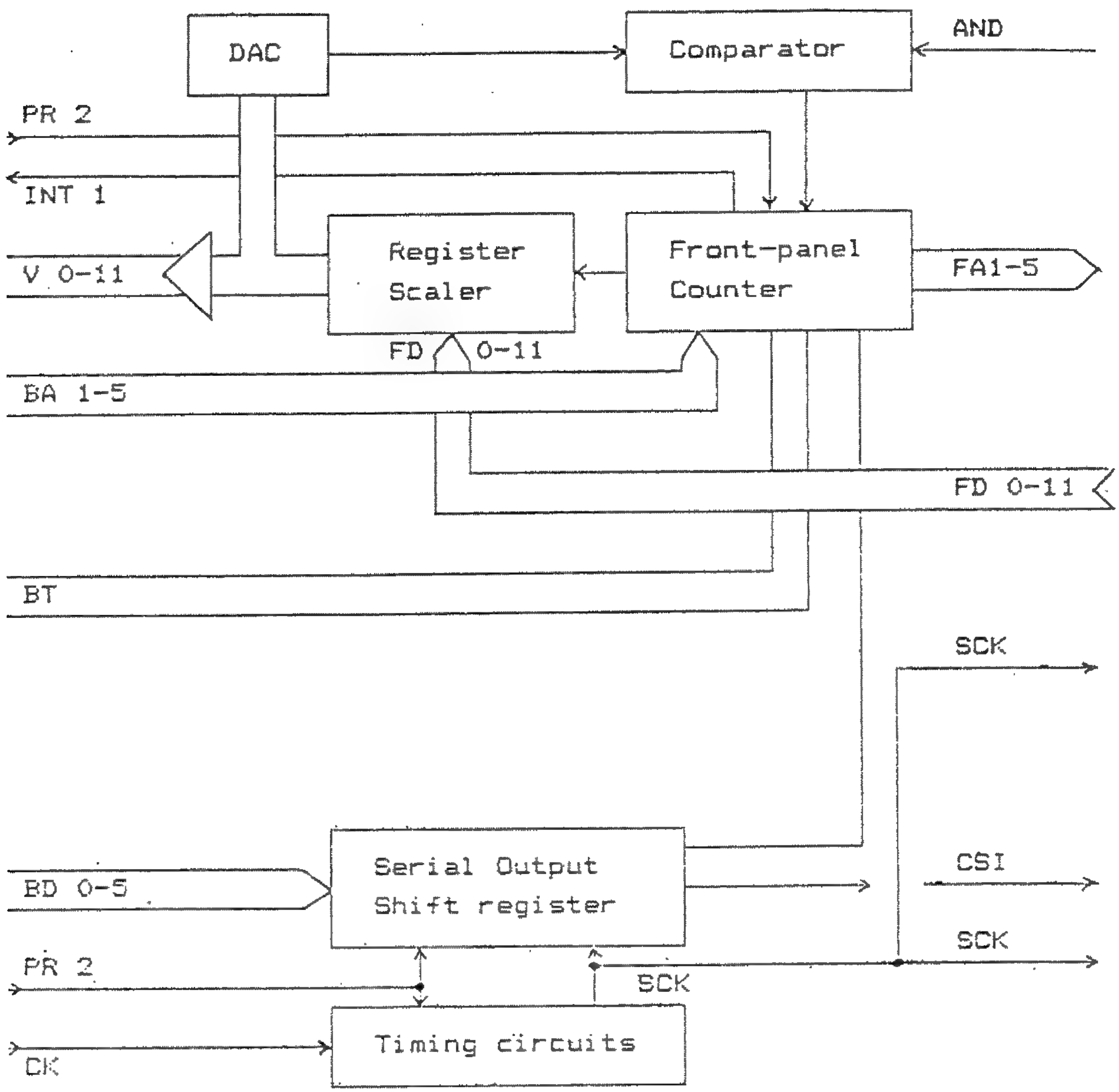
The system clock CK creates the clock SCK at F17. The data are grouped into eight serial bytes. These data are carried on the line CSI <1.1.21.2> to the digital frontend control <1.1.31.2> and trigger control <1.1.32.1>. From there the data go to G17 <1.1.21.1> whence SIN takes them to the front panel LEDs circuits <1.5.4.1>. <1.1.21.2> includes parts of the 9400-5 and 9400-1 boards.



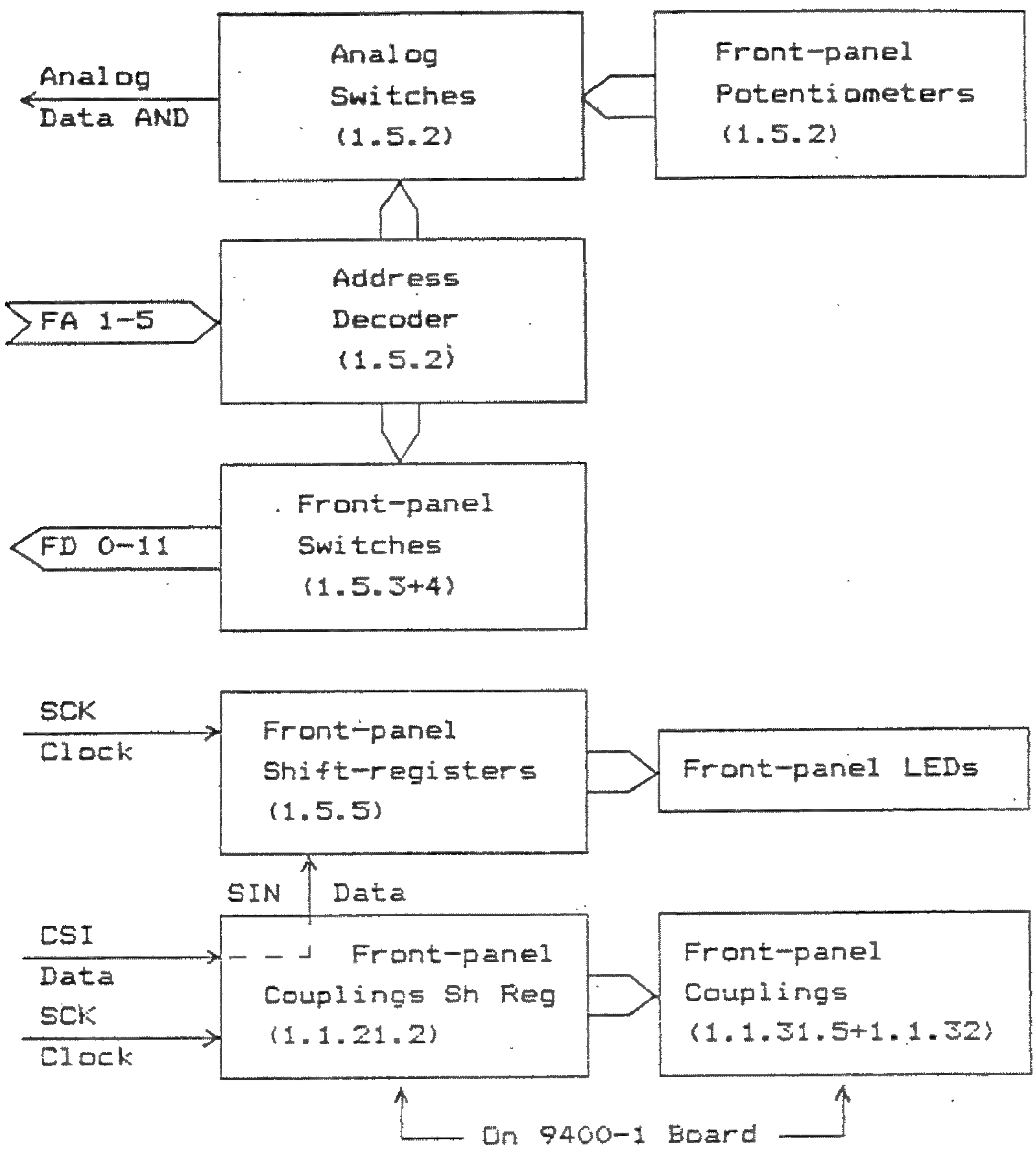
FRONT PANEL CONTROL CIRCUITS

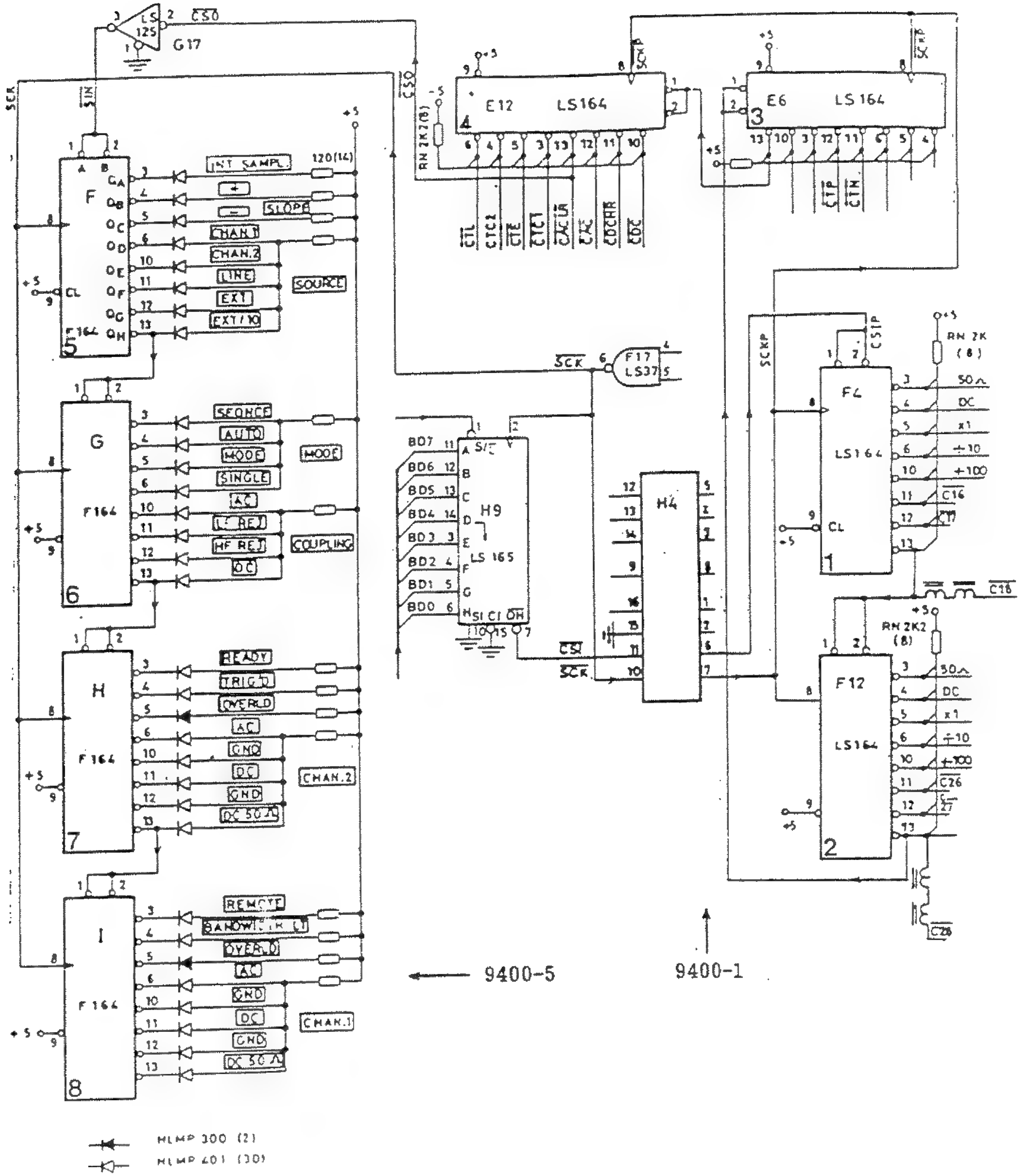
Figure 1.1.21.1

<1.1.21.1A> FRONT-PANEL + INPUT COUPLING LOGIC



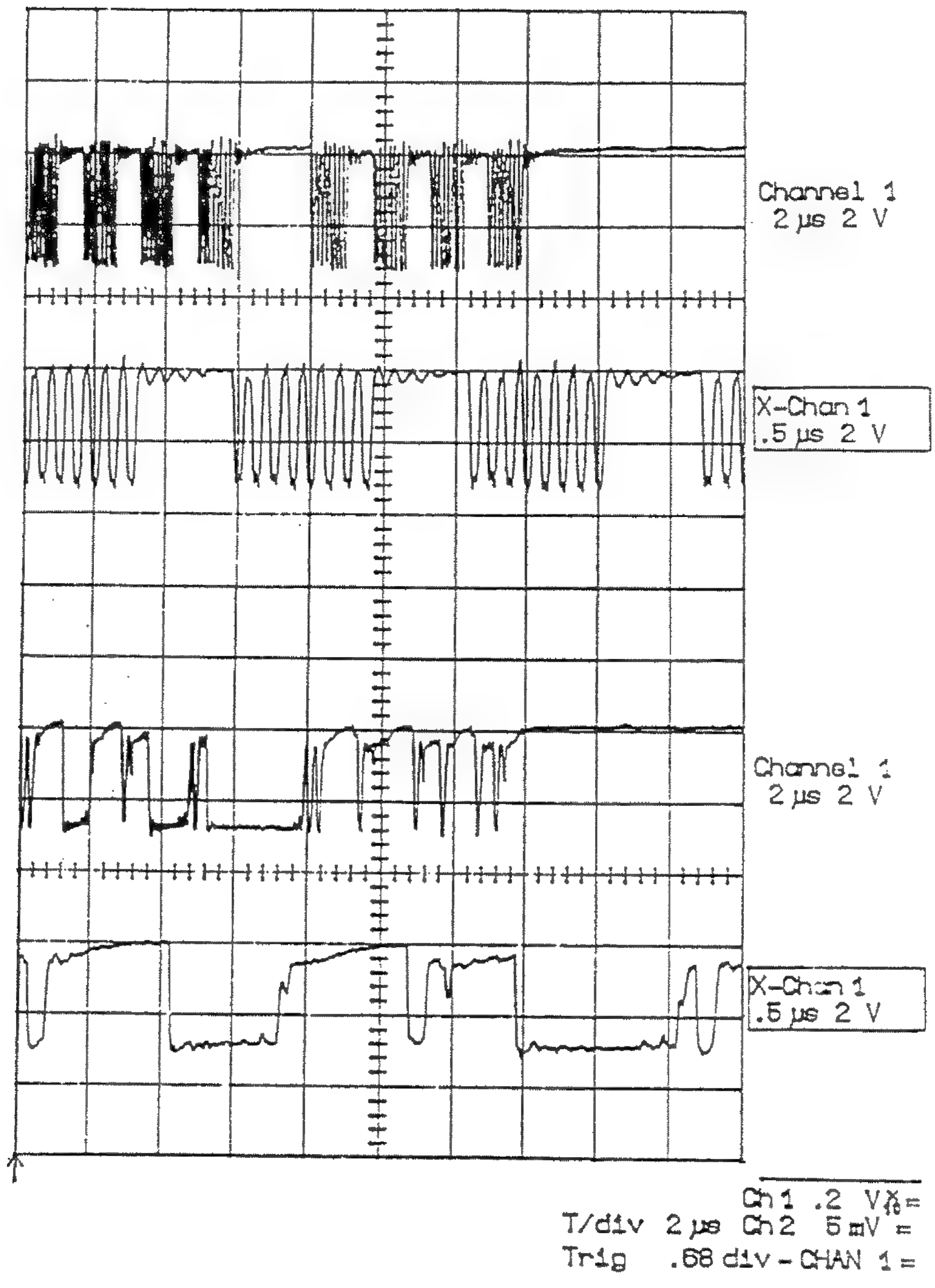
FRONT-PANEL BOARD - BLOCK DIAGRAM





COUPLINGS AND LED CIRCUIT

Figure 1.1.21.2



SERIAL BIT STREAM CST/SIN AND CLOCK SCK

Figure 1.1.21.3

The signals are ordered as follows:

F4 F12 E6 E12 F G H I.

IC Selection signals - First 4 bytes

F4 Chan 1	50 ohm		
<1.1.31.2>	DC		
	X1		
	÷10		
	÷100		
	C16	X8 gain	
	C17	X4	
	C18	X2	
F12 Chan 2	50 ohm		
<1.1.31.2>	DC		
	X1		
	÷0		
	÷100		
	C26	X8 gain	
	C27	X4	
	C28	X2	
E6	PRCAL	probe cal	<1.1.35.1>
<1.1.32.1>	spare		
	BW1	bandwidth	<1.1.31.1>
	BW2	bandwidth	<1.1.31.1>
	EXT/10	ext trig ÷10	<1.1.33.1>
	CTN	neg trig	
	CTP	pos trig	
	spare		
E12	CTC1	internal trigger channel 1	
<1.1.32.1>	CTC2	internal trigger channel 2	
	CTE	external trigger	
	CTL	line trigger	
	CDC	DC coupled trigger	
	CDCHR	DC coupled HF reject	
	CAC	AC coupled trigger	
	CACLR	AC coupled LF reject	

CACLR = CSO, which becomes SIN, driving F, for which see next page.

IC   LED signals - Last 4 bytes

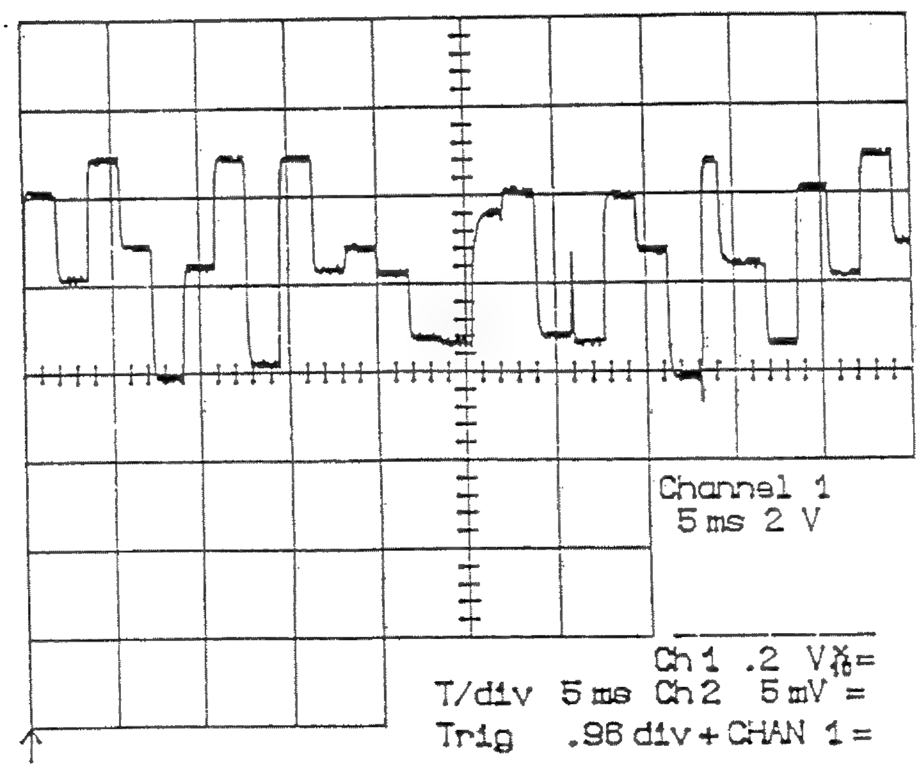
F <1.5.4.1>	INT SAMPL	interleaved sampling
	+	trigger on positive slope
	-	trigger on negative slope
source	CHAN 1	trigger on channel 1
	CHAN 2	trigger on channel 2
	LINE	trigger on power line
	EXT	trigger externally
	EXT/10	externally trigger with ÷10 atten
G	SEQUENCE	sequence of acquisitions
mode	AUTO	auto trigger
	MODE	
	SINGLE	
trig coupling	AC	
	LF REJECT	
	HF REJECT	
	DC	
H	READY	
trig state	TRIG'D	
channel 2	OVERL'D	
coupling	AC	
	GND	
	DC	
	GND	
	DC 50 ohm	
I	REMOTE	DSO control mode
	BANDWIDTH LT	
channel 2	OVERL'D	
coupling	AC	
	GND	
	DC	
	GND	
	DC 50 ohm	

The clock SCK and the data stream CSI/SIN are shown in <1.1.21.3>.

1.1.21.3 Potentiometers

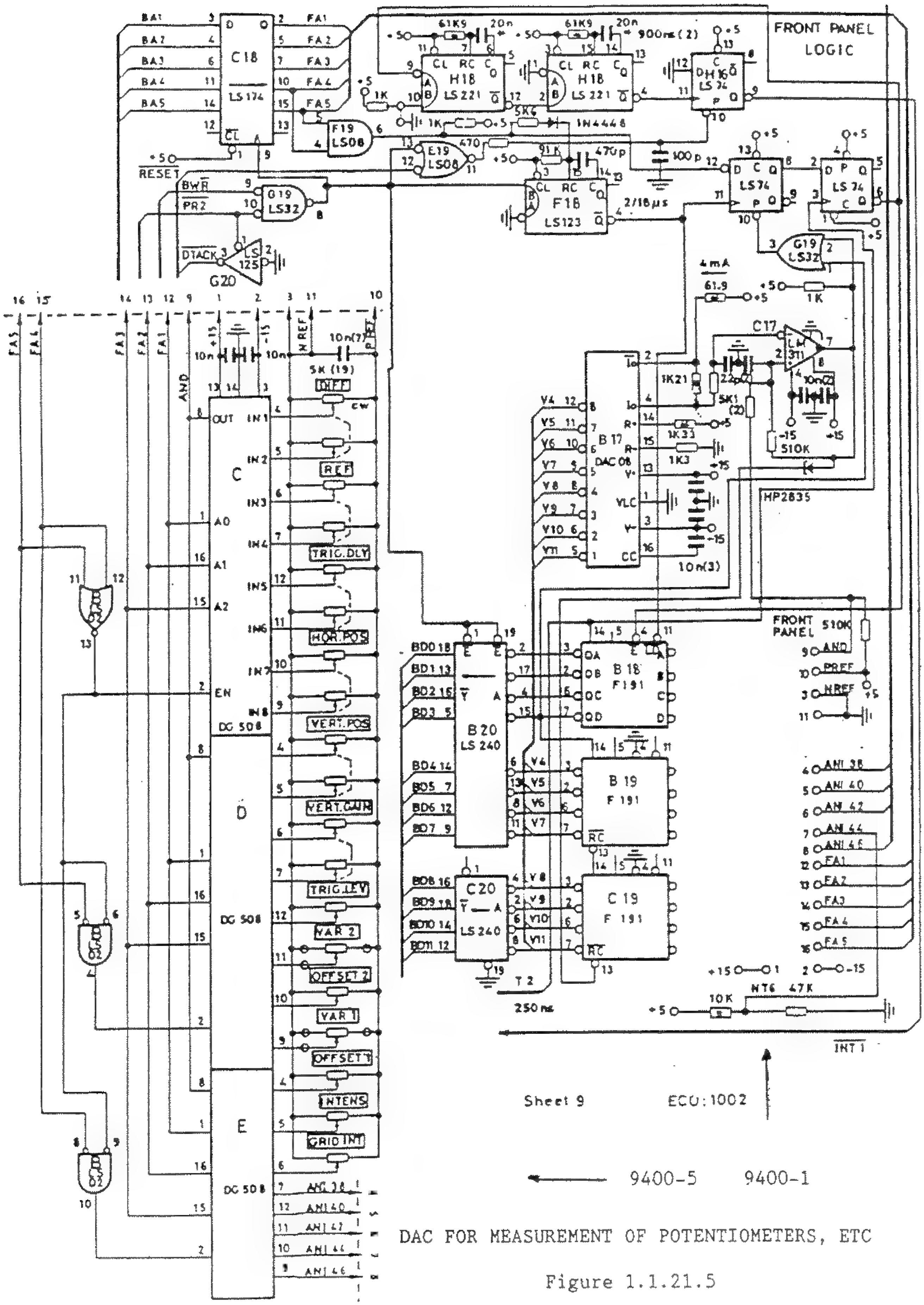
The front panel potentiometers are multiplexed on the front panel board through 8-to-1 line analog switches <1.1.21.5>, which includes parts of the 9400-1 and 9400-5 boards, and <1.5.2.1>, and received through pin 9 of the 9400-1 connector on the serial analog data line AND. The sampling period is about 1.8 ms. The analog signals go to the LM311 comparator C17 <1.1.21.5>, whose other input comes from the DAC08 8 bit DAC, used as a counting ADC, with the binary counters B18 B19 C19 as the source of digital data. When the digital value reaches a certain value, the DAC output equals the AND level, and the comparator will change state, forcing a preset on the 74LS74 flip-flop. The second half of the flip-flop, clocked by the 4 MHz clock T2, will trigger the monostables H18, raising a level 1 interrupt on INT1. The CPU reads the data from the counter via the buffers B20 C20, which are enabled from BWR.PR2 via G19 pin 8. In addition to the front panel potentiometers this circuit measures five analog values from the analog section of the 9400-1 board.

The 24 analog levels in a typical case are shown in <1.1.21.4>.



ANALOG DATA STREAM "AND"

Figure 1.1.21.4



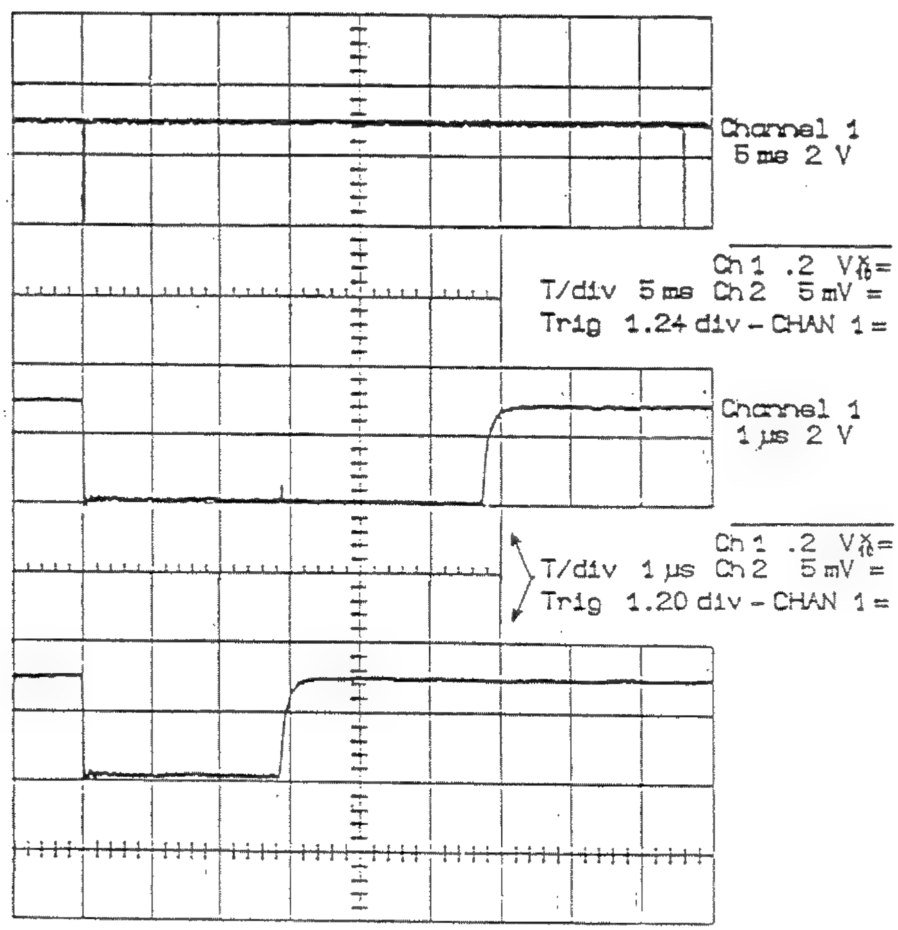
DAC FOR MEASUREMENT OF POTENTIOMETERS, ETC

Figure 1.1.21.5

1.1.21.4 Rotary and Push Button Switches

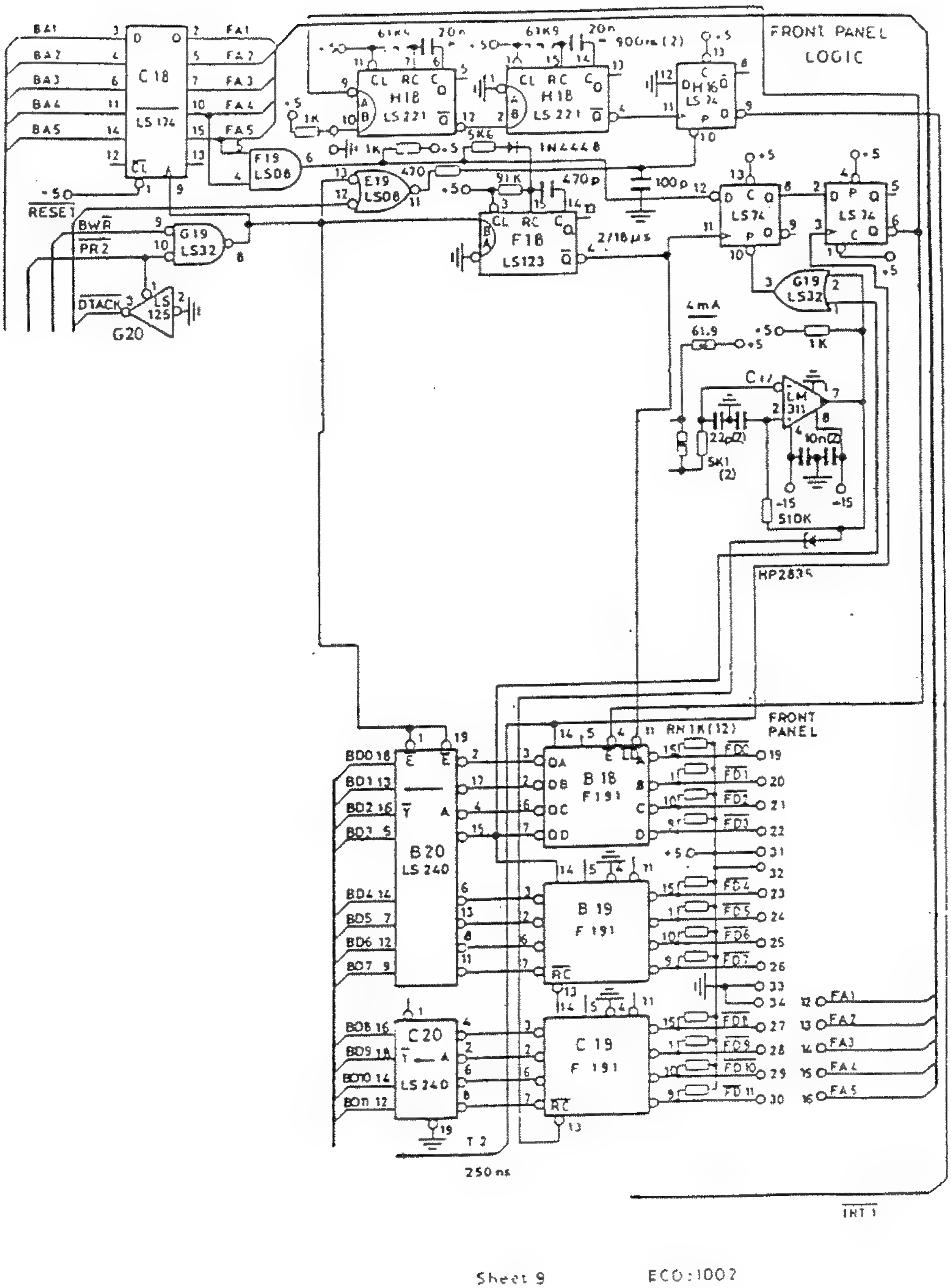
The rotary and push button switches are encoded <1.5.3.1> by the 3-to-8 line decoder on the 9400-5, with a period of about 1.8 ms, and the signals from the switch matrix, which arrive on FD0 - FD11, are loaded by the three binary up/down synchronous counters B18 B19 C19 <1.1.21.7> (which at other times are used to feed the DAC (1.1.21.3)), feeding the octal buffers B20, C20, and thence the bus BD0-11. The load is made by the monostable F18, triggered by BWR.PR2 from G19, and terminated by FA4.FA5 via F19 pin 6 and a resistor diode chain. As an example of the waveforms to be expected, the signals on FD0 are given for two cases <1.1.21.6>, "TRACKING" and "EXPAND A" pressed, top two traces, and "TRACKING" only pressed, bottom trace.

The signals for addressing the switch matrix and the analog switches on the 9400-5 are sent on FA1-5, from C18, a 74LS174 hex flip-flop, latching from BA1-5.



SIGNALS ON FD0 IN A TYPICAL CASE

Figure 1.1.21.6



FRONT PANEL SWITCH CONTROL CIRCUIT

Figure 1.1.21.7

1.1.22 Battery Backup Circuit

The battery backup system powers one 6116 CMOS low power static RAM, with a capacity of 2 K bytes, at the odd addresses, i.e., the low order bytes, of the 68000. The other bytes would read as zero. The backup RAM is addressed at 1D0000 to 1D07FE. Access time is 5 clock cycles at 8 MHz, i.e., 625 ns. This circuit <1.1.22.1> is selected by PR5 (1.1.6) during the power up phase (1.1.3), and at times when new data need to be written to this memory, which stores all the settings of the 9400 DSO which are current at the time of power off.

The array of diodes ensures that the 6116 RAM receives the correct Vcc during normal running, and that while the DSO is off, its Vcc is in the standby range, which draws little current, while retaining the data for over one year at temperatures below 40C, on a fully charged battery. Charging current is drawn from the 9400-9B board (1.9), and is such that about forty hours use of the DSO must elapse before the battery is fully charged.

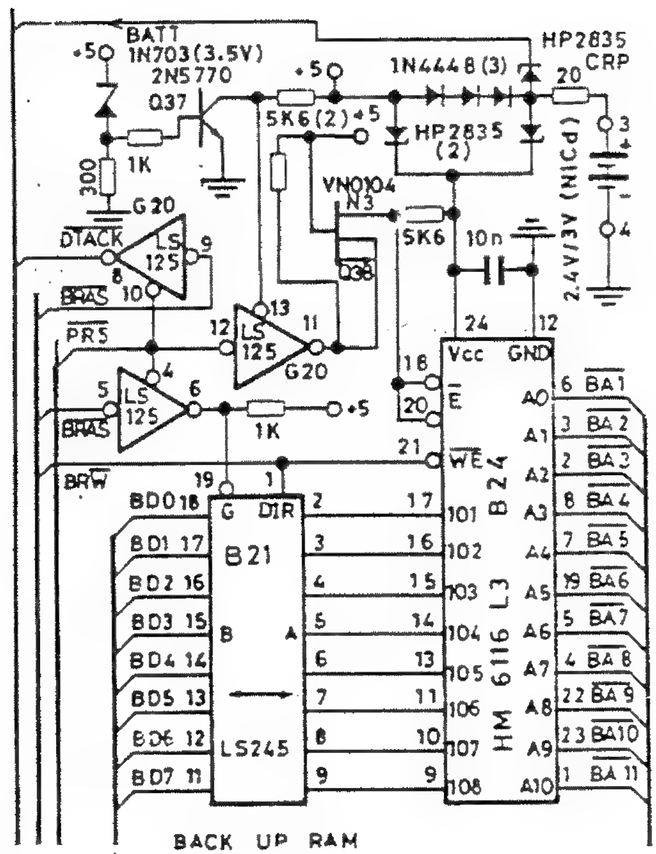
The BATT level goes to a2 of the DMA slot for use by the realtime clock on the 9401-2 (1.1.11) (1.12).

1.1.23 Temperature Measurement

On 9400-1 boards Rev D and after, there is a temperature measurement system. The digital value is read at 1A002C in the front panel area, after the last analog datum. The temperature is transduced by an NTC resistor, NT6; see bottom right of <1.1.21.1>. The precision of the Celsius temperature is 2C or 10%, whichever is the greater. The logarithmic R-T relationship is approximated by the piece-wise linear algorithm:

–	14	<	n	41	101C	>	T	>	84C
–	40	<	n	216	85C	>	T	>	26C
–	215	<	n	241	27C	>	T	>	9C

Where n is the value from the front panel ADC (1.1.21), and T is the centigrade temperature. The algorithm is accurate to better than 1% in this range.



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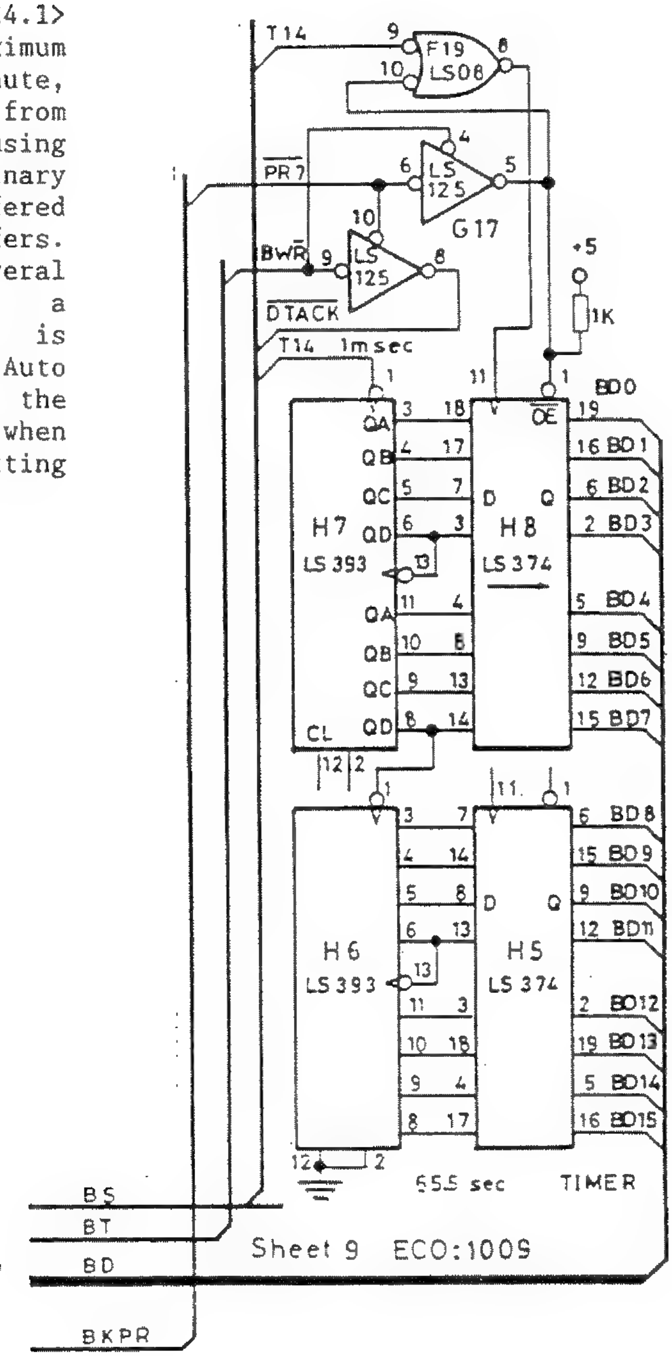
BATTERY BACKUP CIRCUIT

Figure 1.1.22.1

1.1.24 Timer

This circuit <1.1.24.1> provides a timer with a maximum period of about one minute, derived by counting down from T14, the 1.024 ms clock, using two 74LS393 dual 4 bit binary counters, H6 and H7, buffered by two 74LS374 octal buffers. The timer is used for several functions for which a relatively long period is needed, e.g., timing Auto trigger, turning off the display in Normal trigger when no trigger appears, and putting messages on the screen.



TIMER

Figure 1.1.24.1

1.1.25 DMA Slot

The slot nearest the CRT on the right (1.1.11) carries the 9400-6 board in older 9400s, and in newer ones it carries the 9401-2 board. This slot provides direct memory access (DMA), and is foreseen as a means of expanding the versatility of the 9400, as well as a means of using a tester such as the 4928.

The slot addresses the interrupt levels 2, 6 and 7 (1.1.7), assigned as follows:

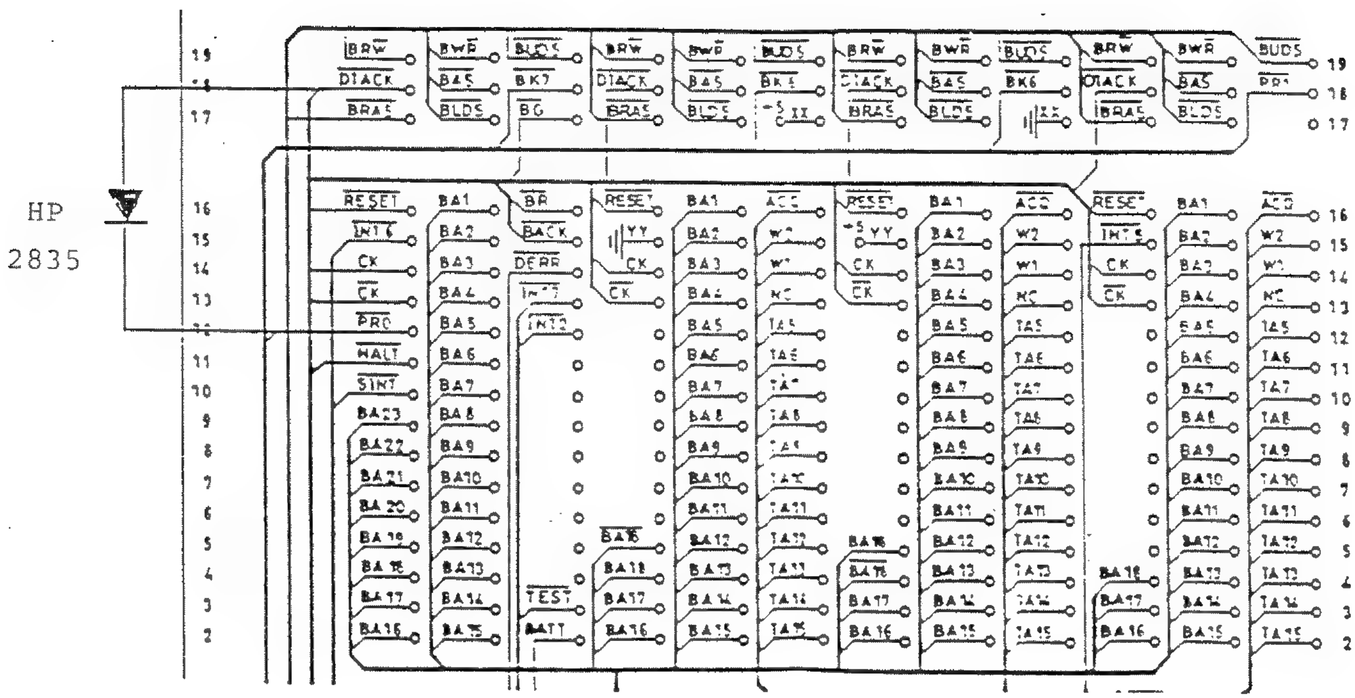
- 2 peripheral device, e.g. floppy disk
- 6 GPIB
- 7 test

From this slot the processor can be controlled by commands such as HALT, RESET, BOOT, DMA dialogue line.

Note

The basic version of the 9400A does not contain a GPIB board. In order to make it work with the present standard software, 2.06STD, a Schottky diode HP2835 is mounted on the DMA connector on the solder side of the 9400-1 board as indicated in Figure 1.1.25.1. It simulates the data acknowledge signal DTACK when the missing board is addressed by PRO, see 1.1.6.

Whenever a GPIB board 9401-2 is mounted for calibration with CALSOFT, this diode has to be removed first. It has to be resoldered once the GPIB board is removed, as otherwise the DSO would not boot up. It must also be pointed out that the basic 9400A locks up if the GPIB port is selected in the plotter setup menu.



Diode returning DTACK signal for the basic 9400A w/o the GPIB board.

Figure 1.1.25.1

Analog Section of 9400-1 Board

Contents

1.1.30 Analog Sections of 9400-1

Introduction

The 9400-1 board carries the main processor and many of the digital control functions of the 9400, as well as a number of analog circuits and mixed functions. They are shown in the block diagram <1.1.30.1>, and include:

- Input coupling selection - each channel
- Front-end amplifier/attenuator hybrid:
  - Each channel, including:
  - Fine gain control
  - Coarse gain control
  - Bandwidth control
  - Trigger bleed off
- Trigger selection of:
  - Source
  - Coupling
- Self-calibration circuits
- Probe calibrator circuits

Where there are two systems, one for each channel, this manual will describe Channel 1; Channel 2 is identical.

Because the analog circuits are controlled by the digital part of the 9400-1 board, it is necessary to look at several sections, particularly (1.1.17) and (1.1.21).

Important Distinction between the 9400 and the 9400A

In order to increase the bandwidth for the Model 9400A, the gain on the 9400-3A ADC board is slightly decreased (ECO 1004 for the 9400-3A board). For this, the feedback resistor between pin 18 and pin 8 of the HSH202 is changed from 1 kΩ to 910 Ω. This loss of gain is compensated for at the HVV output (pin 22) by replacing the 43 Ω resistor to 39 Ω (ECO 1016 for the 9400-1 main board). The resistor R at the HVV output defines the gain between the front-end and the ADC as:

$$\text{gain between front-end and ADC} = \frac{R}{R + 50}$$

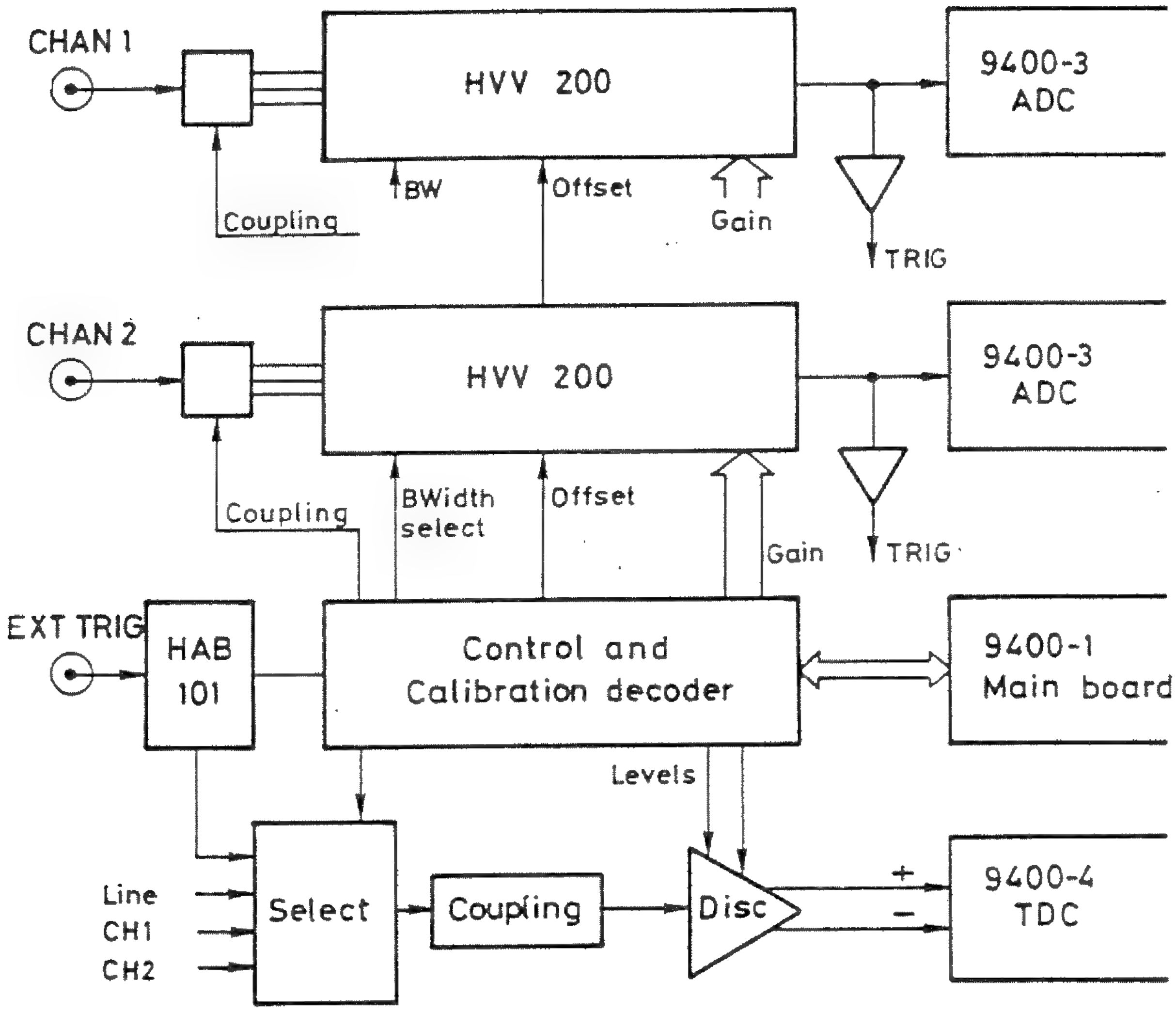
In addition, HVV at ECO 1003 has to be used on 9400-1 at ECO 1016. Therefore, be careful not to mix these ECOs between the 9400, the old with the 9400-3 and the new with the 9400-3, and the 9400A. The possible configurations are listed below:

9400 with old 9400-3	9400-1 at ECO 1015 with 43 Ω at HVV output.
9400 with new 9400-3A	9400-1 at ECO 1016 with 39 Ω at HVV output HVV at ECO 1003. 9400-3A at ECO 1004 with 910 Ω S/H feedback. OR 9400-1 at ECO 1015 with 43 Ω at HVV output 9400-3A at ECO 1003 with 1 kΩ S/H feedback
9400A	9400-1 at ECO 1016 with 39 Ω at HVV output HVV at ECO 1003 9400-3A at ECO 1004 with 910 Ω S/H feedback

If resistors have to be changed to prepare a board for one of the four configurations above, make sure that:

- the overall gain (front-end + ADC) is within limits. Check this by using the internal test "gain curves" for all sensitivities and BW ON and OFF. See the internal tests, Section 3.1.7. The overall gain for all sensitivities can be readjusted by changing the resistor at the HVV output.

- the HF overshoot is within limits, see adjustment 2.4.3.4. If the feedback resistor on the ADC board is changed, the capacitor parallel to it MUST be readjusted.



ANALOG BLOCK DIAGRAM

Figure 1.1.30.1

1.1.31 Frontends

1.1.31.1 Introduction

The outline for one channel is shown in <1.1.31.1>. Bracketed data refer to Channel 2. The input stages are based on the LeCroy hybrid HVV200, which contains accurate high frequency amplifiers with variable gain, and circuits to switch gain ranges and bandwidth.

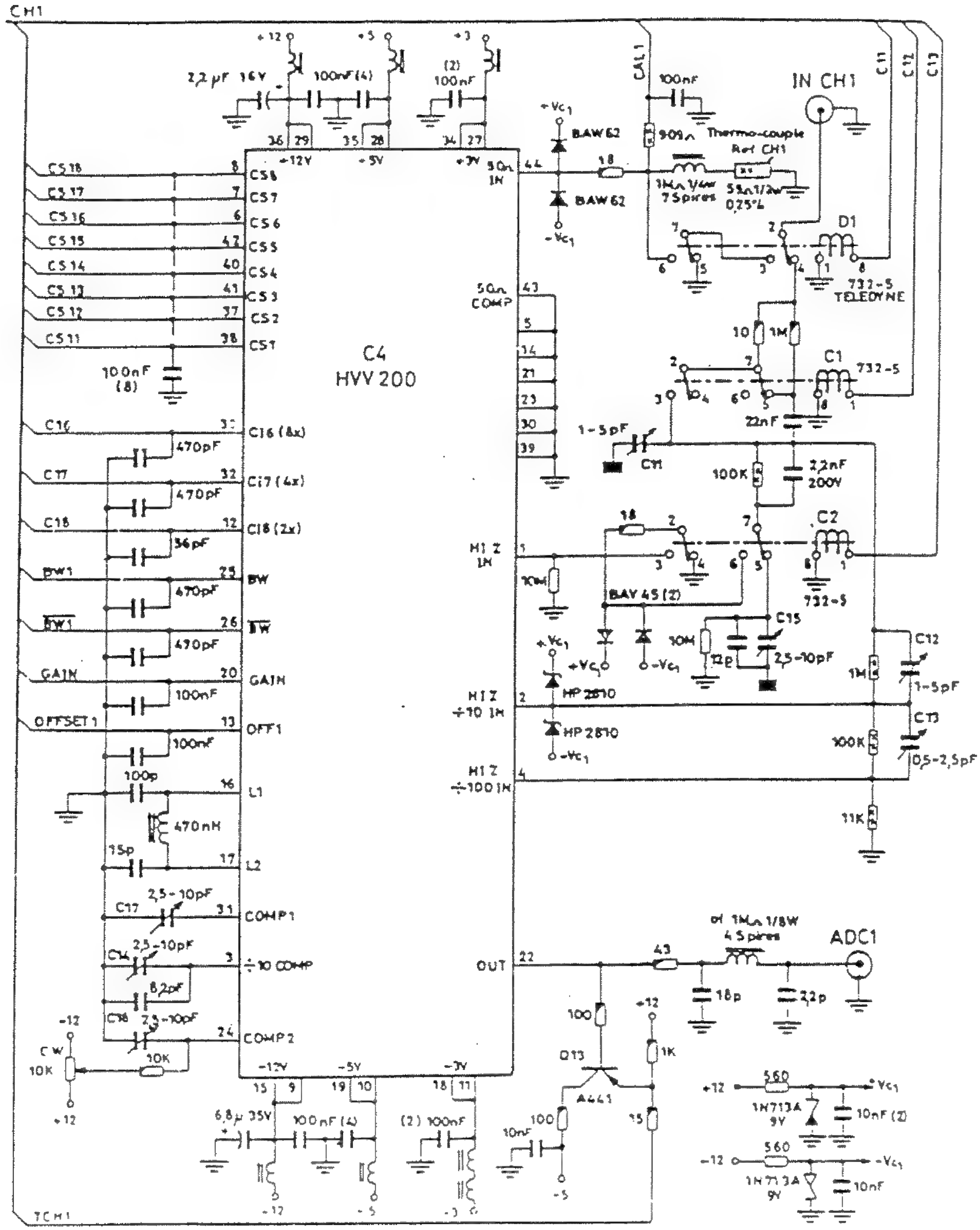
1.1.31.2 Input Coupling and Protection

The signal from the input socket is switchable by relay from the 50 ohm to the high-Z input of the HVV200. The 50 ohm input is also connected to CAL1 (CAL2), for the purpose of calibration, which takes place whenever a channel control or bandwidth control is changed. A signal presented by CAL1 (CAL2) is digitized by the channel, and the resulting information enables the processor to adjust the channel until the result is correct.

The digital control lines are shown in <1.1.31.2>, while the analog controls are in <1.1.31.3>.

AC/DC selection is by relay. Diodes type HP2810 and BAV45 provide protection of the hybrid against overload on the high impedance input. The 50 ohm resistors and the hybrid are protected by thermocouples on the resistors, which feed the overload detection circuits (1.1.36). In addition, a series 18 ohm resistor is added, followed by two clamping diodes type BAW62, to protect the 50 ohm input of the hybrid.

The HVV200 uses considerable power, and requires a substantial heat sink.



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FRONTEND HYBRIDS HVV200

Figure 1.1.31.1

1.1.31.3 HVV200 Hybrid

The HVV200 hybrid contains circuits to control:

- Stepped attenuation
- Continuously variable gain
- Continuously variable offset
- Bandwidth limit

The internal functions of this hybrid will not be described in this manual.

The control lines are <1.1.31.1>:

CS11-18	(21-28)	CS1-8	digital	<1.1.31.2>
OFF1	(OFF2)	offset control	analog	<1.1.31.3>
GAIN1	(GAIN2)	gain control	analog	<1.1.31.3>
BW1	(BW2)	bandwidth control	digital	<1.1.32.1>
C16-18	(26-28)	stepped attenuate	digital	<1.1.31.2>

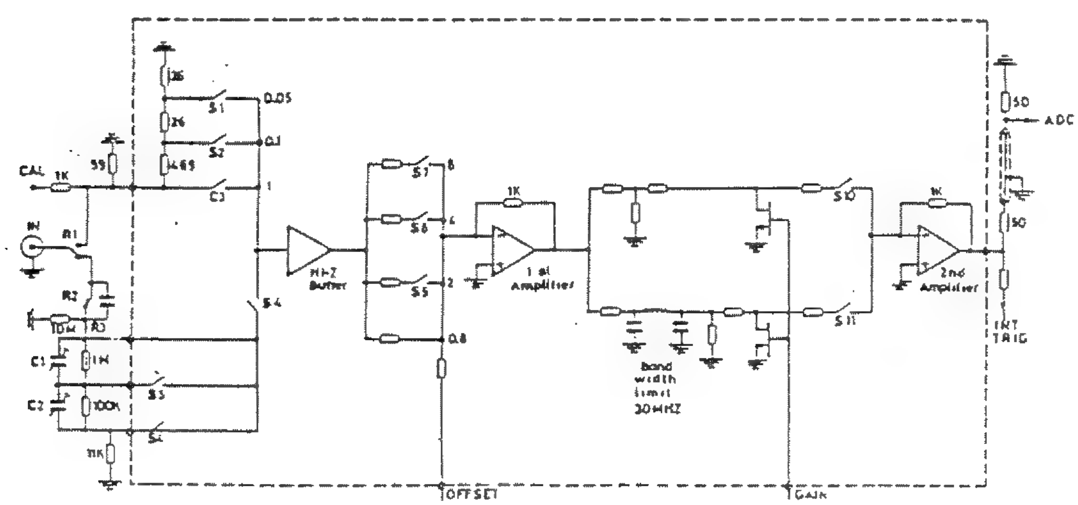
The output of the HVV200 goes to an SMB socket on the 9400-1; a coaxial cable takes the signal from there to the input of the 9400-3 ADC board (1.3). The output also drives an emitter follower which feeds the trigger line TCH1 (TCH2) for the internal trigger function.

The functions of the HVV200 are shown in <1.1.31.1A>.

1.1.31.4 Control Lines

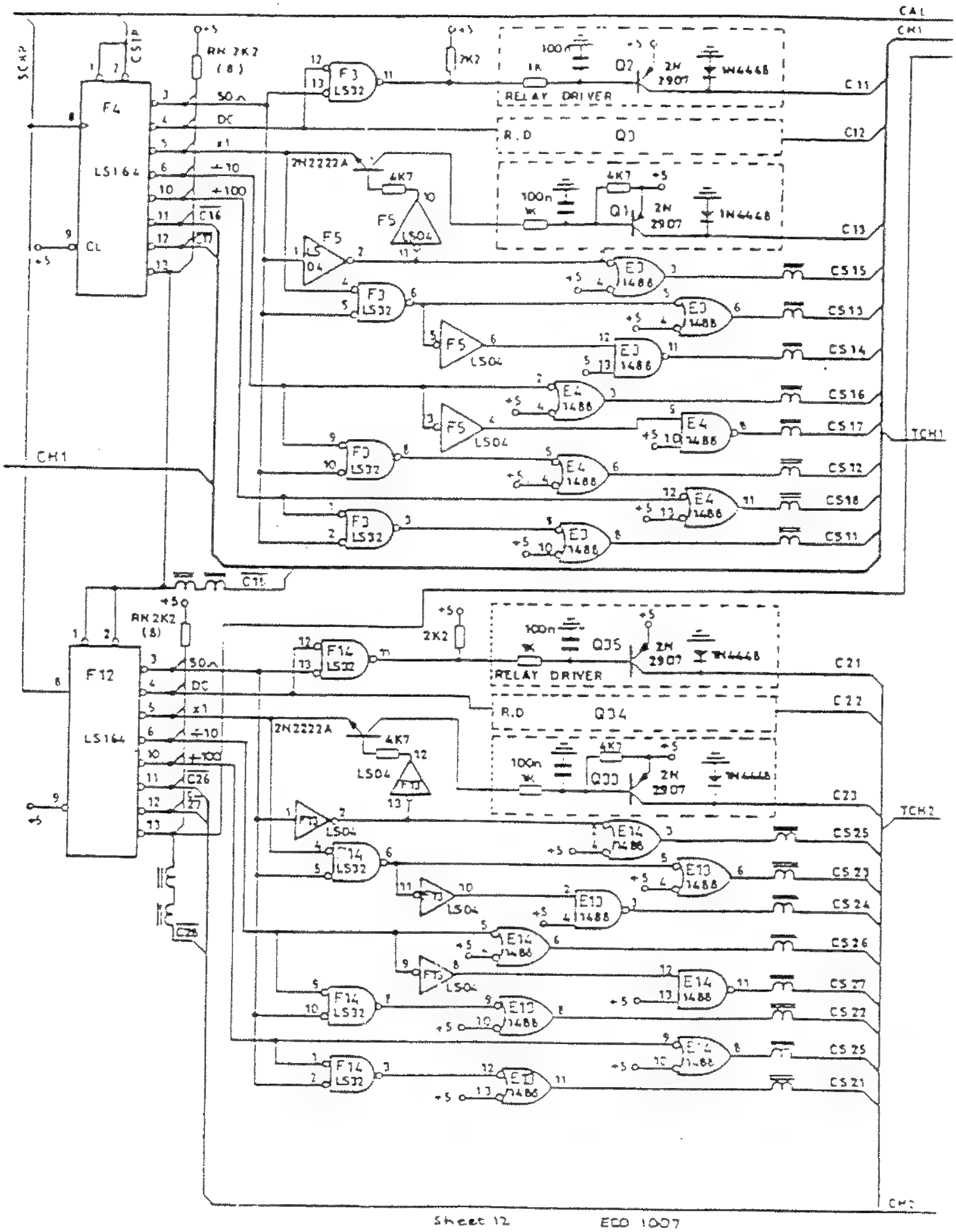
The various digital control lines are buffered by TTL logic, except for the relay drivers <1.1.31.2>.

For derivation and use of the SCK and CSI signals see (1.1.21).



HVV200 FUNCTIONS

Figure 1.1.31.1A



DIGITAL FRONTEND CONTROL

Figure 1.1.31.2

1.1.31.5 Digital Frontend Control

The control lines for the frontends are derived from CSIP <1.1.31.3> (1.1.21.1)(1.1.21.2) (which include complete schematics for the controller, and typical waveforms), via the serial-to-parallel shift registers F4 and F12, clocked by SCKP (same references). The lines from F4 and F12 are decoded into the C11-13, CS11-18, C21-23, CS21-29. <1.1.31.2>.

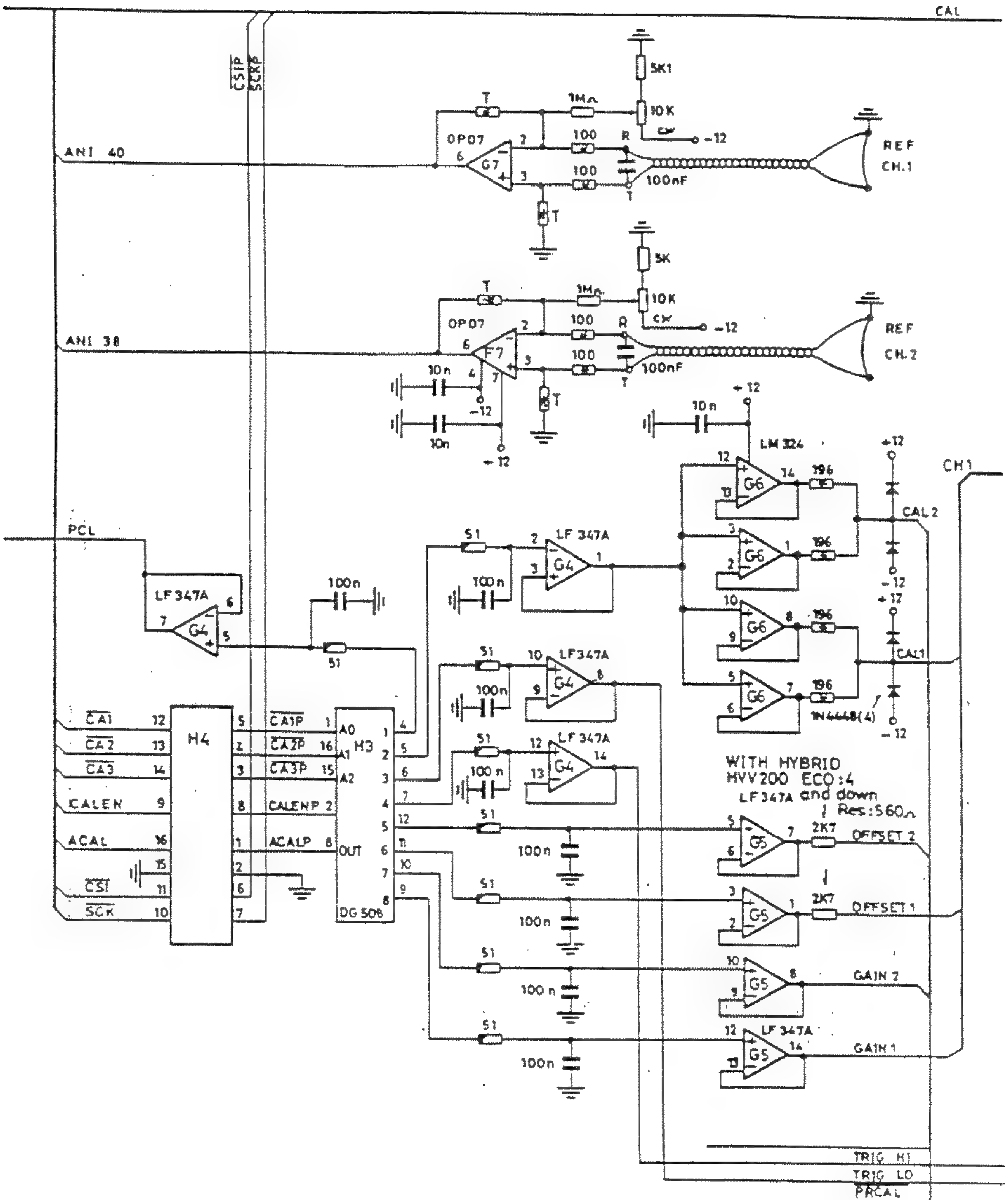
C11	DC	AND	50 ohm
C12	DC		
C13	X1	AND	NOT 50 ohm
CS11	÷100	AND	50 ohm
CS12	÷10	AND	50 ohm
CS13	X1	AND	50 ohm
CS14	50 ohm	AND	NOT CS13
CS15		NOT	50 ohm
CS16	÷10		
CS17		NOT	SC16
CS18	÷100		

1.1.31.6 Analog Frontend Control

These circuits <1.1.31.3>, control the analog functions of the HVV200 hybrids:

-	GAIN1	Channel 1 gain control
-	GAIN2	Channel 2 gain control
-	OFFSET1	Channel 1 offset
-	OFFSET2	Channel 2 offset
-	CAL1	Channel 1 calibration signal
-	CAL2	Channel 2 calibration signal
-	TRIGHI	Upper trigger threshold (1.1.32)
-	TRIGLO	Lower trigger threshold (1.1.32)

These signals are demultiplexed by the DG508 8-way analog switch H3, addressed by CA1P-CA3P, derived from CA1-3, and enabled by CALEN (1.1.17). Note that PCL goes to the probe calibrator (1.1.35). The analog signals are buffered by op-amps G5 and G6, the calibration lines needing pairs to get enough drive, with protection against damage from channel input signal overdrive. The signals ACAL and CALEN are shown in <1.1.17.2>.



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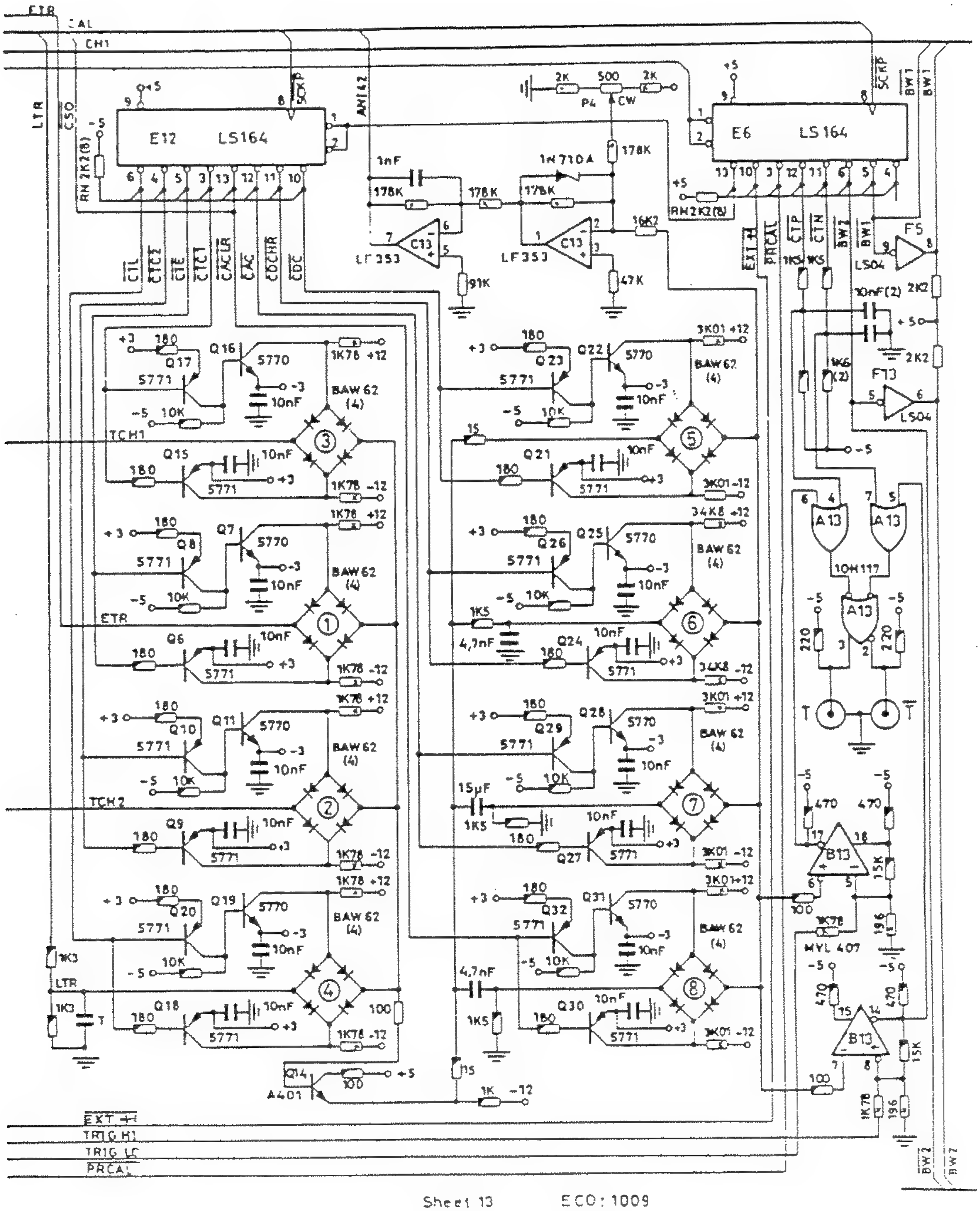
ANALOG FRONTEND CONTROL

Figure 1.1.31.3



TRIGGER CONTROL CIRCUITS

Figure 1.1.32.1

1.1.32 Trigger Circuits

The 9400 DSO provides for internal trigger (1.1.31.3), line trigger (1.1.8), and external trigger at two sensitivities (1.1.33). Since it is extremely important, in view of the need to sample at very high rates, especially the effective rate with random interleaved sampling (RIS), to achieve accurate timing, the trigger modes must be switched with switches which cause little delay to the signal.

These are provided by diode bridges <1.1.32.1>. Their inputs are on the left, and their outputs are on the right, with the diodes in the conducting state for an "on" switch. The switches are driven from the parallel output shift register E12, a 74LS164. The outputs drive the transistor triples such as Q15-17, so that when a shift register output is low, Q15-16 conduct and cut off the diodes.

The four trigger inputs are:

- LTR <1.1.8.1> 50/60 Hz square wave
- TCH1 <1.1.31.1> int trig from HVV200 output
- TCH2 <1.1.31.1> int trig from HVV200 output
- ETR <1.1.33.1> ext trigger front panel input

The outputs from the four switches on the left of <1.1.32.1> are in parallel, and feed the four coupling selectors on the right, again controlled by E12. The options are:

- CACLR AC coupled, low frequency reject
- CAC AC coupled
- CDCHR DC coupled, high frequency reject
- DC DC coupled

The outputs from these second switches go to the two comparators of the LeCroy MVL407, and thence to the ECL output stage A13, whose complementary outputs go to two SMB connectors which feed the timebase board, 9400-4 (1.4.8).

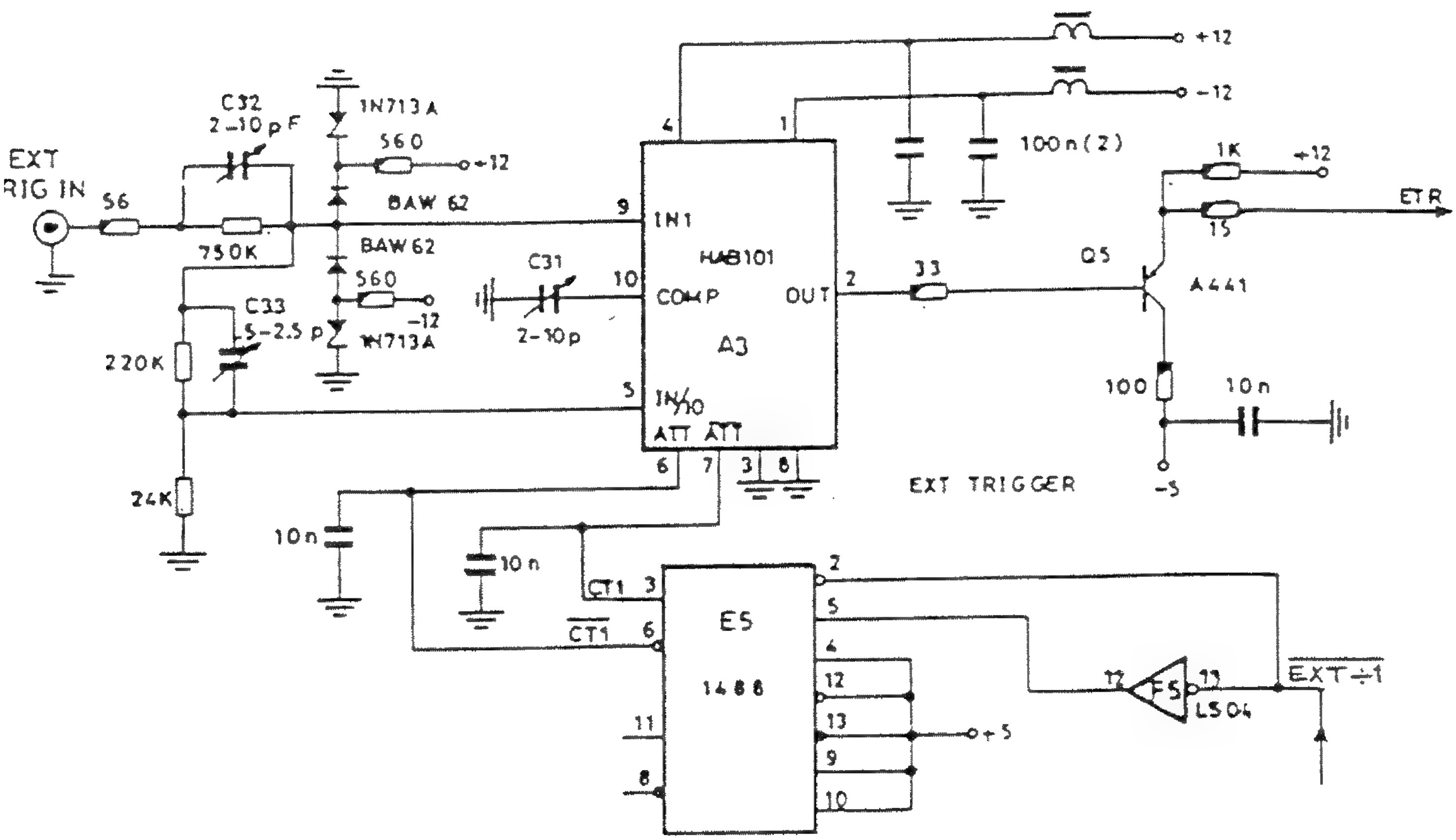
The MVL407 is controlled by the levels TRIGHI and TRIGLO, which are derived from G4, <1.1.31.3>.

The controller for the shift registers E6, E12 is described in (1.1.21.1)(1.1.21.2).

1.1.33 External Trigger

The external trigger <1.1.33.1> feeds A3, a LeCroy hybrid which contains a switchable attenuator, controlled by the ATT lines, pins 6 and 7, and a comparator, feeding Q5, from which the ETR line goes to the trigger switches <1.1.32.1>. The attenuation is switched by E5, controlled by E6, the second parallel shift register in <1.1.32.1>.

Compensation and diode protection are provided at the external trigger input.



EXTERNAL TRIGGER CIRCUIT

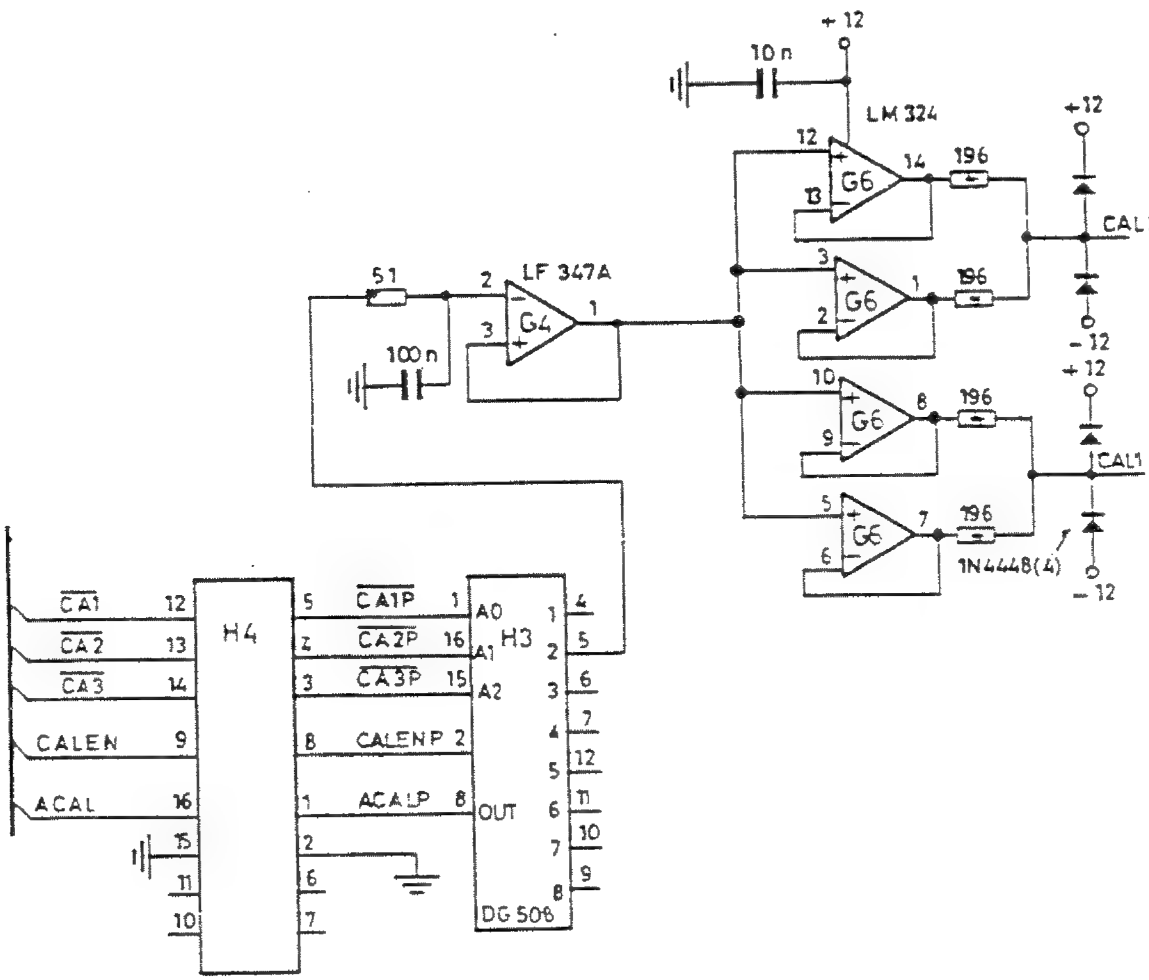
Figure 1.1.33.1

1.1.34 Calibration System

The 9400 DSO employs a system of auto-calibration for the gain of each channel, so that the sensitivity of each channel is always known, even when the fine gain control is not at its X1 position. The calibration takes place at power up, and is repeated every time any front panel control is adjusted.

This is accomplished by means of the CAL1 and CAL2 levels applied at the 50 ohm inputs of the frontends <1.1.31.1> and generated from the analog demultiplexer <1.1.31.3>, from the analog data stream ACAL <1.1.17.1>. The digitization of CAL1 and CAL2 provides the processor with information on the overall gain of the channels, from the input to the digital bus. Clearly the system relies on the accuracy of the input resistors and of the DAC and the transmisson of ACAL to the frontend.

The system is summarized in <1.1.34.1>.



CALIBRATION SYSTEM

Figure 1.1.34.1

1.1.35 Probe Calibrator

This circuit <1.1.35.1> drives the calibrator output on the front panel, providing a square wave or a DC level of accurately known amplitude. The circuit is based on a CA3046 transistor array, with the pair used in long tail connection. The output transistor has feedback to the base to define the gain, and to enable frequency compensation to be included.

The slider of the preset potentiometer is connected to ANI46, one of the analog input lines which are fed back on the front panel board (1.5.2) via an analog switch to the 9400-1 (1.1.21.3) for measurement.

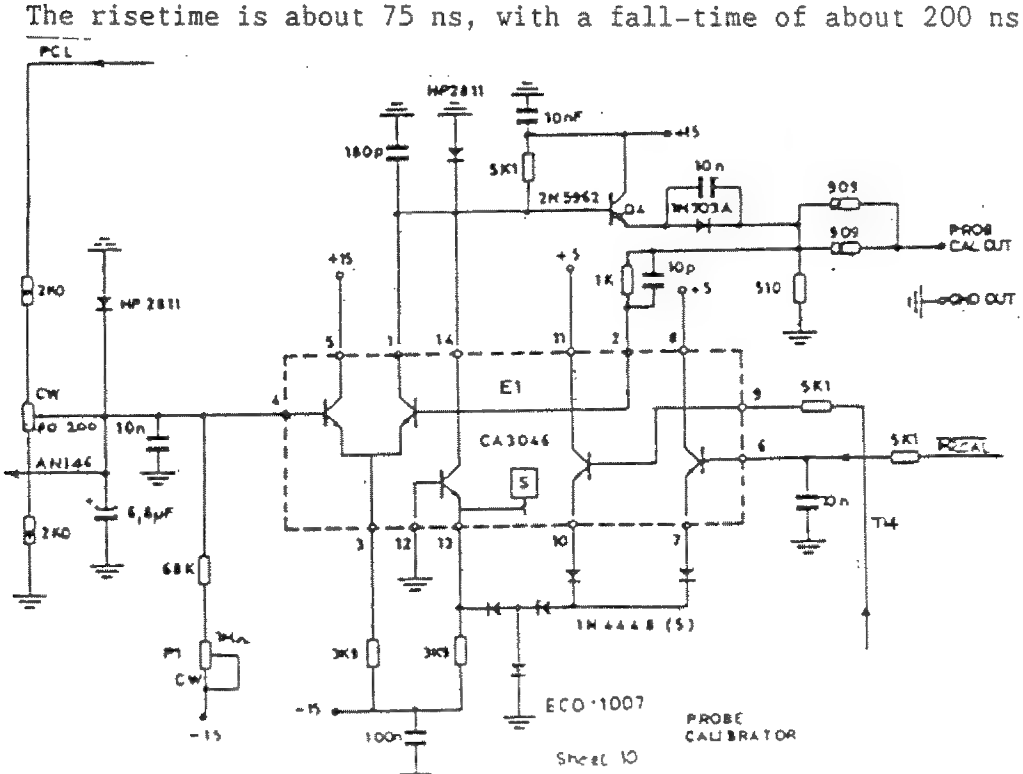
The lines PRCAL and T14 <1.1.15.1> can be used to control the CAL output. PRCAL <1.1.32.1> E6 is high for a square wave output, and low for DC. T14 is a square wave of period 1.024 ms, derived from the 8 MHz clock (1.1.15). PCL is derived from the analog controller G4 <1.1.31.3> <1.1.17.1>.

The amplitudes available are:

- into 1 Mohm	0 to 5 V	DC or square wave
- into 50 ohm	0 to 0.5 V	DC or square wave

The DC levels are available only under control of DSO tester.

The risetime is about 75 ns, with a fall-time of about 200 ns.

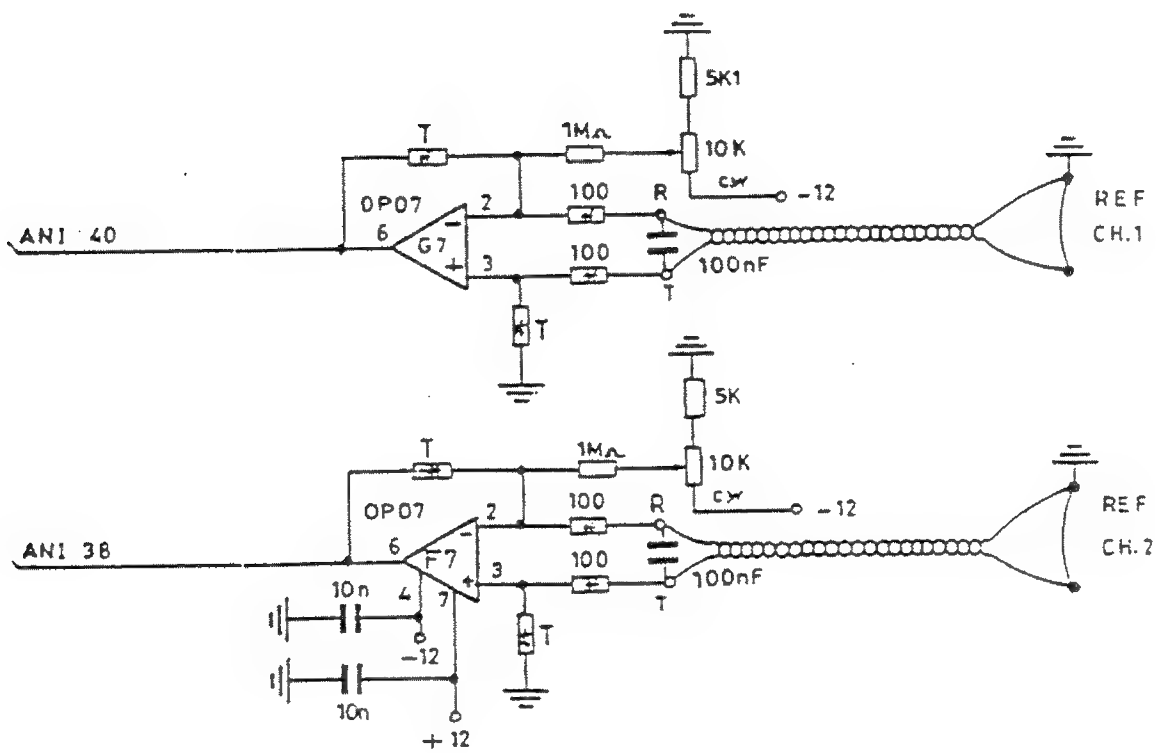


PROBE CALIBRATOR

Figure 1.1.35

1.1.36 Overload Protection 50 Ohm

In order to avoid overheating of the 50 ohm input resistors, which could permanently alter their value, they are each provided with a thermocouple, connected to an operational amplifier <1.1.36.1>, which sends a DC level via ANI40 or ANI38 to the analog switch on the front panel board <1.5.2.1> E, which delivers the levels the 9400-1 board (1.1.21.3) for assessment. Each amplifier has a preset offset control. T are resistors selected to set the gain.

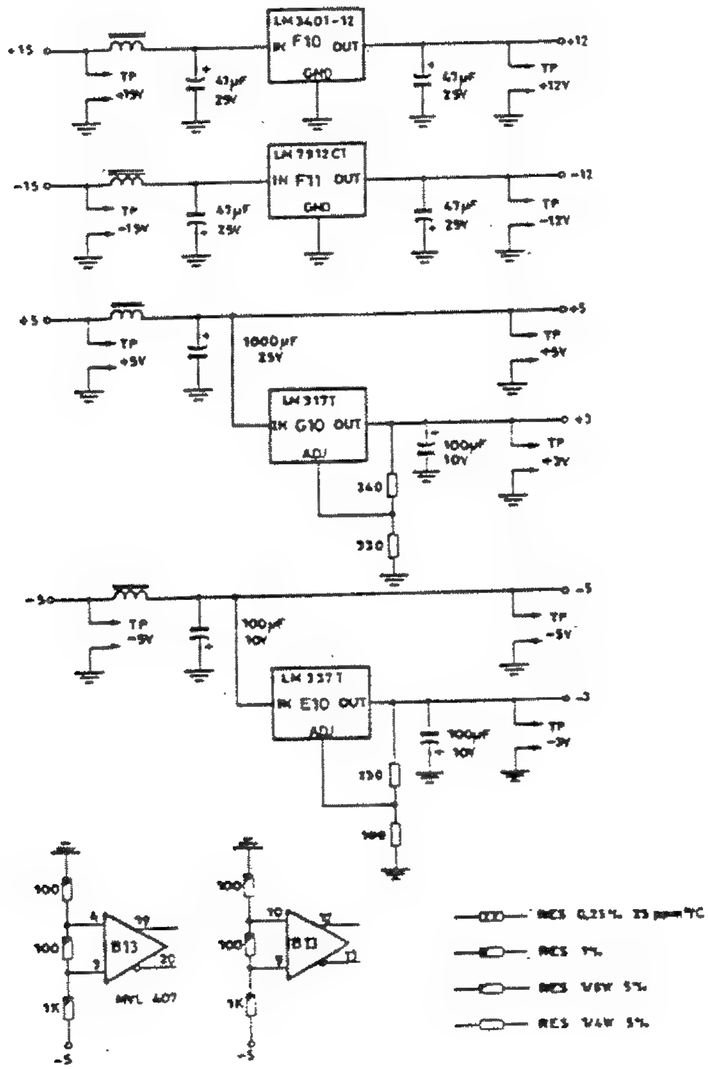


50 OHM OVERLOAD PROTECTION

Figure 1.1.36.1

1.1.37 Power Supplies

The precision levels needed by the analog circuits are provided by four regulators <1.1.37.1>, situated near the center of the 9400-1 board. These regulators also provide low frequency noise rejection for the supplies to critical circuits. The two 12 V regulators, F10 and F11, must be matched for voltage output.



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9400-1 POWER SUPPLIES

Figure 1.1.37.1

1.2 9400-2 Display Board

Table of Contents

1.2 9400-2 Display Board

1.2.1 Introduction

This board controls the CRT display, taking digital data from the 9400-1 bus, converting them to analog form, and producing signals to control the position and brightness of the spot on the screen. (The spot position will be referred to in this section even for the case where the beam current is turned off, to avoid circumlocution).

The image consists of a number of straight lines - vectors - making up one scan, or page, of the display, the pages being repeated at the frequency of the public power supply, 50 Hz or 60 Hz, which means that any stray magnetic fields at that frequency will not cause the image to wobble - only a steady deflection will be seen, which is much less objectionable, especially as the grid and waveforms will be distorted equally. The vectors are all drawn at about the same speed, so that a constant trace intensity is simply obtained.

Each page of the display consists of a number of vectors, some of which are visible, while others, used when non-contiguous parts of the image are to be drawn, are invisible. The vectors can be further classified into vertical, horizontal, and sloping lines, each requiring different data from the 9400-1.

The analog position signals are generated by X and Y DACs, as are the velocity data, but the velocities are further processed by two EPROMs, which give the components of velocity needed to make sloping lines. The resultant speed of the spot on the screen is always the same, which simplifies the brightness control, and also means that for each component, the maximum rate is the same, simplifying amplifier design.

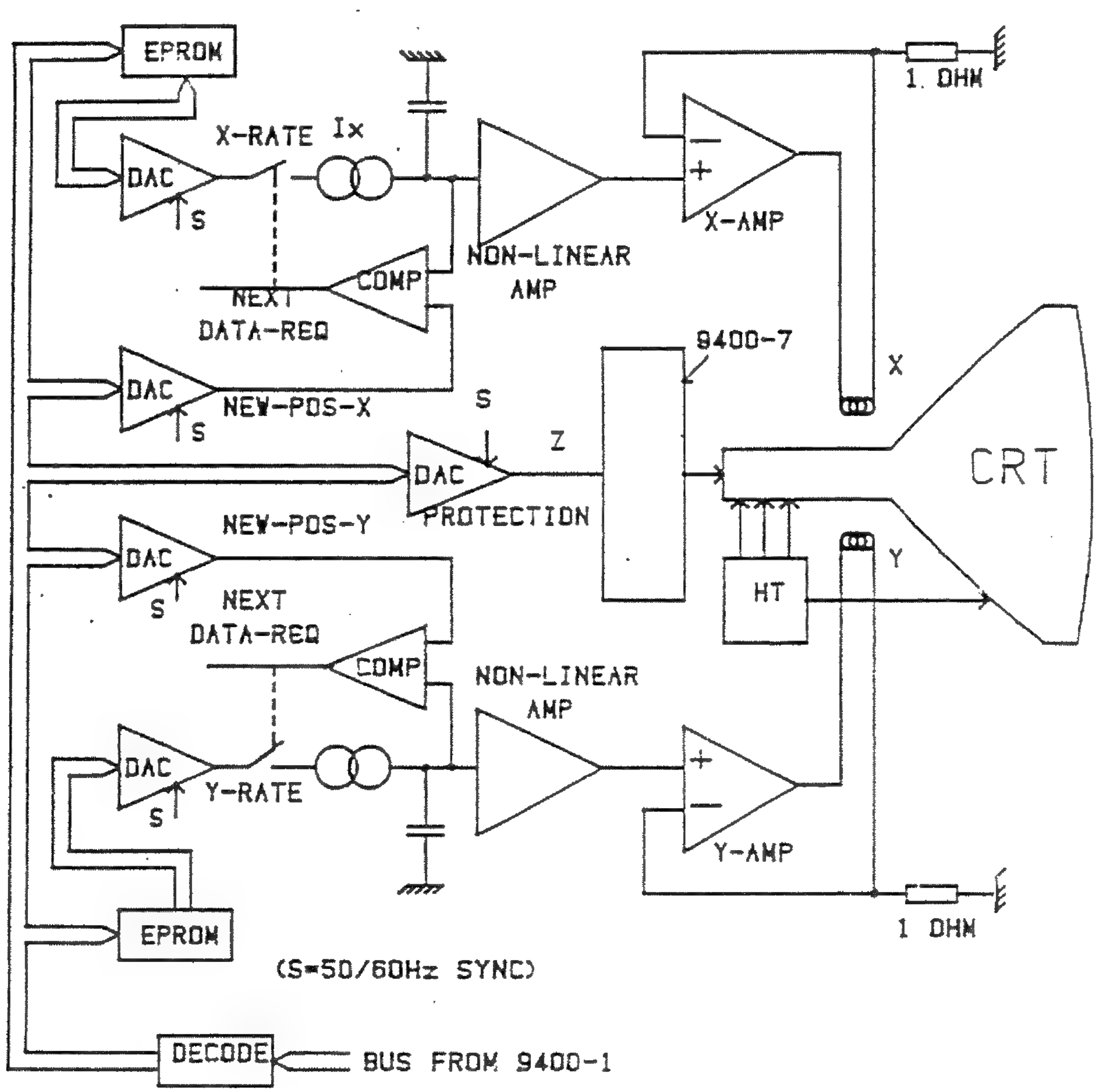
The CRT is magnetically deflected, which enables a large screen to be used, with a high final anode potential giving a sharp, bright trace; since the scan is not in real time, the image forming system can be optimized entirely for image quality with no compromises of the kind which arise with high writing speeds. The resolution of the display is 10 bits, 1024 points, on each orthogonal axis, the center, corresponding to zero yoke current, being at (512,512). The deflection processors include corrections for the non-linearity of the current position relationship.

The amplifiers must be capable of handling considerable power, because the load is inductive, which means that the theoretical class B efficiency with resistive load cannot be approached.

If an unsuitably long time base period is chosen, there will be so many waveform cycles to be drawn that the page may take more than one, or even more than two or three line cycles, in which case the scanning frequency drops to the next possible sub harmonic of the line frequency, resulting in unpleasant flickering. With any realistic settings this effect will not occur.

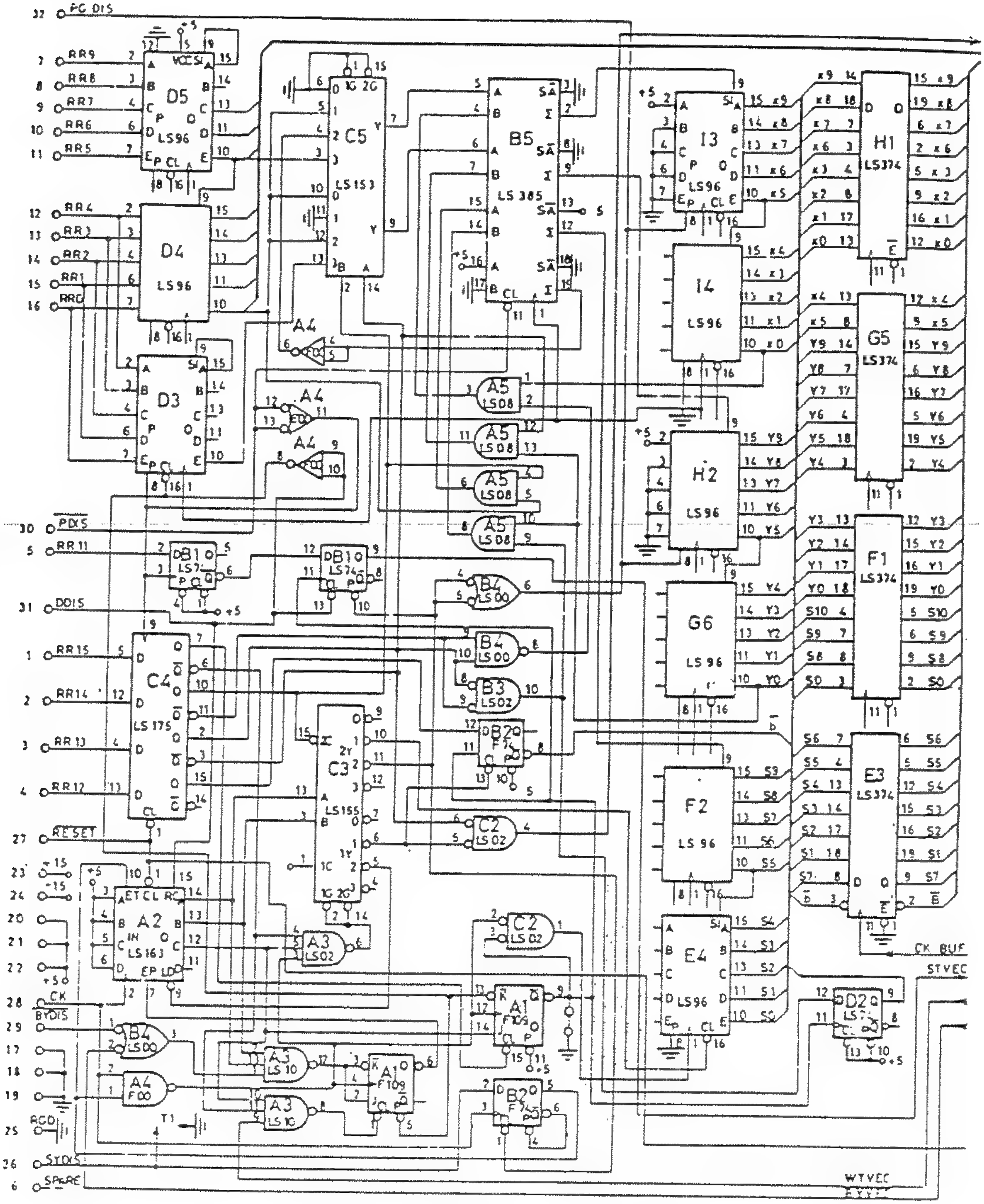
As well as controlling the screen image, the 9400-2 generates the DC levels needed by the CRT for accelerating and focusing the electron beam, as well as some of the protection circuitry which prevents the phosphor from being damaged in a variety of circumstances, some which occur during normal running of the DSO, and others which would arise as a result of a fault.

The main functions of the 9400-2 board are shown in the block diagram <1.2.1.1>; they will be described roughly in order from bus to deflection coils. Further information will be found in (1.1.16) which describes the display controller.



9400-2 BLOCK DIAGRAM

Figure 1.2.1.1



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9400-2 DECODING CIRCUITS

Figure 1.2.2.1

1.2.2 Bus Servicing and Decoding

The 9400-2 uses 16 bus lines <1.2.2.1> of which the 10 LSBs are used as follows:

- D0-7 brightness control of spot on screen
- D0-9 position of spot on screen

while the 5 LSBs are used for mode control purposes:

- D11 0 spot move 1 spot leave
- D12 0 spot off 1 spot on
- D13-15 decode to 8 image control functions:

  - 0 page end, center spot, wait for SYDIS
  - 1 mode 0 and mode 3 together
  - 2 NOP

  - 3 load spot intensity D0-7
  - 4 DX = 0 Y position D0-9
  - 5 DY = 0 X position D0-9
  - 6 DX = 1 Y position D0-9
  - 7 DX = D5-9 DY = D0-4

In addition, there are several control lines to and from the 9400-1:

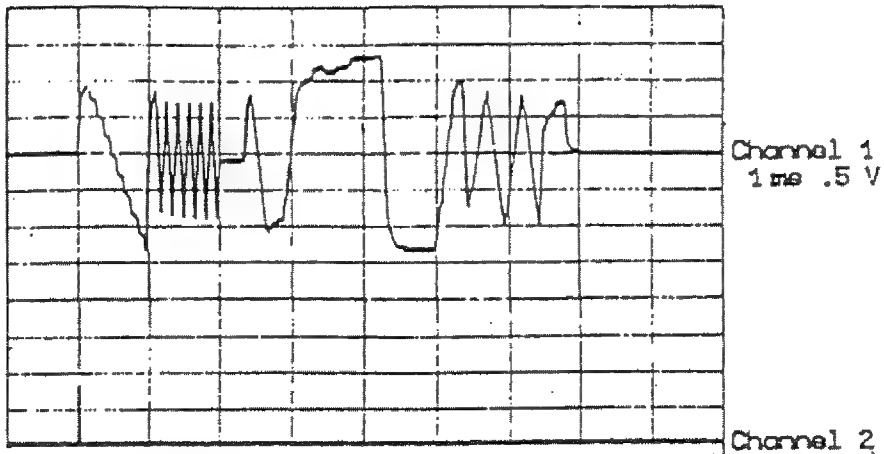
9400-1 to 9400-2:

- CK 8 MHz clock
- RESET general 9400 reset, await SYDIS
- SYDIS start page, 50/60 Hz
- BYDIS 0 RAM busy, 1 data ready
- PDIS load data clock

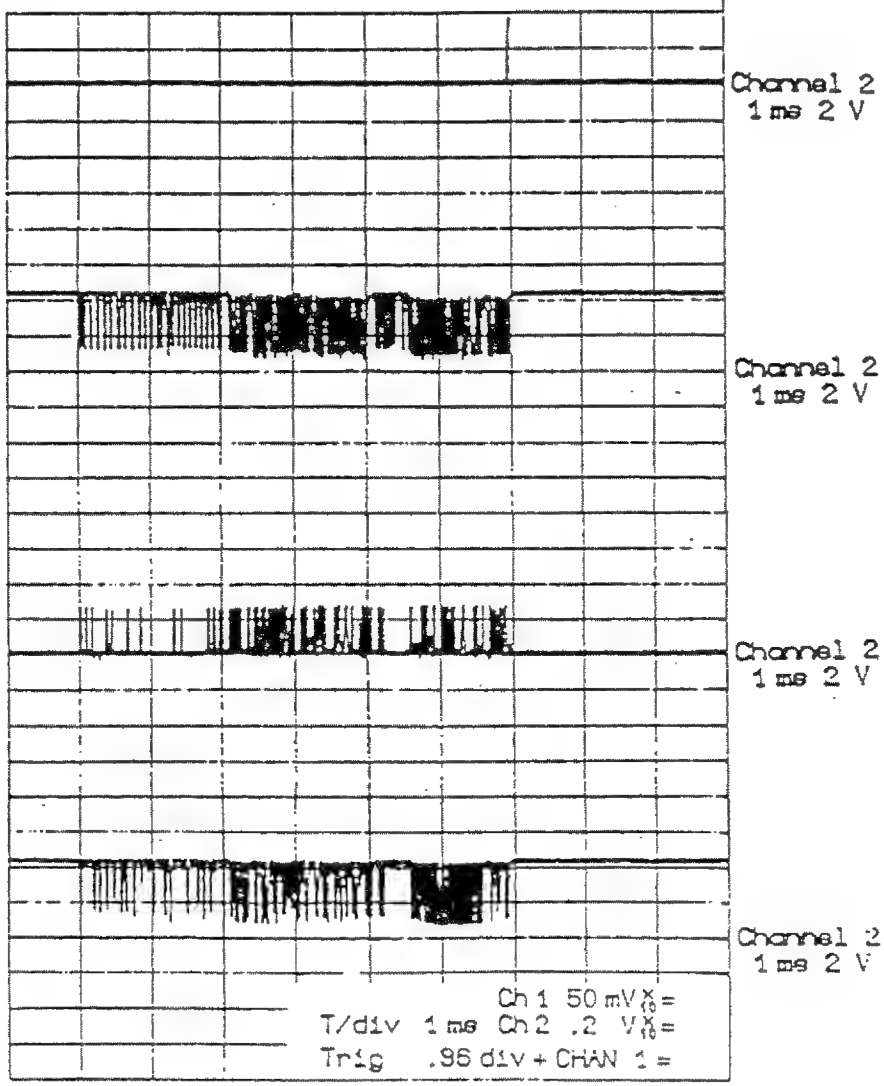
9400-2 to 9400-1:

- PGDIS end of page acknowledge
- DDIS ready for next data
- PGD display blocked

The 10 bit image deflection data go to the three 74LS96 asynchronous 5 bit shift registers, D3-5, which send a serial stream to the 74LS96 shift registers E4 F2 G6 H2 I4 I3, the flip-flops E3 F1 G5 H1, and on to the DACs. The luminance data go straight to the buffer J4, and thence to the Z-DAC J3.



Y	Deflection of trace (for reference only)
SYDIS	Display synchronisation
PGDIS	9400-2 signals page end
BYDIS	RAM busy/data ready
DDIS	9400-2 ready for new data
PDIS	load data clock

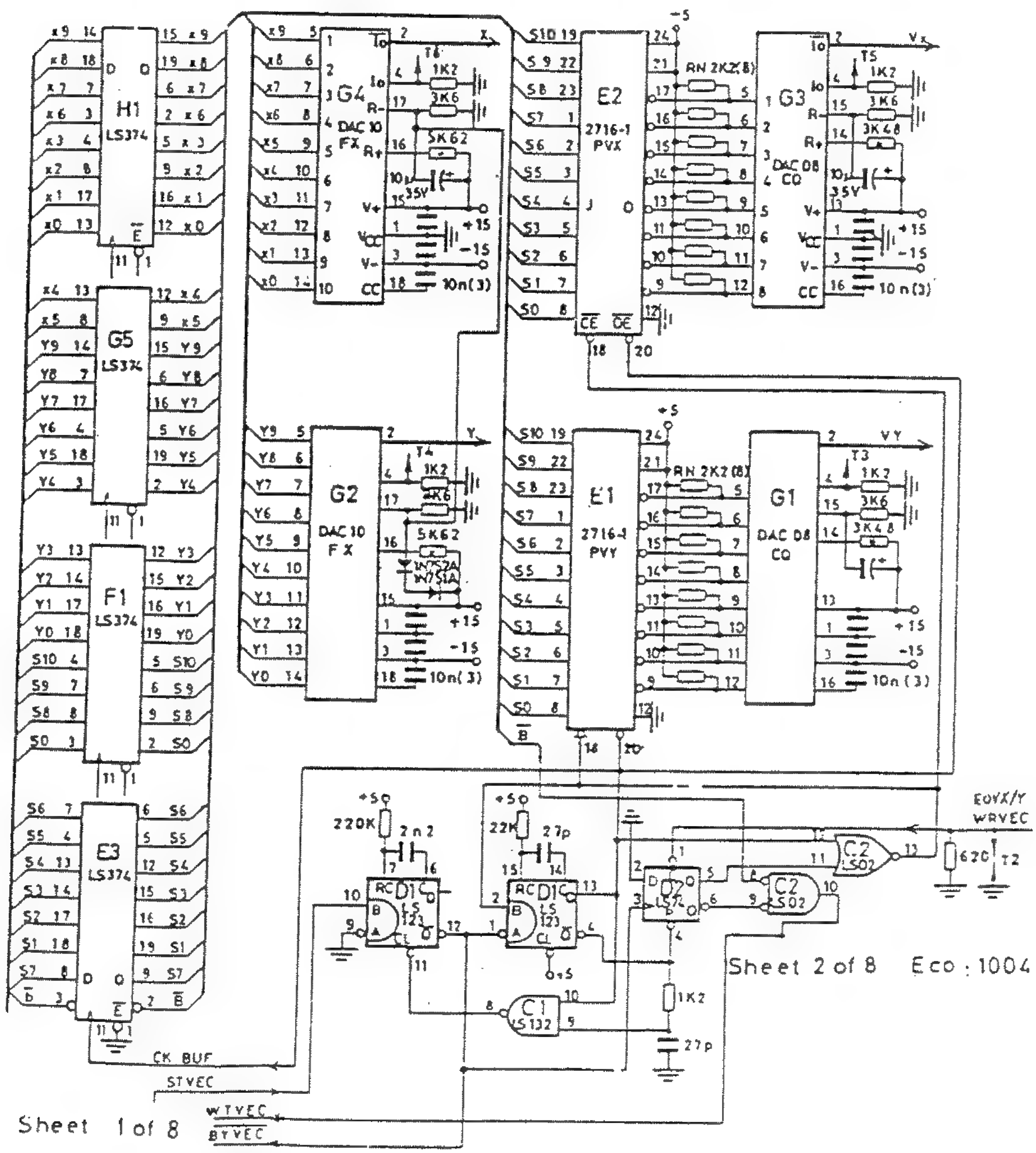


CONTROL SIGNALS FOR THE DISPLAY

Figure 1.2.2.2

1.2.3 X and Y DACs for Position

The parallel data from the final registers F1, G5 and H1, <1.2.2.1> are used by the 10 bit X and Y DACs G4 and G2, to make the analog position data for the next spot position <1.2.3.1>, the signals going respectively to the X and Y deflection processors. The S data from E3 and F1 go to the 2 K byte EPROMs E1 and E2, which contain conversion tables which convert the input data to X and Y velocities, with 8 bit precision. The VX and VY signals go to the two deflection processors (1.2.6).



X AND Y DACS FOR POSITION AND VELOCITY

Figure 1.2.3.1

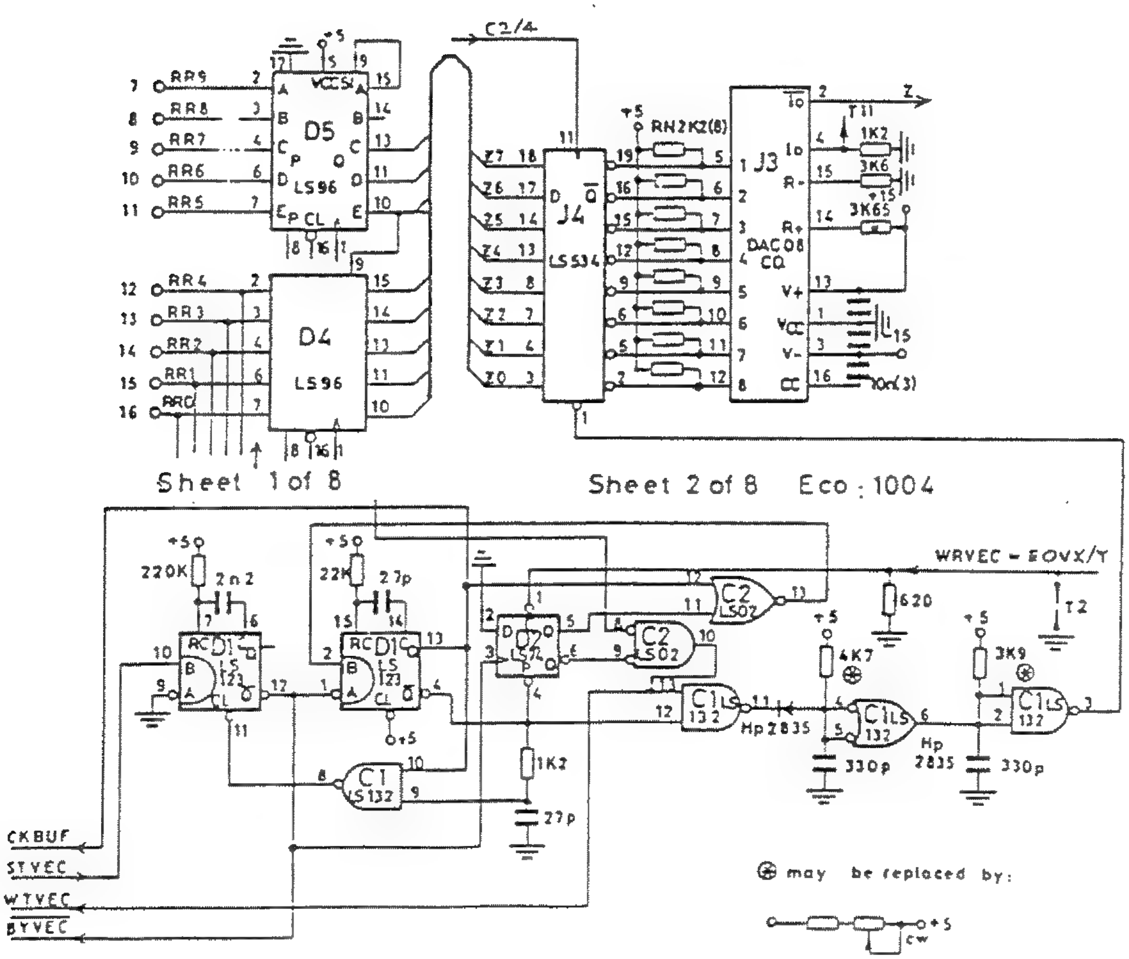
This diagram <1.2.2.2> shows the control signals for a simple example of a display, including one grid, and one trace with the accompanying settings data. The first picture shows the actual screen image on one 9400 DSO. The other pictures are taken from a second DSO which probed first. The signals shown are (from top to bottom):

Y	The vertical deflection signal
SYDIS	Display sync
PGDIS	Page end
BYDIS	RAM busy/data ready
DDIS	9400-2 ready for next data
PDIS	data strobe

It will be seen that there is more activity than the number of vectors would seem to require - this is because long vectors are drawn in segments of no more than a quarter of the screen size.

1.2.4 Luminance DAC

The 8 bit DAC J3 is loaded from the register J4, clocked by C1, at a slightly different time than the clocking of X and Y <1.2.4.1>, a subtle effect of the deflection coil impedance, so that turning the trace on and off coincides exactly with the change in velocity of the spot. Note that Z actually cuts off the beam between vectors for a very short time, so that the Z waveform consists of flat sections with spikes. Z goes more negative to increase brightness. The Z line is pulled up <1.2.5.1> in the event of various problems which would cause phosphor damage. The 9400 DSO does not have a means of detecting scan loss, so power should never be applied unless both deflection coils are in place.

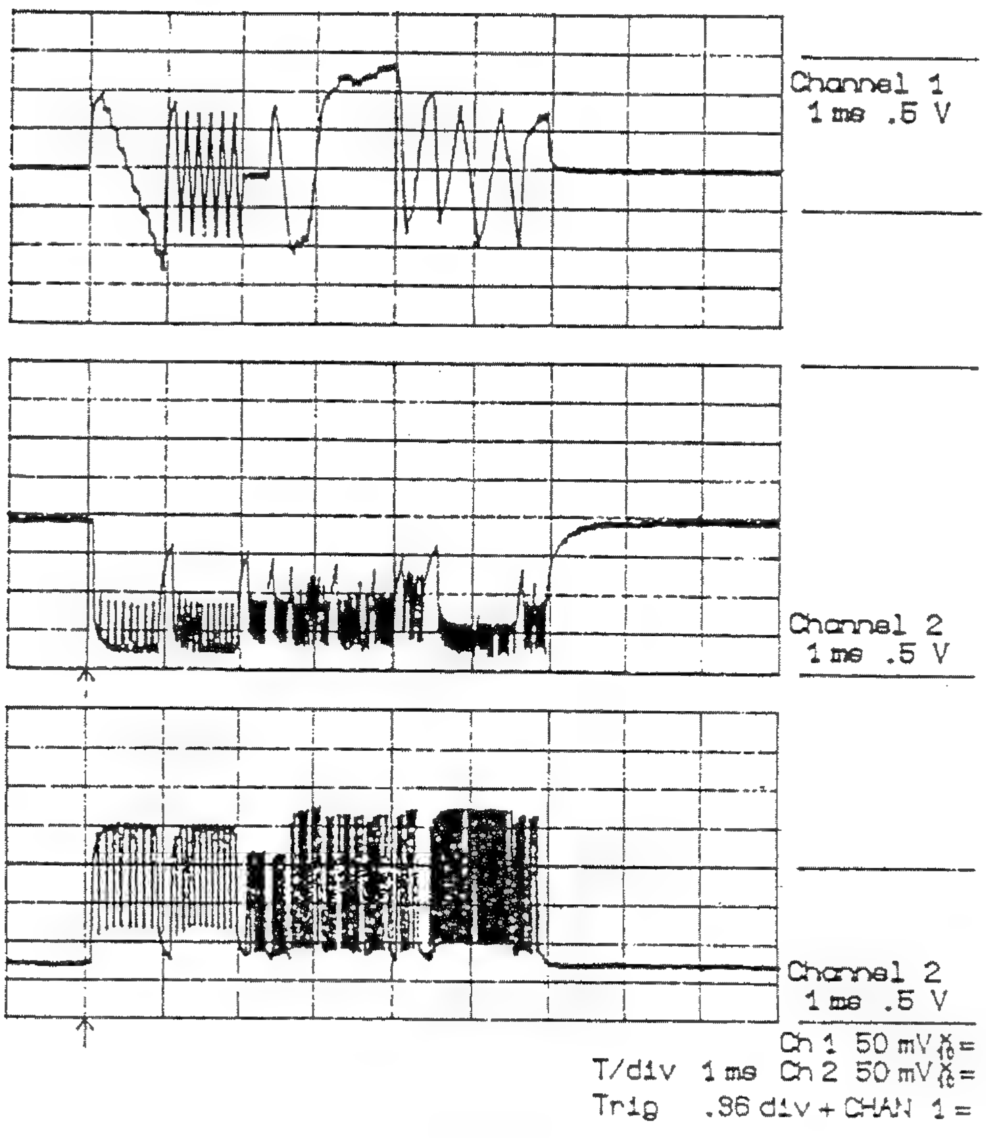


LUMINANCE DAC FOR Z

Figure 1.2.4.1

This diagram shows the brightness signal for the same screen as in <1.2.2.2>. The functions shown here are (from top to bottom):

Y	Vertical deflection signal
Z	Brightness signal, negative excursion = brighter
TP11	Z DAC test point, positive excursion = brighter



BRIGHTNESS SIGNALS FOR A SIMPLE DISPLAY

Figure 1.2.4.2

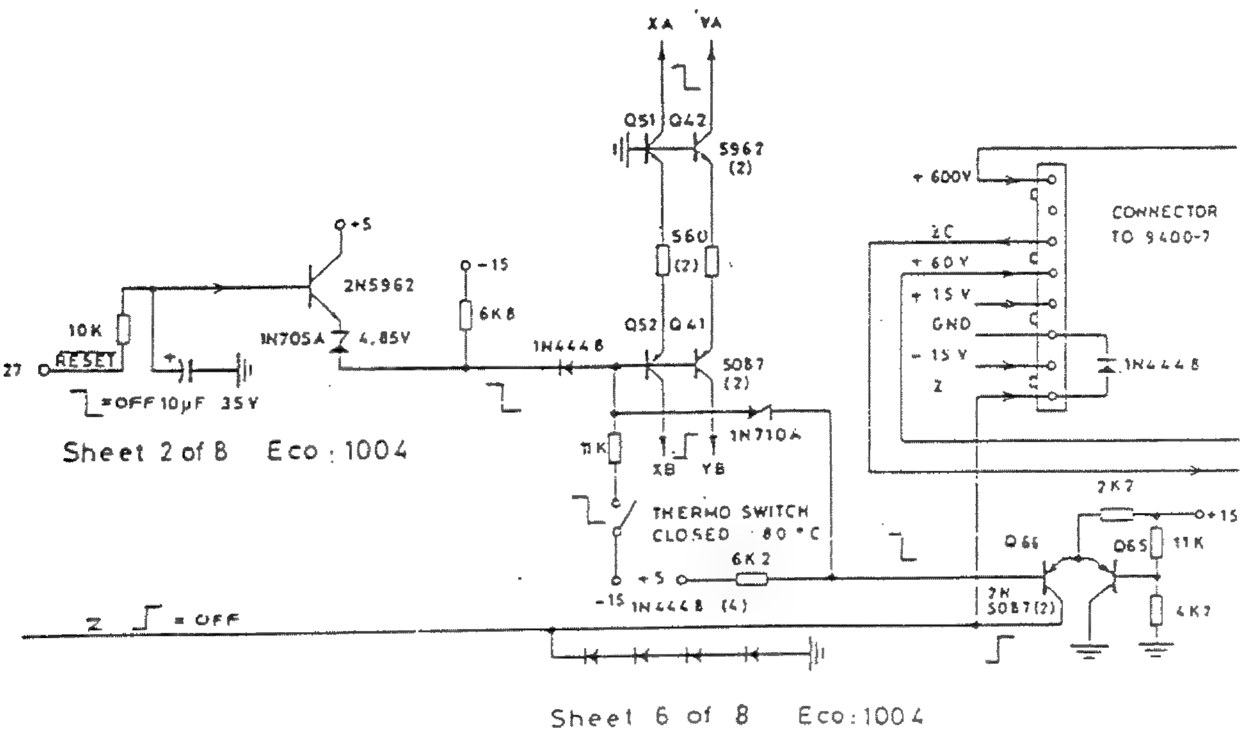
1.2.5 Reset and Protection Circuits

RESET is the general 9400 DSO reset, which is held low during power up reset (1.1.3) and during auto reboot (1.1.2) should that event occur during DSO operations. If the RESET line goes low <1.2.5.1> the spot is taken to the middle of the screen, by XA, YA, XB, YB <1.2.8.1> and the beam is cut off by Z.

The RESET line goes to a 2N5962 emitter follower, which, with the 1N748A Zener diode, produces a small negative potential at AMPL OFF. If RESET goes low, AMPL OFF turns on Q41-42, and Q51-52, pulling YA, YB and XA, XB toward ground, and cutting off the signal to the output stages of the deflection amplifiers. At the same time, Q66 turns on, making Z go sufficiently positive to cut off the CRT beam current.

The thermal switch will have the same effects, if the temperature of the heat sink of the power MOSFETs in the power amplifiers should reach 80 C.

In the event of the +5 V line going down, AMPL OFF is pulled down as for a reset, cutting off beam and deflection. Several other protection modes are provided on the 9400-7 CRT board (1.7), to protect the sensitive CRT phosphor.



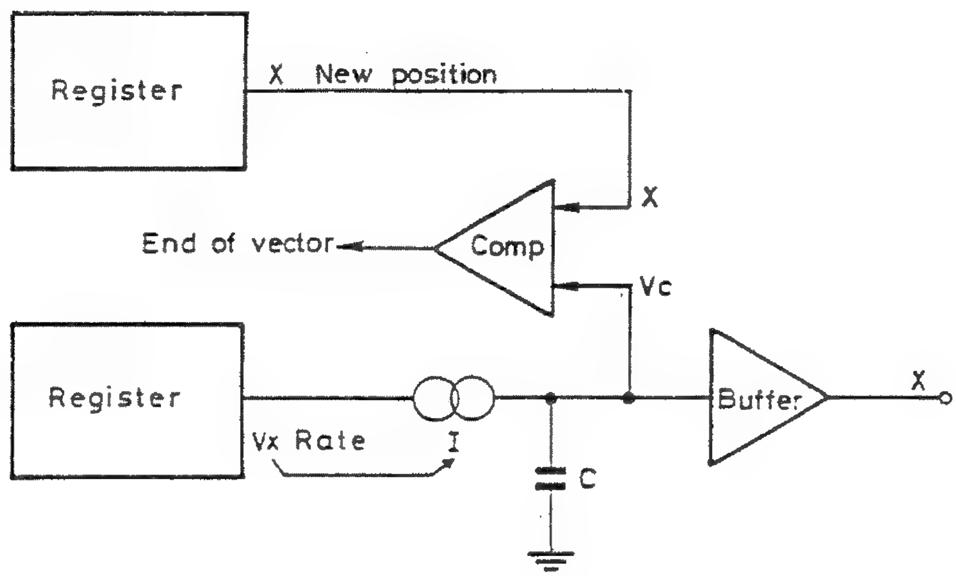
RESET AND PROTECTION CIRCUITS

Figure 1.2.5.1

1.2.6 Deflection Processing - Rate Integrators

1.2.6.1 Principal of Operation

The function of the rate integrators is to produce a succession of linear ramps at the right rate for moving the CRT spot between successive X and Y points. The basic idea is that the integrator is presented with velocity data, and final position data as shown in the notional diagram of the principle <1.2.6.1>. The integrator ramps until the comparator toggles, at which point the process stops and new data are requested.



BASIC INTEGRATOR OPERATION

Figure 1.2.6.1

1.2.6.2 Actual Integrator Functions

There is one rate integrator for each deflection axis; as they are identical, only one will be described <1.2.6.2>. The position signal X passes through the buffer I1, and drives the base of Q26. The rate signal VX drives the emitters of Q19-20, one of which will be on. Note that the current mirror Q16-20 has the extra transistor Q18, so that the accuracy of the current match is greater than in a simple mirror, where the two currents differ by one base current.

The precision high stability 150 nF capacitor charges at a constant rate, driving the follower Q21, which passes on the signal for further processing. This signal is also fed back via a Zener diode to Q25 base.

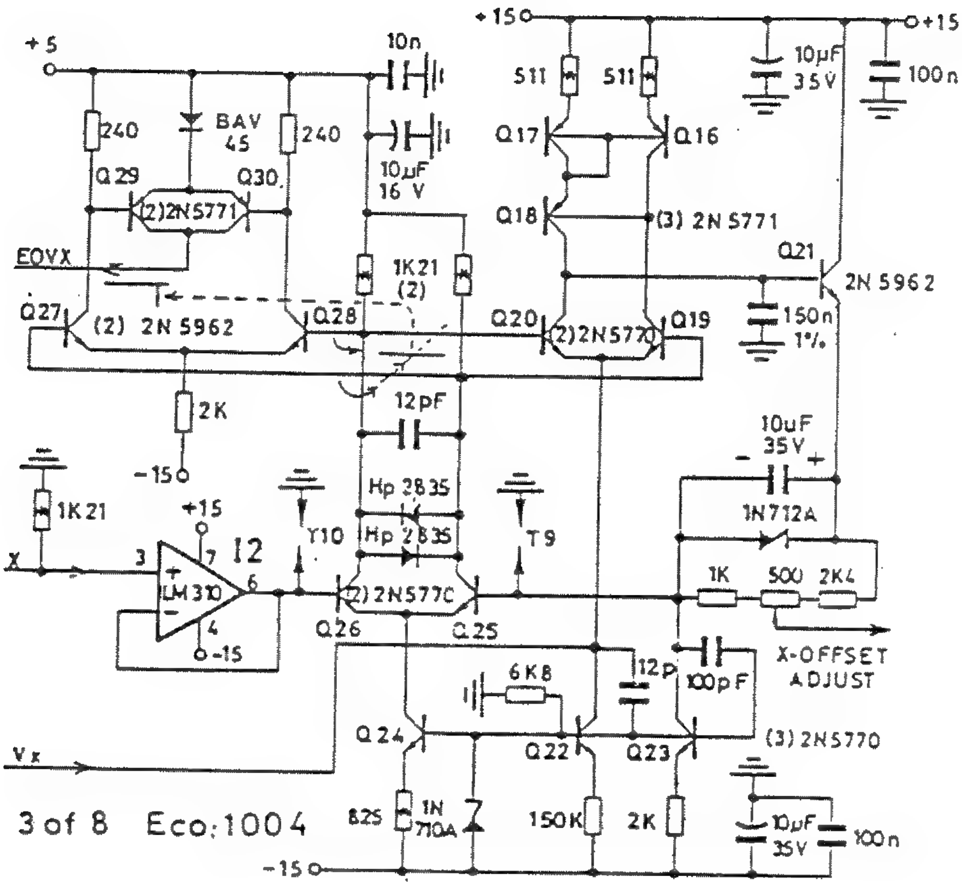
Because one LSB of the position DACs corresponds to only 4 mV, several pairs of transistors must be matched to this accuracy. The pairs are:

Q1-2 Q4-5 Q12-13 Q16-17 Q19-20 Q27-28.

While the capacitor is being charged or discharged during a vector, the long tail pair Q25-26 will hold one transistor on and one off, in each pair, Q19-20, Q27-28 and Q29-30. Therefore, one transistor will pull EOVX high. Note that EOVX and EOVY are wire ORed, and they act on the CLEAR of D2 pin 1. When the voltages at T9 and T10 become equal, neither Q29 nor Q30 will conduct, because the b-e drop of Q29-30 plus diode drop BAV45 is more than the voltage across the 240 ohm resistor. Thus EOVX will drop, and clear D2, disabling the EPROMs via C2 pin 13. The wire OR means that although circuit tolerances will cause either X or Y to terminate first, the trace will then disappear, so that a little kink at the end is not seen.

EOVX/EOVY therefore show a succession of narrow spikes at T2 in a working system. C2 pin 10 drives C1 to turn off Z, which also makes a spike at the end of each vector.

The waveform from the Y deflection DAC <1.2.6.3> is shown with the eventual deflection signal for the same case as in <1.2.2.2>.



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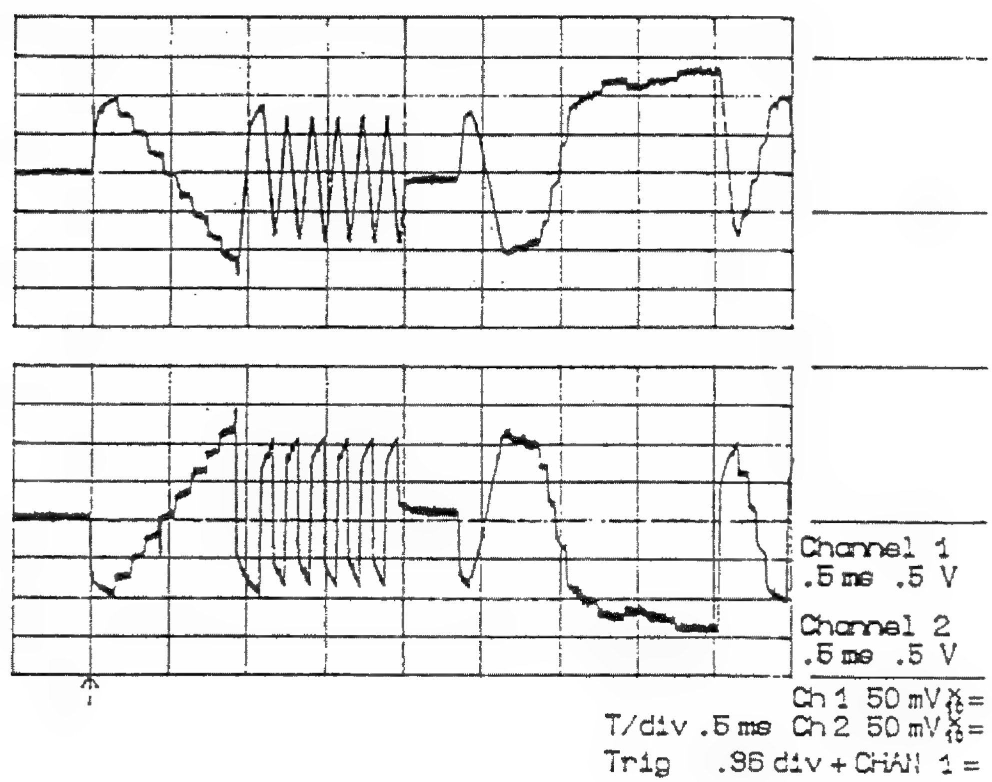
RATE INTEGRATOR SCHEMATIC

Figure 1.2.6.2

Upper waveform is required deflection signal
Lower waveform is input to integrator



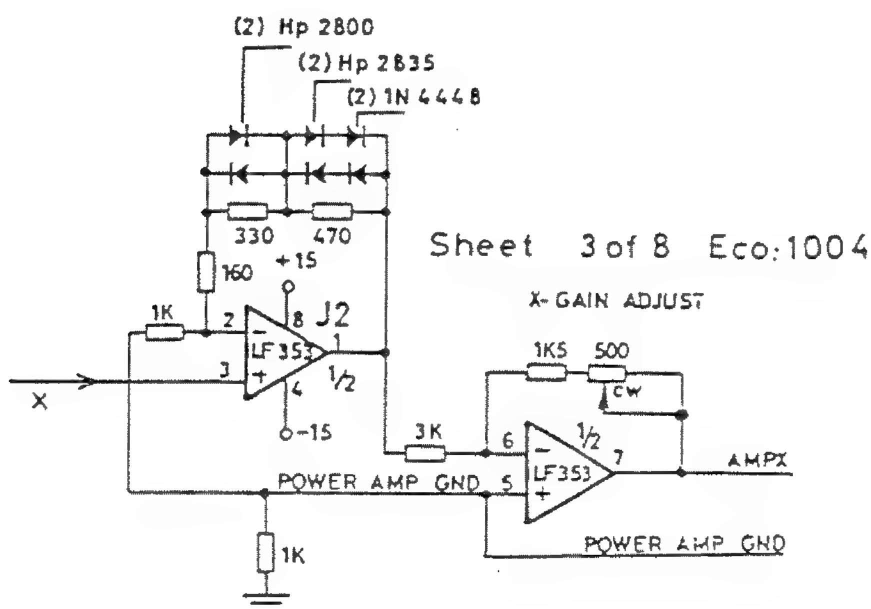
SIGNALS AT THE INTEGRATOR INPUT

Figure 1.2.6.3

1.2.7 Deflection Processing - Linearity Correction

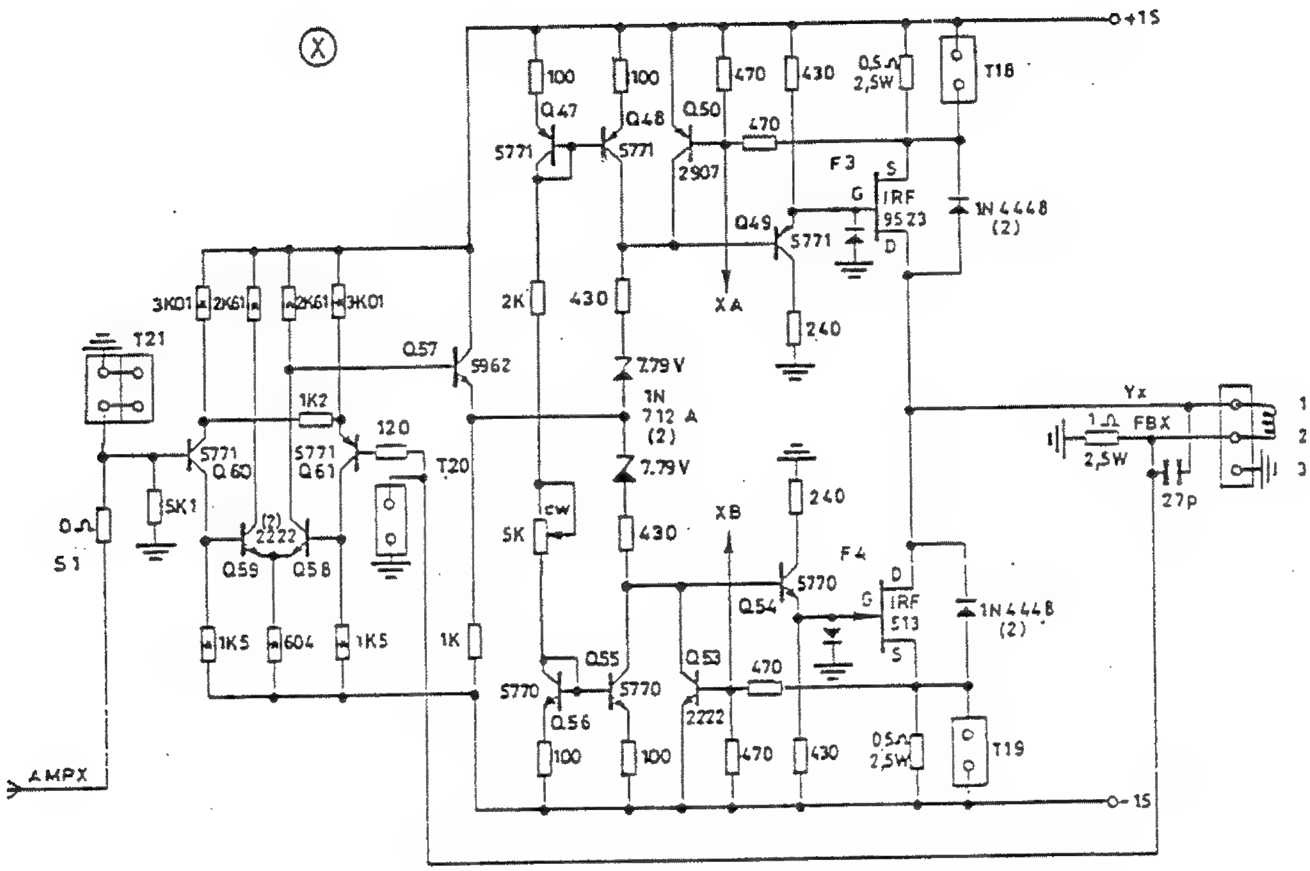
The deflection system in a magnetically deflected CRT is complicated by the fact that the angle of beam deflection is, in principle, proportional to the yoke current, while the displacement on the screen is roughly proportional to the tangent of the deflection angle, as the screen is nearly flat. Some corrections can be made by careful yoke design, but there remains a non-linearity which must be corrected, although the linearity need not be absolutely perfect, because the grid and the waveforms are generated by the same system. Nevertheless, a good appearance of linearity is desirable.

To counteract the increasing rate of change of TAN A at higher A, the correction circuits <1.2.7.1> increase the negative feedback at higher deflections, through the non-linearity of the diodes at op-amp J1 pins 1 and 2. The other half of J1 provides an inverting buffer and a means of presetting the gain to the correct value. Offset is adjustable by a movable pick-off from the Zener diode.



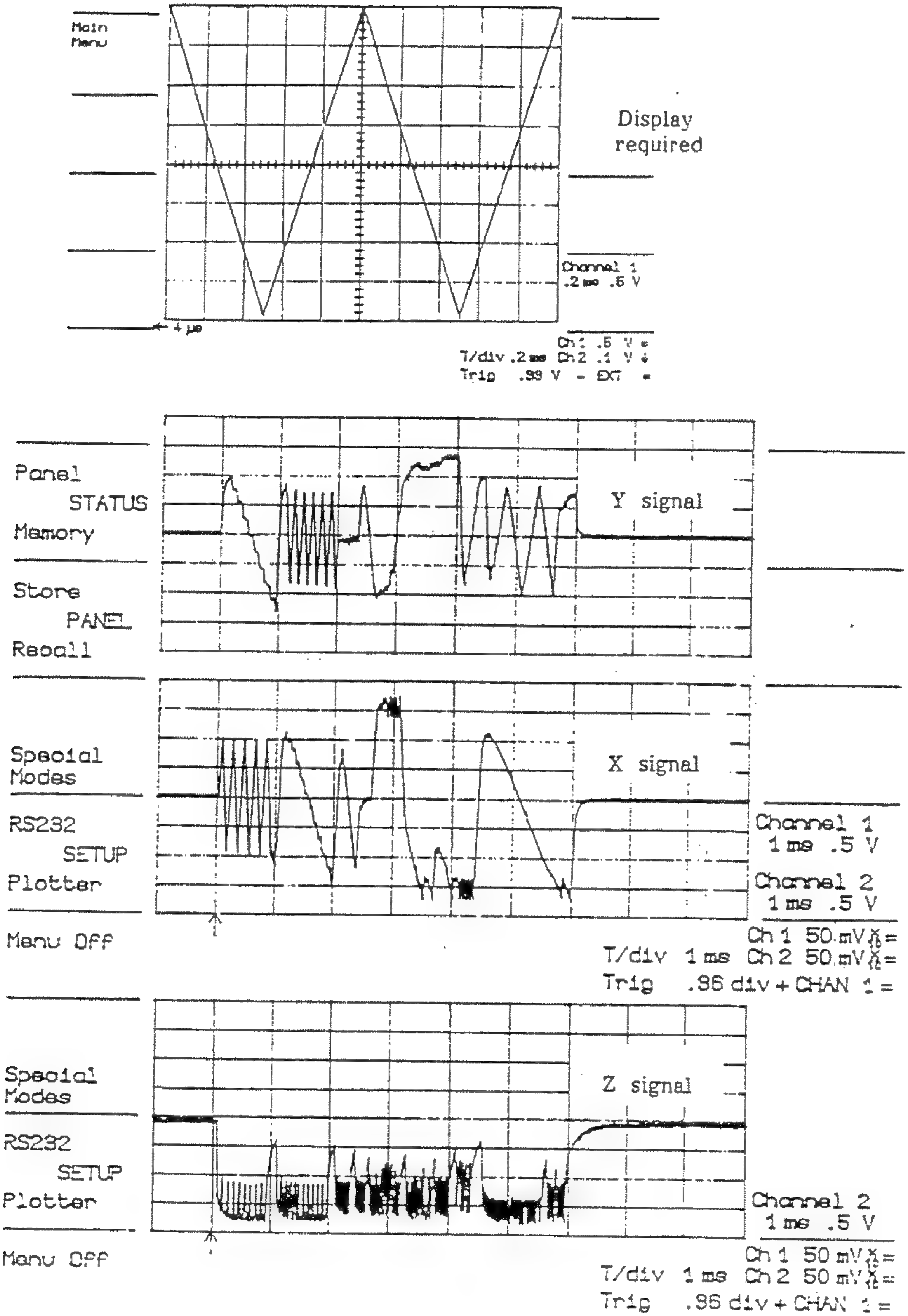
NON-LINEARITY CORRECTION

Figure 1.2.7.1



POWER AMPLIFIERS

Figure 1.2.8.1



X, Y AND Z WAVEFORMS TO PRODUCE A SIMPLE DISPLAY

Figure 1.2.8.2

1.2.8 Deflection Processing - Power Amplifiers

The X and Y amplifiers are linear amplifiers which use feedback from the 1 ohm resistor in series with the deflection coils <1.2.8.1> to produce an output current which is proportional to input voltage, the gain being 1A/V.

The input stage Q58-61, is a high gain subtraction stage, whose output is the difference between the input and the feedback. Q57 is follower to feed the driver stages Q49 and Q54 via the level shifters, which each comprise a Zener diode and a resistor. The drivers feed power MOSFETs, which supply the deflection current. Because these devices have large gate capacitance, substantial drive current is needed.

To protect against excessive current demand upon the MOSFETs the two 0.5 ohm current sensing resistors feed back a signal which turns on Q50 and Q53 if the current reaches a preset limit.

To keep a standing current in the MOSFETs in the absence of drive (for no feedback system can work if there is no gain) the 5 k potentiometer is adjusted to drive the current mirrors Q47-48 and Q55-56 at the correct level.

Catching diodes are provided on the MOSFET gates, and also on the drains, to guard against inductive effects from the load. Note that voltage waveforms measured in the amplifier will, in general, have more spikes than the input voltage and output current signals, because of the inductive load. A 27 pF capacitor across the load gives high frequency stability.

Waveforms for a display with one simple waveform and a grid are shown in <1.2.8.2>, in which the top part of the diagram shows what appears on the screen, while the middle two sections show signals obtained by probing with a second 9400 DSO, Y deflection above, and X deflection below. At the bottom the Z signal is included; it goes more negative to increase brightness.

From right to left can be seen the X and Y waveforms which produce:

horizontal grid lines,
vertical grid lines,
various small features,
the displayed waveform.

1.2.9 CRT Power Supplies

1.2.9.1 Introduction

The CRT requires several power supplies at different voltages, for the cathode, the control grid, the electron gun, including focusing, and the final anode. These are all supplied by an oscillator based circuit on the 9400-2 board <1.2.9.1>.

The supplies are as follows:

- heater for cathode	15 V DC
- cathode, from luminance circuit	
- grid, variable,	0 V approximate
- anode 1	400 V DC approx
- focus electrode	variable DC
- final anode	11 kV DC

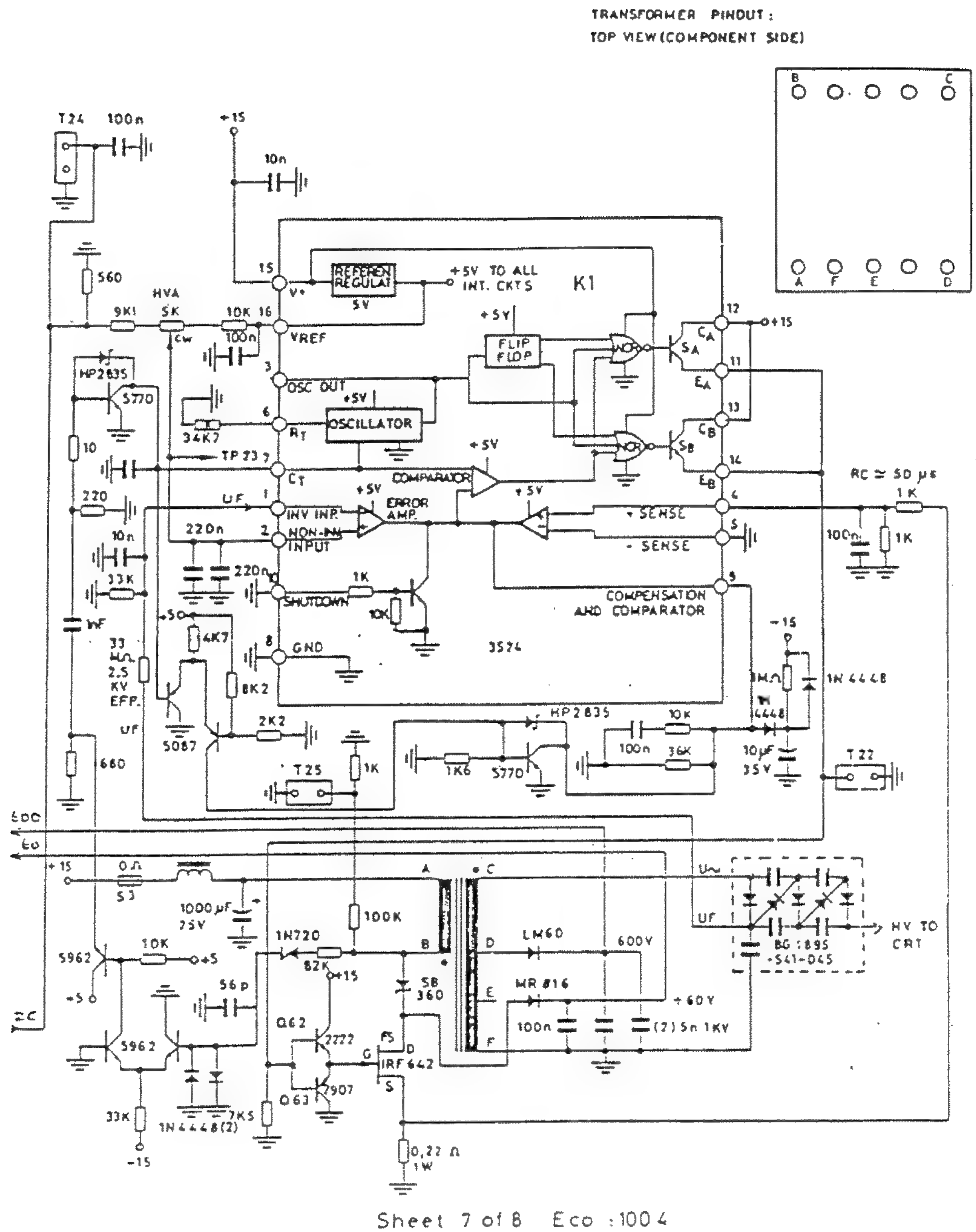
The distribution and control of these supplies is described in (1.2.4) and (1.7), as well as in this section.

1.2.9.2 Oscillator

The oscillator which drives the EHT generator is 3524 single chip device which is timed by an RC time constant, connected at pins RT and CT of the 3524. The RC voltage is sensed by a comparator, whose reference is derived from an error amplifier, the shutdown control being unused in this application.

In uncontrolled free running oscillation the device would generate pulse at the transistors SA and SB, with a half cycle difference; in this application they are wire ORed so that the effective output frequency is doubled. The duty cycle of these pulses is a function of the comparator reference level.

In fact, the behavior of the oscillator is considerably modified by the various feedback loops provided. These are described in the next section.



CRT POWER SUPPLIES

Figure 1.2.9.1

1.2.9.3 EHT Driver Stage

This is the part at the bottom of the schematic. The SA+SB output drives the complementary emitter follower pair, Q62-63, to give the current drive to the MOSFET F5, which although in principle a voltage driven device, has a large interelectrode capacitance which requires current if a fast risetime is needed. The saturated transformer allows a current ramp in the MOSFET, which is suddenly turned off by Q63. The stored energy is used at the secondary to drive the following:

- BG1895 multiplier to generate final anode voltage
- LM60 and reservoir to generate 600 V
- MR816 and reservoir to generate 60 V

The SB360 in the FET drain path prevents the built-in reverse protection diode of the FET from damping the oscillation of the transformer after one half cycle. The oscillation would in fact continue for several cycles, but for the way the feedback comes into play.

1.2.9.4 Feedback Controls

- Feedback from B on the transformer, via a long tail pair eventually reaches a 2N5770, which discharges the timing capacitor at pin CT, prematurely ending the timing cycle.

- Feedback from FET source. This is a current sensor, feeding the +SENSE input of the oscillator, to control current limit.

- Feedback from UF, the multiplier input, to the inverting input of the error amplifier, gives stabilization of the EHT voltage, since the impedance of the multiplier is low relative to that of the CRT. If the current demand of the CRT is raised or lowered because the brightness controls are adjusted, or because the complexity of the image is changed, the UF voltage trips the comparator at a different time, altering the duty cycle at SA+SB.

1.3 9400-3 and 9400-3A ADC Boards

Table of Contents

There are two types of ADC boards in the 9400 and 9400A oscilloscopes as follows:

9400-3 boards: in 9400s with serial numbers up to about 87200 (October 87),

9400-3A boards: in 9400s with serial numbers above about 87200 (October 87 and in all 9400A oscilloscopes.

This chapter was written for the 9400-3 board: for the 9400-3A, some supplementary sections are included. See Figures 1.3.1A and 1.3.2A.

The two boards are interchangeable, (with one minor modification described below), because the timings of the 9400-3A have been made to emulate those of the 9400-3, even though the ADC circuits are completely different.

Important Distinction between the 9400 and the 9400A

In order to increase the bandwidth for the Model 9400A, the gain on the 9400-3A ADC board is slightly decreased (ECO 1004 for the 9400-3A board). For this, the feedback resistor between pin 18 and pin 8 of the HSH202 is changed from 1 kΩ to 910 Ω. This loss of gain is compensated for at the HVV output (pin 22) by replacing the 43 Ω resistor to 39 Ω (ECO 1016 for the 9400-1 main board). The resistor R at the HVV output defines the gain between the front-end and the ADC as:

$$\text{gain between front-end and ADC} = \frac{R}{R + 50}$$

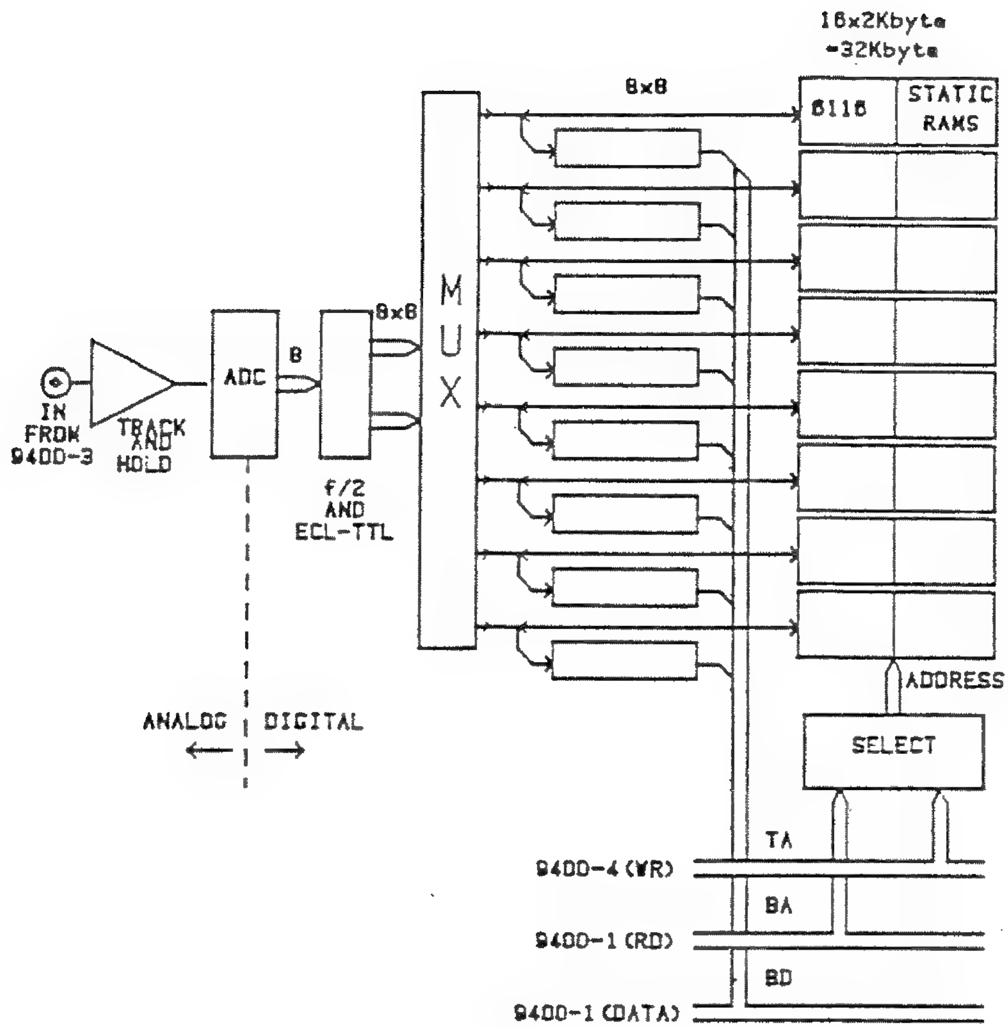
In addition, HVV at ECO 1003 has to be used on 9400-1 at ECO 1016. Therefore, be careful not to mix these ECOs between the 9400, the old with the 9400-3 and the new with the 9400-3, and the 9400A. The possible configurations are listed below:

9400 with old 9400-3	9400-1 at ECO 1015 with 43 Ω at HVV output.
9400 with new 9400-3A	9400-1 at ECO 1016 with 39 Ω at HVV output HVV at ECO 1003. 9400-3A at ECO 1004 with 910 Ω S/H feedback. OR 9400-1 at ECO 1015 with 43 Ω at HVV output 9400-3A at ECO 1003 with 1 kΩ S/H feedback
9400A	9400-1 at ECO 1016 with 39 Ω at HVV output HVV at ECO 1003 9400-3A at ECO 1004 with 910 Ω S/H feedback

If resistors have to be changed to prepare a board for one of the four configurations above, make sure that:

- the overall gain (front-end + ADC) is within limits. Check this by using the internal test "gain curves" for all sensitivities and BW ON and OFF. See the internal tests, Section 3.1.7. The overall gain for all sensitivities can be readjusted by changing the resistor at the HVV output.

- the HF overshoot is within limits, see adjustment 2.4.3.4. If the feedback resistor on the ADC board is changed, the capacitor parallel to it MUST be readjusted.



BLOCK DIAGRAM OF 9400-3 ADC BOARDS

Figure 1.3.1.1

1.3 9400-3 ADC Boards

Each DSO contains two of these boards, one for each analog input channel. The functions of these boards are to:

- Track and Hold analog data from preamplifiers
- Convert held samples to 8-bit words
- Write 8-bit words into 32K RAM at current address
- Hold digital data in RAM until required
- Read 32K RAM and send data to processor

1.3.1 Functional Outline of the 9400-3

The main functions of the ADC boards are shown in <1.3.1.1> and they will be described in a progression from the analog input to the memory output to the bus. It will be seen from the schematic (8.3) that there are many preset controls on the ADC boards. These must not be adjusted in the field; each one requires calibration using LeCroy test gear designed for this board. Furthermore, changing hybrids and other parts at the front-end of these boards will also create a need for recalibration.

The 9400-3 boards are controlled by the 9400-4 board, which sends clock signals, control signals, and addresses to the 9400-3. There are two groups of clock signals, the fast clock, CK, which is always 50 MHz or 100 MHz, which governs the track hold and ADC, and the memory writing clock, CKR, which with SYNC, runs at a wide range of frequencies to accommodate the many different time-base settings of the 9400. Thus at all but the fastest time-base settings, the 9400-3 makes many more samples than are actually used by the DSO.

Because, at many of the faster settings, the static RAMs cannot keep up with the supply of samples, the data are multiplexed, at first into two streams, then into 16, so that each memory IC is exercised relatively infrequently. The data are buffered into the 9400-1 in two ways. In normal mode the data would be written into the static RAMs during an acquisition, and read out afterwards. In roll mode, which is employed at the very slowest time-base settings, the data are sent straight to the 9400-1 board for processing on to the display.

A table relating clock rates to time base settings will be found in (1.4).

1.3.2 Clock Management

The analog sections of the 9400-3 board use three lines of the clock bus, <1.3.2.1> pins 2 and 3, CK, which are anti-phase 100 MHz or 50 MHz signals, and pin 5, RATE, which is a level which is high for 100 MHz, low for 50 MHz. All the clock bus signals are generated on the 9400-4 <1.4.6.1>.

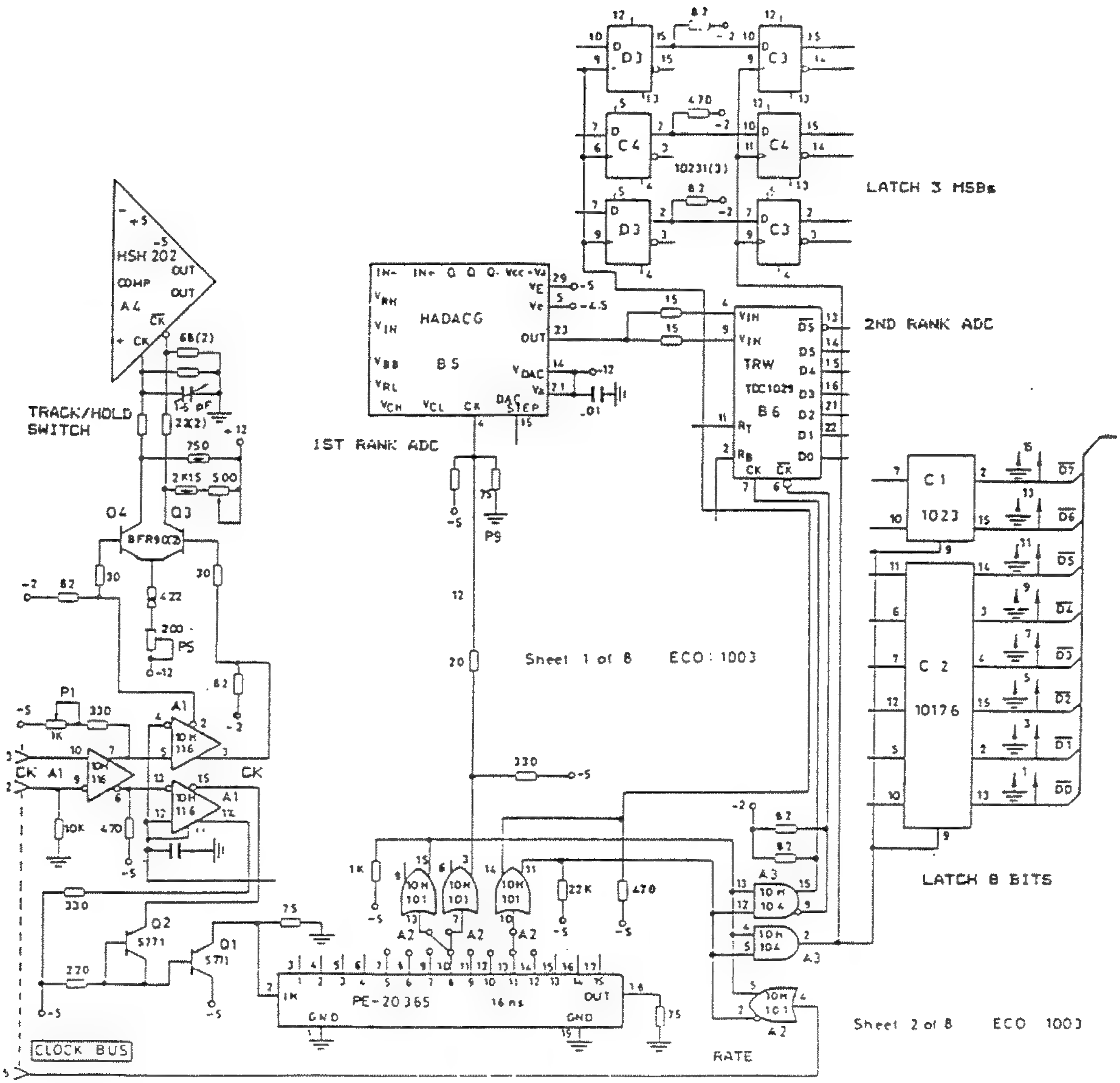
ECL line receivers A1 transmit the clock to the HSH202 sample-and-hold via the long tail pair Q3-4. There are four preset adjustments associated with this circuit:

- P1 Adjustment of track hold ratio
- P4
- P5
- 1-5 pF These three adjustments are tuned up during manufacture to minimize two unwanted effects in the sample-and-hold circuits. These are:

- Recovery spikes, which are glitches that could appear in the analog output as a result of digital breakthrough at the transitions between track and hold.

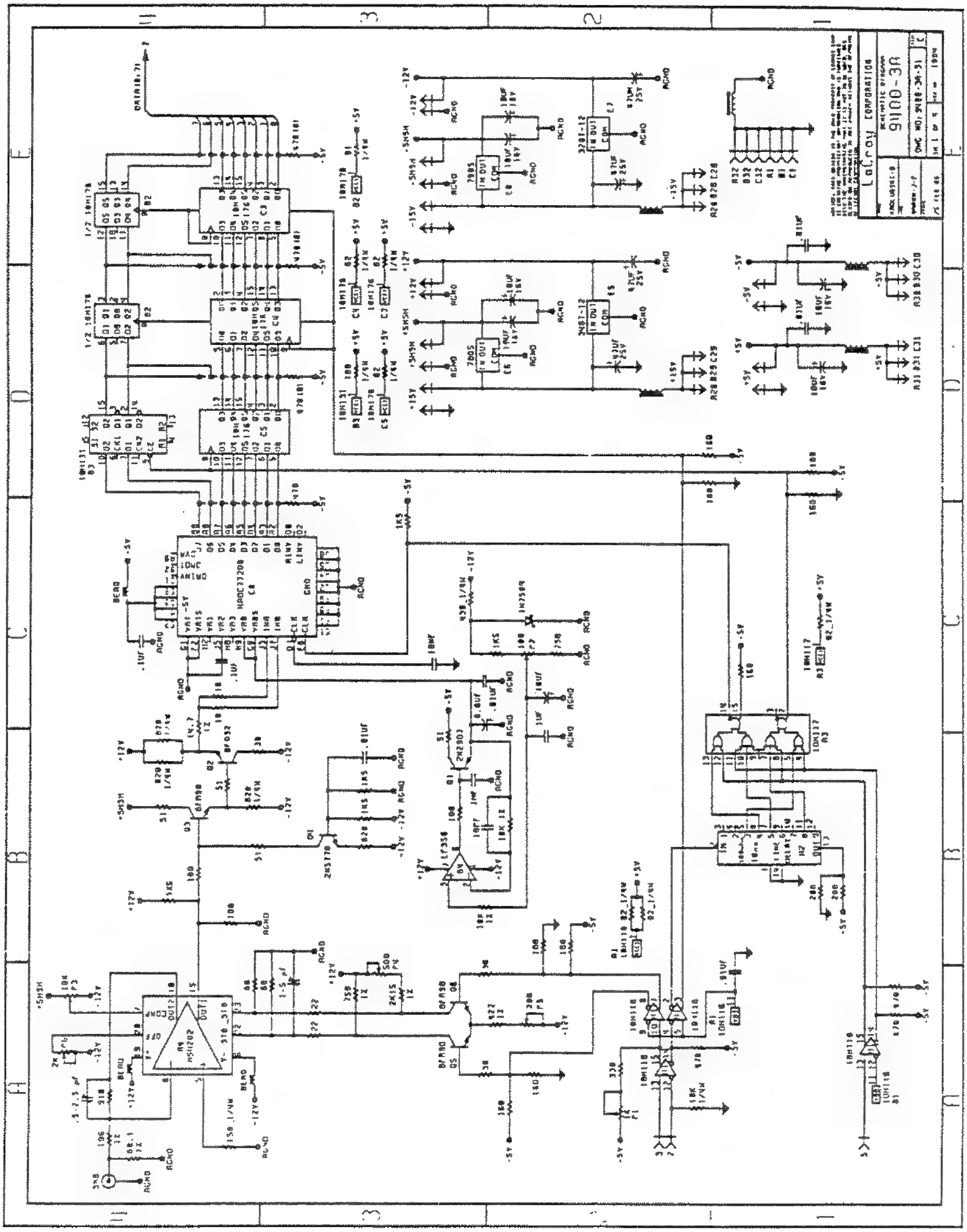
- Track hold step, an unwanted level shift that can occur between the track phase and the hold phase.

  The clock also goes to Q2, which is saturated, and acts as a level shifting diode, and Q1, an emitter follower to drive the 75 Ω delay line which is needed to time the functions of the dual-rank ADC. The RATE level at A2 is used to select the clock rate to the second-rank ADC B6.



9400-3 CLOCK MANAGEMENT

Figure 1.3.2.1



9400-3A BOARD

FIGURE 1.3.2A

1.3.2A Clock Management

The CK bi-phase clock from the clock bus, pins 2 and 3, drives three circuits -

- The sample-and-hold hybrid, A4, a HSH 202
- The 8-bit flash ADC, C6, a HADC7720
- The digital delay, B2, B3, C3, C4, C5

The ADC is clocked at either 100 MHz or 50 MHz depending on the time-base setting. The clock-bus line RATE, pin 5, is high for 100 MHz and low for 50 MHz. All signals on the clock bus originate on the 9400-4 board.

ECL line receivers transmit the clock to the HSH202 via the long-tail pair Q5, Q6. There are four preset controls in this part of the board -

- P1 Adjustment of the track:hold ratio
- P4
- P5
- 1-5 pF

These three controls are tuned during manufacture to minimize track-and-hold problems

The clock also drives the delay line A2, from which A3 produces a clock for the ADC, and a clock for the delay circuits. The ADC clock is timed to clock the ADC correctly with respect to the sample-and-hold.

The ADC clock is unbalanced and has a duty cycle of about 60%. The extra time between the "hold" and the "decode" enables the digital values to settle with sufficient reliability so that fliers are not a problem.

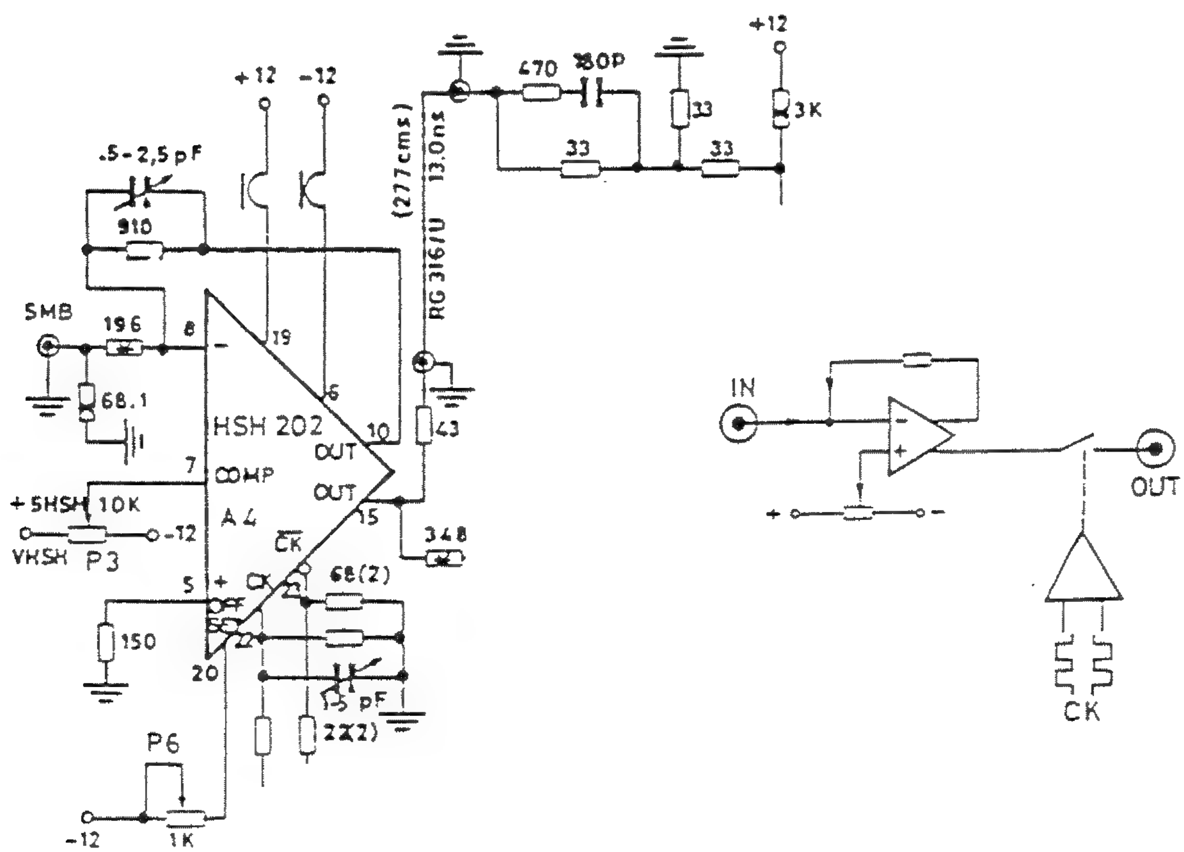
1.3.3 Track and Hold

These functions are based on the HSH202 hybrid which was developed at LeCroy SA. The circuit <1.3.3.1> contains an accurate amplifier with high gain, and a gate/hold function. In the track function, the device acts as an amplifier with two outputs, one used to feed the ADCs, (pin 15) and the other for feedback, via the compensation trim RC network. There are two presets for the HSH202, neither of which is field adjustable without the special test gear for the 9400-3 board. The presets are:

- P3 — Hold rise/droop adjustment.
  At the correct setting, the output voltage neither drifts up nor drifts down during the hold phase.

- 0.5-2.5 pF — Amplifier compensation, set to give maximum bandwidth without undue overshoot on step responses.

The clock inputs are used to make the transitions between the track phase and the hold phase.



TRACK AND HOLD SCHEMATIC AND BLOCK DIAGRAM

Figure 1.3.3.1

1.3.4 Dual-rank ADC Functions

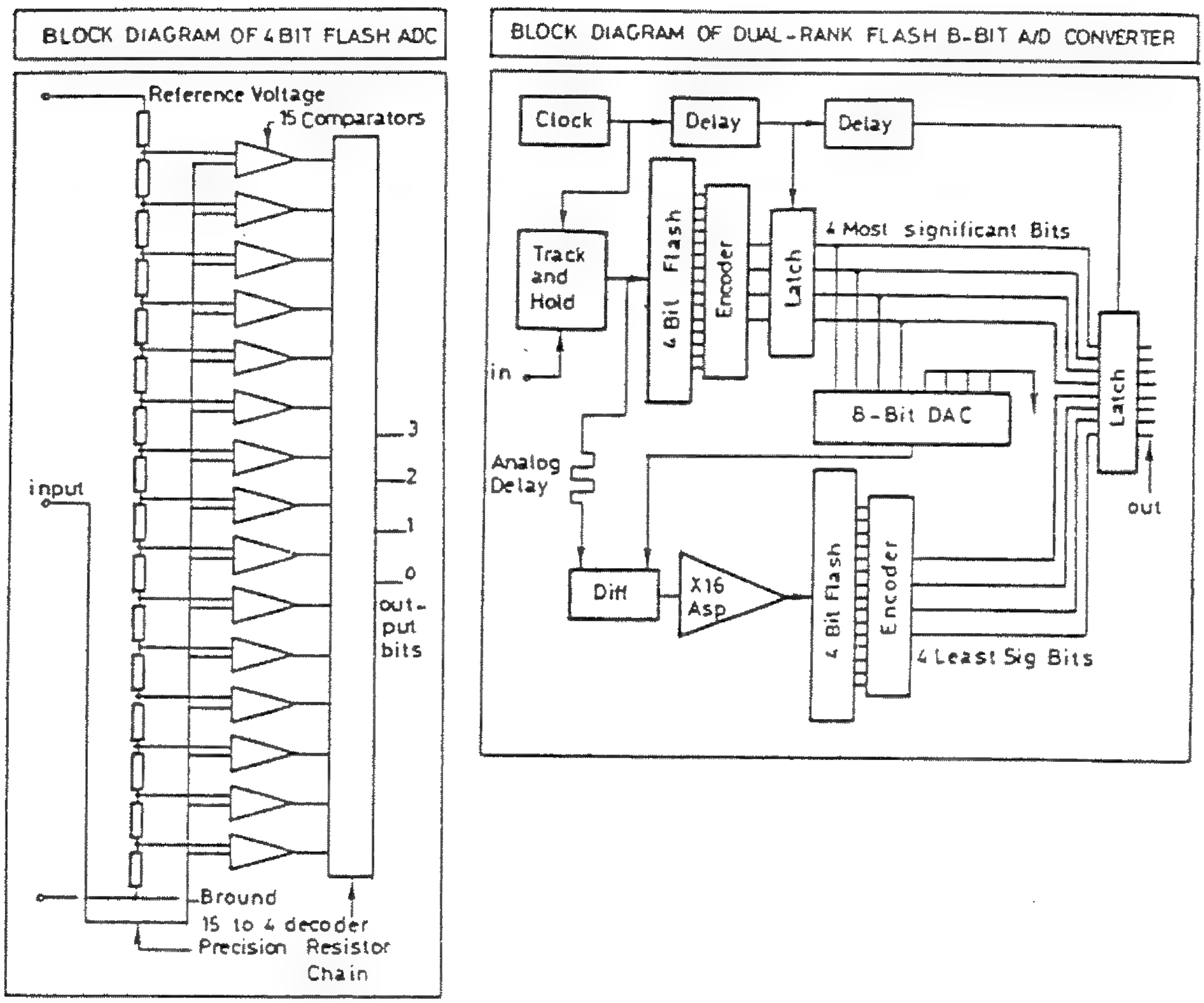
The 9400 uses dual-rank ADCs in the 9400-3 ADC boards, because the manufacture of a sufficiently fast and accurate ADC by other methods is impracticable. The successive approximation method is too slow, while an 8-bit flash ADC would require 255 fast comparators, as well as 255 accurate levels and a fast encoder to encode the result on to eight lines.

The dual-rank system is a compromise which takes advantage of the speed of the flash method, while restricting the size of each rank to a manageable level. The principle is shown in <1.3.4.1>, and although it looks fairly simple, its accurate implementation at high signal and sampling frequencies is far from easy.

The basic idea is to make a fast coarse conversion of the data, and then to reconvert the result with a DAC, the output of which is subtracted from the original signal to make the input for the second rank, which does the fine scale conversion. Finally, all the bits can be latched into a register. The 9400 uses a slightly more complicated system, merging a 3-bit ADC with a 6-bit ADC to make an 8-bit result (1.3.6); the redundancy allowing the use of a technique which greatly reduces the chance of large glitches ("fliers") at rank boundaries, namely, to make the range of the second ADC twice one step of the first ADC, instead of making it equal. Furthermore, the step size of the first rank ADC is passed on to the reference inputs of the second, so that compensation for drift can be made.

The function of the system can be understood by considering a simple example, a ramp input to the ADC. The first rank produces a coarse staircase waveform, which when subtracted from the input produces a set of smaller ramps from which the second rank makes the LSBs. The original and subtracted signals are shown in <1.3.5.3>.

For simplicity a 4+4 dual-rank ADC is shown here, rather than the 3+6=8 system used in the 9400. The functions of the 3+6 system are explained in the text.



PRINCIPLE OF DUAL-RANK ADC

Figure 1.3.4.1

1.3.4A Single-rank Flash ADC

The replacement of the dual-rank ADC by a single flash ADC simplifies the board significantly and eliminates several trims and numerous parts.

The current source Q4 shifts the output (± 800 mV) of HSH before going to buffer Q3/Q2, by - 800 mV, as required by HADC 77200 which has its upper reference at ground.

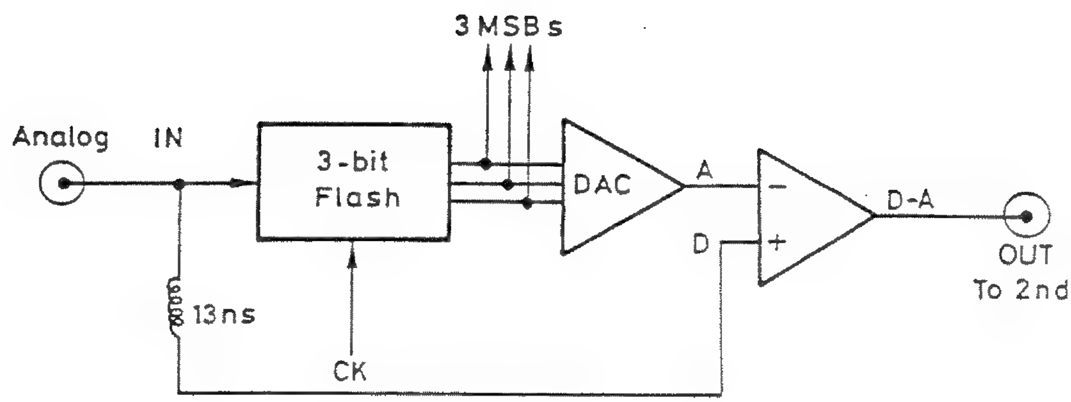
Trim P2 is for the adjustment of the ADC gain or range, respectively.

As the time delay through the single-rank ADC is less than that through the old dual-rank ADC, the digital delay B2 - C5 is used to bring the resulting signal into the correct timing for the next part of the circuit, so that the 9400-3 and 9400-3A boards can be interchanged.

1.3.5 First-rank HADAC

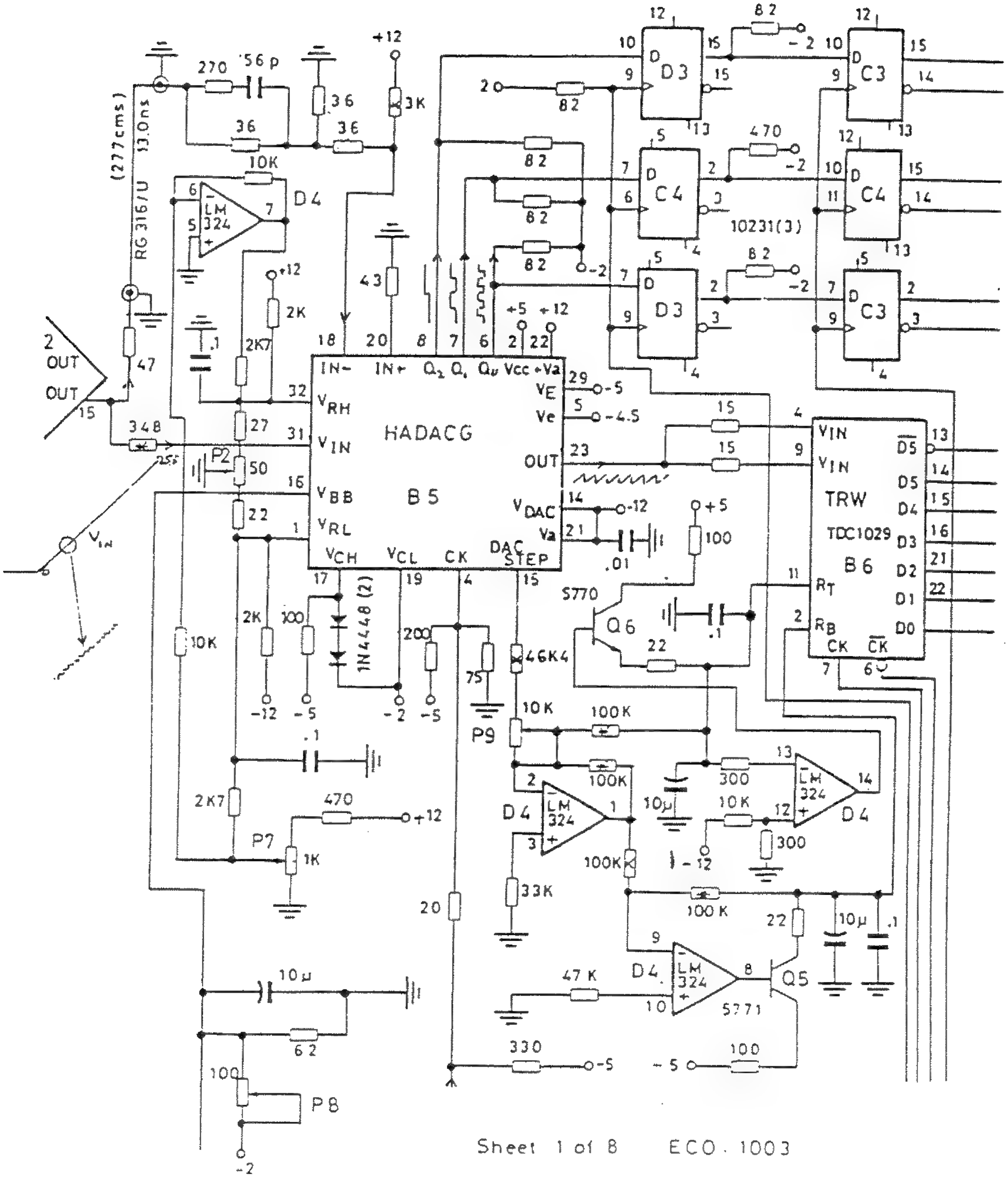
1.3.5.1 Introduction

This is a hybrid developed at LeCroy for the 9400. A simplified block diagram is shown in <1.3.5.1>, and the schematic of the HADAC and support circuits is shown in <1.3.5.2>. The analog signal from the hold hybrid enters at pin 31 and is flash converted by a 3-bit ADC, effectively to eight levels, seven of which are encoded into three digital bits which will become the three most significant bits of the final ADC output. The data are reconverted to analog in the usual dual rank way, the result being subtracted from the delayed input from the hold hybrid. The delay cable, being physically small, to encompass 13 ns in a small volume, has not quite the desired response at the highest frequencies, and a simple compensation network follows it. The result of the subtraction goes to the second-rank flash ADC.



HADAC BLOCK DIAGRAM

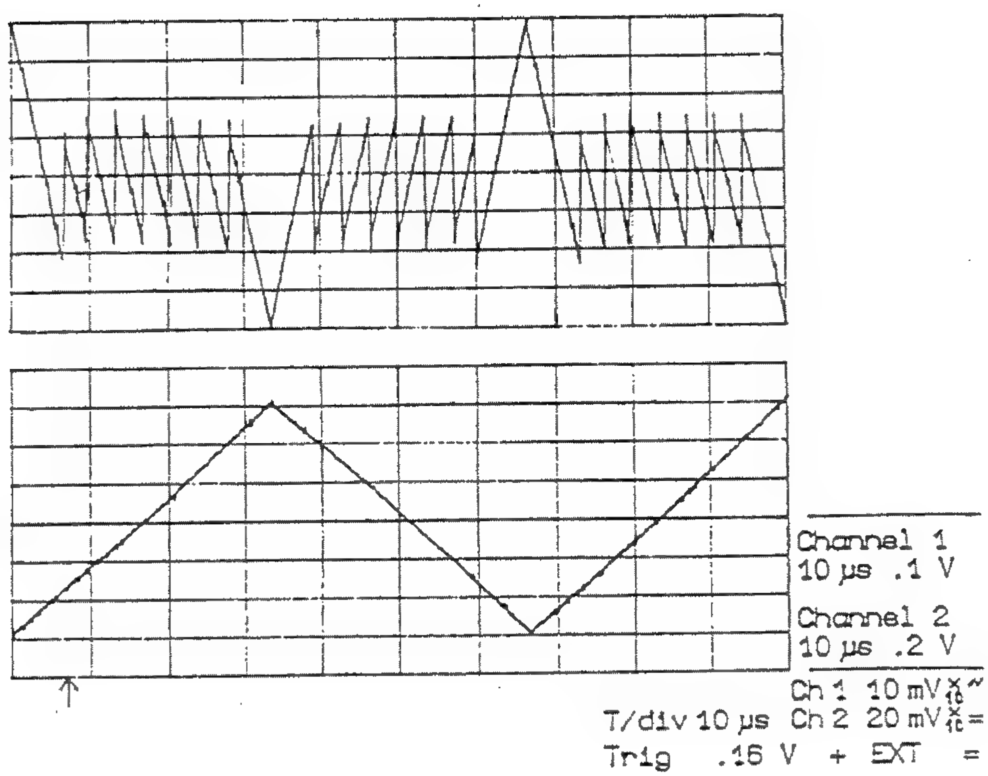
Figure 1.3.5.1



FIRST-RANK ADC AND SUPPORT CIRCUITS

Figure 1.3.5.2

This diagram shows the result of a moderate overdrive of the HADACG with a ramp waveform. The lower trace is the output of the HSH202, and the upper trace is the output at pin 23 of the HADACG. The signal frequency was about 1 kHz.



OUTPUTS OF HSH202 AND HADACG

Figure 1.3.5.3

1.3.5.2 First-rank Support Circuits

The support circuits and preset adjustments are as follows:

- First-rank discriminator range

  The discriminators of a dual-rank ADC can be thought of as being specified by levels set by a precision resistor chain, supplied from pins 1 and 32 of the HADAC. One op-amp of the LM324 quad, D4, with the two presets, P2,P7, sets the range and offset of the divider chain.

- Clock

  This enters from the delay line, at pin 4.

- DACStep

  An interesting feature of the HADACG is that one level is not used in the decoding tree - instead it is used to set the size of step needed by the second rank, using the network of three op-amps D4, LM324, and the preset P9. The digital output of the HADACG goes through the D-type flip-flops C3,C4,D3,D4, which latch them through with the right timing for addition with the second-rank bits.

The presets in this part of the board are to be adjusted only if the special test gear for the 9400-3 board is used.

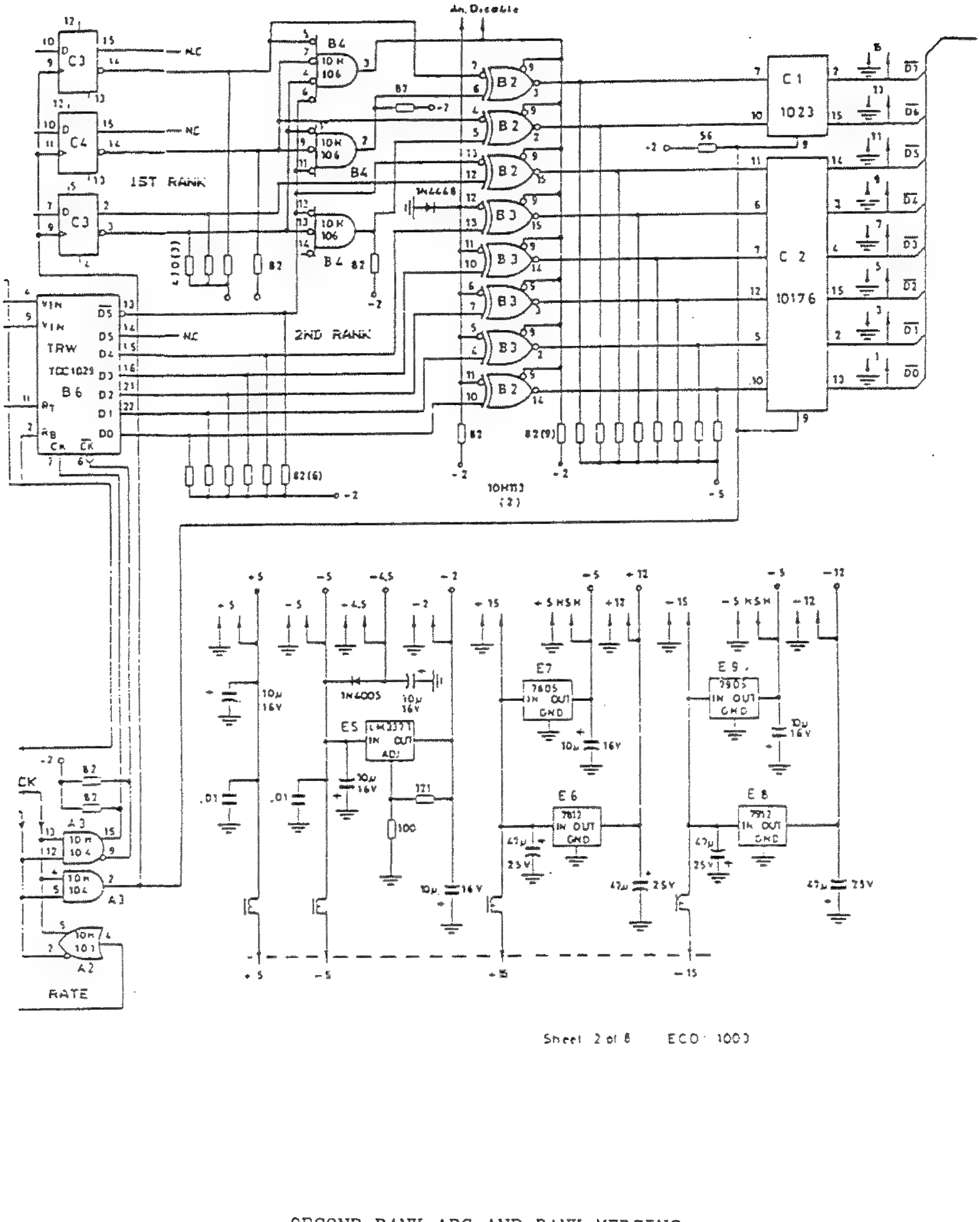
1.3.6 Second-rank ADC

This ADC is a 6-bit ADC made by TRW, a TDC1029, B6 on the schematic. There is little to say about this fairly standard ADC circuit, except the interesting way in which it is used in the LeCroy 9400. The combination of a 6-bit ADC with a 3-bit ADC is not only an interesting problem, but also an opportunity to use the redundancy to improve the performance of the system, for example to prevent the appearance of gross errors which sometimes appear when ranks are poorly combined. The range of the DAC output from the HADACG is set at half the span of the TRW ADC, and is centered on that span. Thus, small deviations in the HADAC output will not show as ADC bit errors, since the second-rank ADC will digitize that same range again. The two ranks finally come together in the exclusive ORs B2-3, which are all set at 1's in the event of overflow by the output from B4 pin 3. All these exclusive ORs can be disabled for test purposes, so that signals can be injected after the latches C1 and C2.

At the outputs of B2,B3 the eight bits appear together as a complete set for the first time, and are latched at C1 and C2 to provide a stable set of data for further processing.

The remainder of the 9400-3 board is devoted to multiplexing the data into the relatively slow banks of 6116 static RAM.

The schematic also shows the local voltage regulators on the 9400-3.

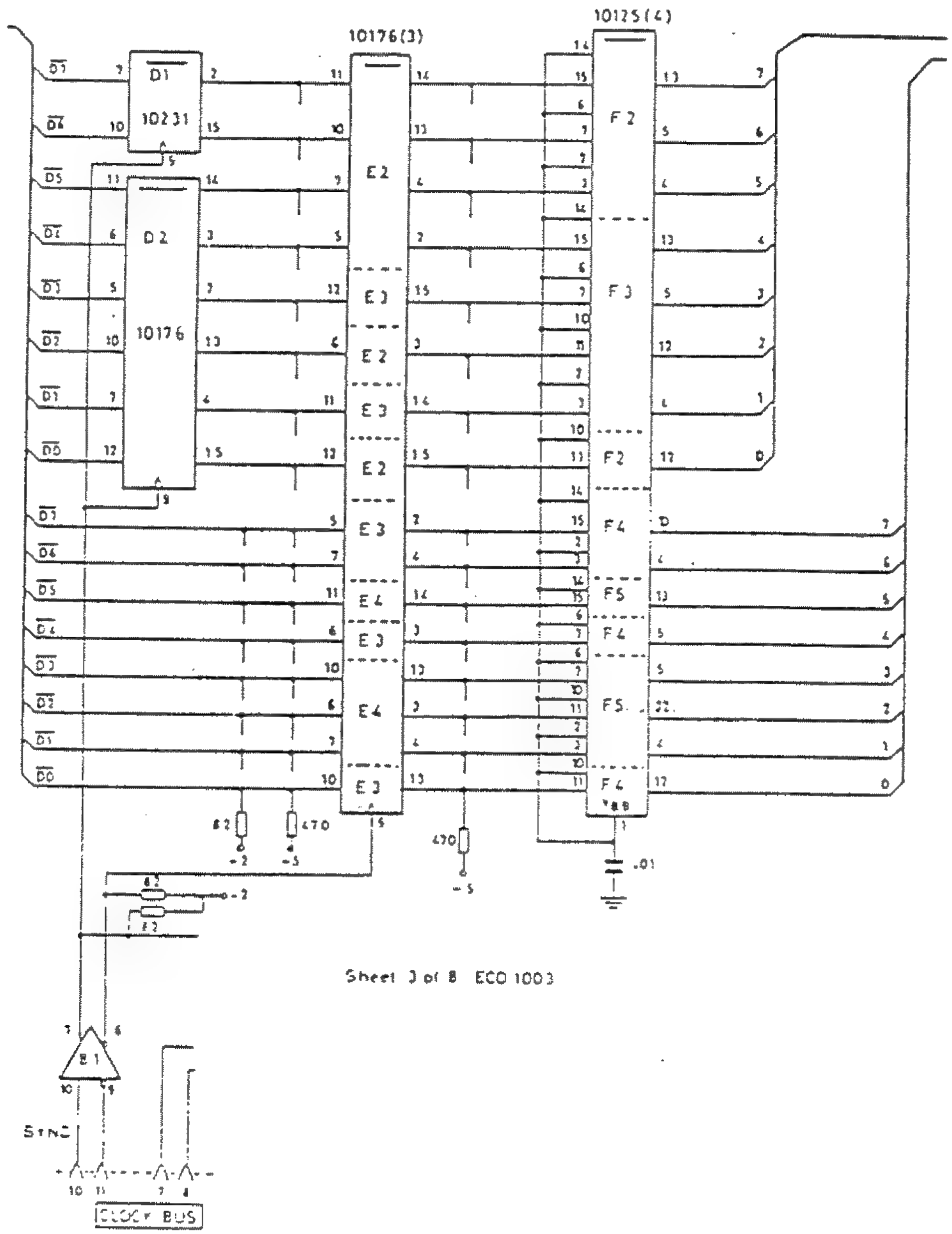


SECOND-RANK ADC AND RANK MERGING

Figure 1.3.6.1

1.3.7 Frequency Reduction and Conversion to TTL

The data appear at the outputs of C1 and C2 at a rate of 50 MHz or 100 MHz, depending on the settings of the 9400. The rate is halved by the next circuit, to enable further processing to be done in TTL. <1.3.7.1> The flip-flops D1 and D2 are clocked on alternate cycles only, so that the bank of flip-flops, E2-4, contains at any time two sets of data, from two consecutive samples. The pairs of samples are converted to TTL by the ECL-to-TTL converters F2-5.

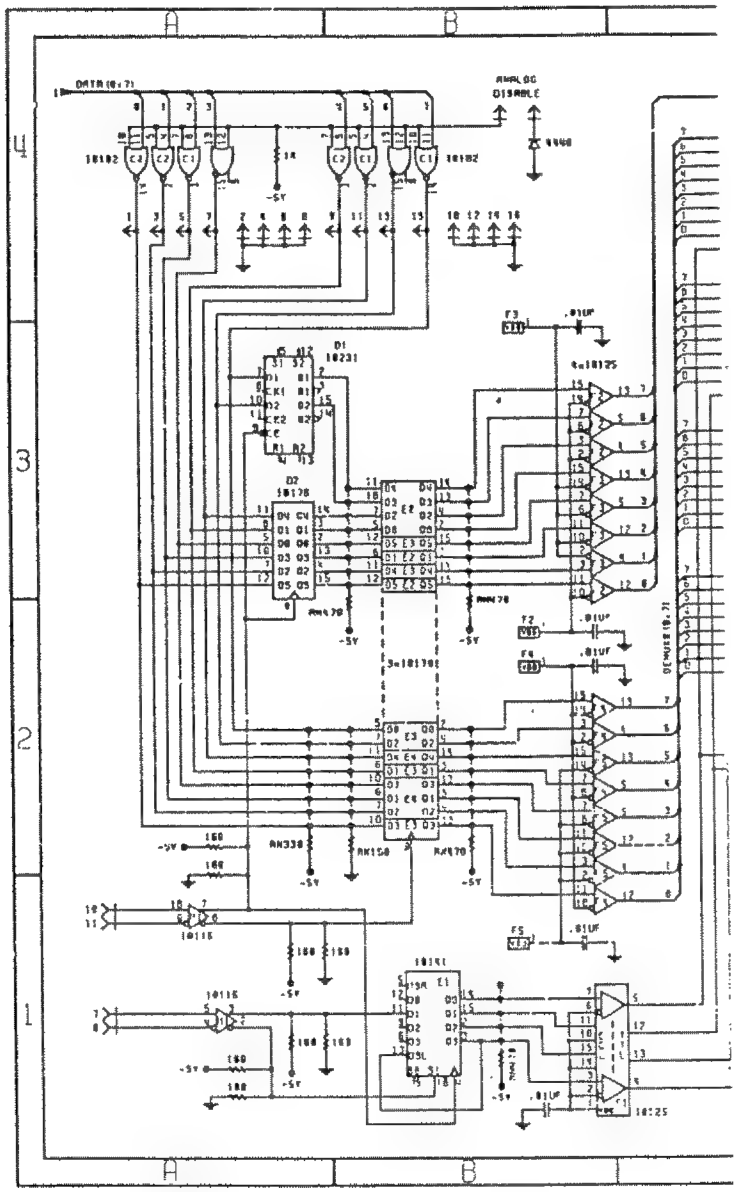


FREQUENCY REDUCTION AND ECL-TO-TTL

Figure 1.3.7.1

1.3.7A Frequency Reduction and ECL to TTL Conversion

From this point on the two types of board are functionally identical, but note that the analog disable function becomes ICs C1 and C2, and the ECL to TTL function is now labeled D1 to D2, see Figure 1.3.7A.



9400-3A Frequency Reduction and ECL to TTL

Figure 1.3.7.1A

1.3.8 Multiplexing the Data for the RAMs

The next step is to multiplex the data so as to present them to the 6116 static RAMs at an acceptable rate. The shift register E1 <1.3.9.1> clocked by CKR and provided with data by SYNC, produces four address lines which F1 converts to TTL. The buffers are use in the order:

G K H L I M J N, and their OE lines are controlled by ACQ and the the OE lines of the static RAMs.

These multiplexers feed the static RAMs and also a set of eight buffers which are connected to the buffered 68000 data bus BD <1.3.9.1>.

The relationship of CKR and SYNC is shown in <1.3.8.2>.

1.3.9 Memory Control and Direct ADC Read

The eight data streams from the multiplexer branch into two routes <1.3.9.1>, one to the static RAMs on the 9400-3 (1.3.10), and the other to the eight 74LS240 octal buffers, G5-N4, which in turn feed the two buffers L6 and M6, in the roll mode of the 9400, in which the ADC data are transferred directly to the 9400-1 BD bus (1.1.10) (1.1.11).

The eight buffers are always used for data transfer, either from the multiplexer in roll mode, or from the static RAMs in normal mode.

The output enables, OE, of the multiplexer, are controlled by the ACQ signal from the 9400-4 <1.3.9.1>, and the OE lines of the static RAMs, so that the multiplexer outputs data when the RAMs do not.

The 3-bit address word BA from the 9400-1 is decoded by F12 to eight lines, each of which enables one data stream. The order of the streams is shown in the diagrams.

The other control lines from the 9400-1 have the following functions:

- BRAS Buffered row address select
- BK6 From address space bank decoder (1.1.5)
- BWR Write read select
- BAS Address strobe
- XX DC level - high for Channel 1 - low for Channel 2
- YY DC level - high for Channel 2 - low for Channel 1
- BLDS Lower byte select (1.1.1.4)
- BUDS Upper byte select (1.1.1.4)

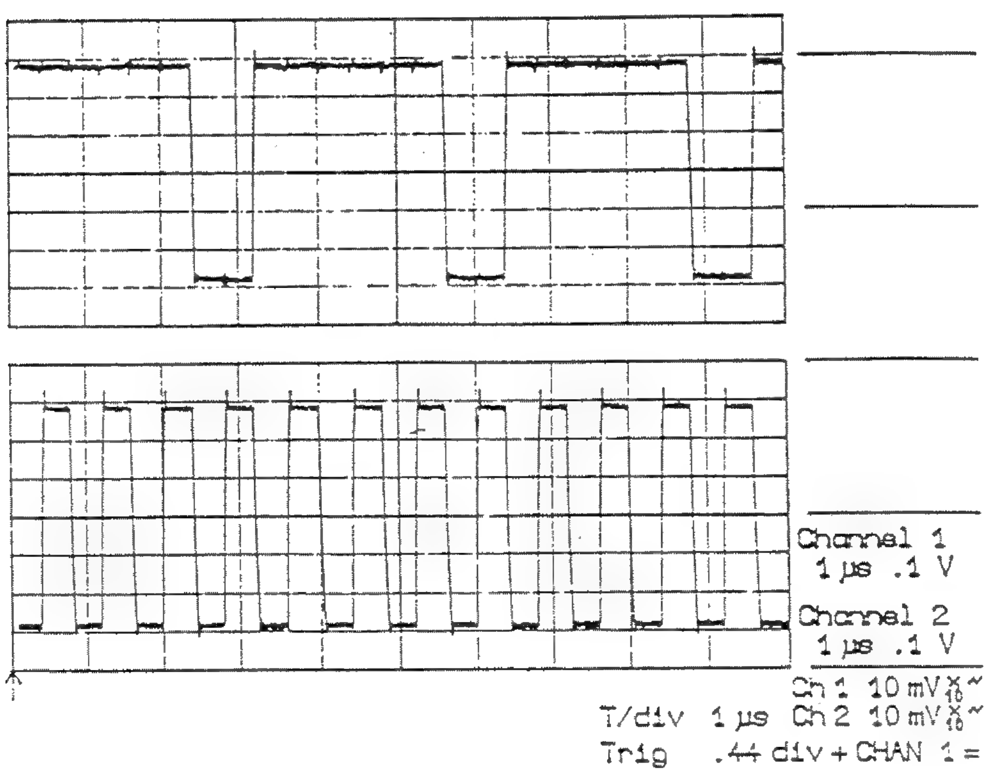
XX and YY are used with BLDS and BUDS to direct the data from DSO Channels 1 and 2 to the low and high byte addresses respectively, of the 68000 memory. This means that the two ADCs can be read simultaneously if necessary.

1.3.10 ADC Memory and Memory Read Buffer

The digitized data from the ADCs are written into two banks of eight 6116 static RAMs, the 6116 being a 2 kbyte memory <1.3.9.1>. The write enable signals are derived from G6, while the output enables are derived from the 9400-4 ACQ <1.4.15.1>. The ACQ signal and the two OE signals go to F13 <1.3.9.1>, which drives the OE pins of the multiplexers (1.3.8). In roll mode, the OE of the memories are disabled, and the data go straight from the multiplexer to the data buffers, while in normal mode, the OE of the memories are are enabled for data transfer from them to the 9400-1.

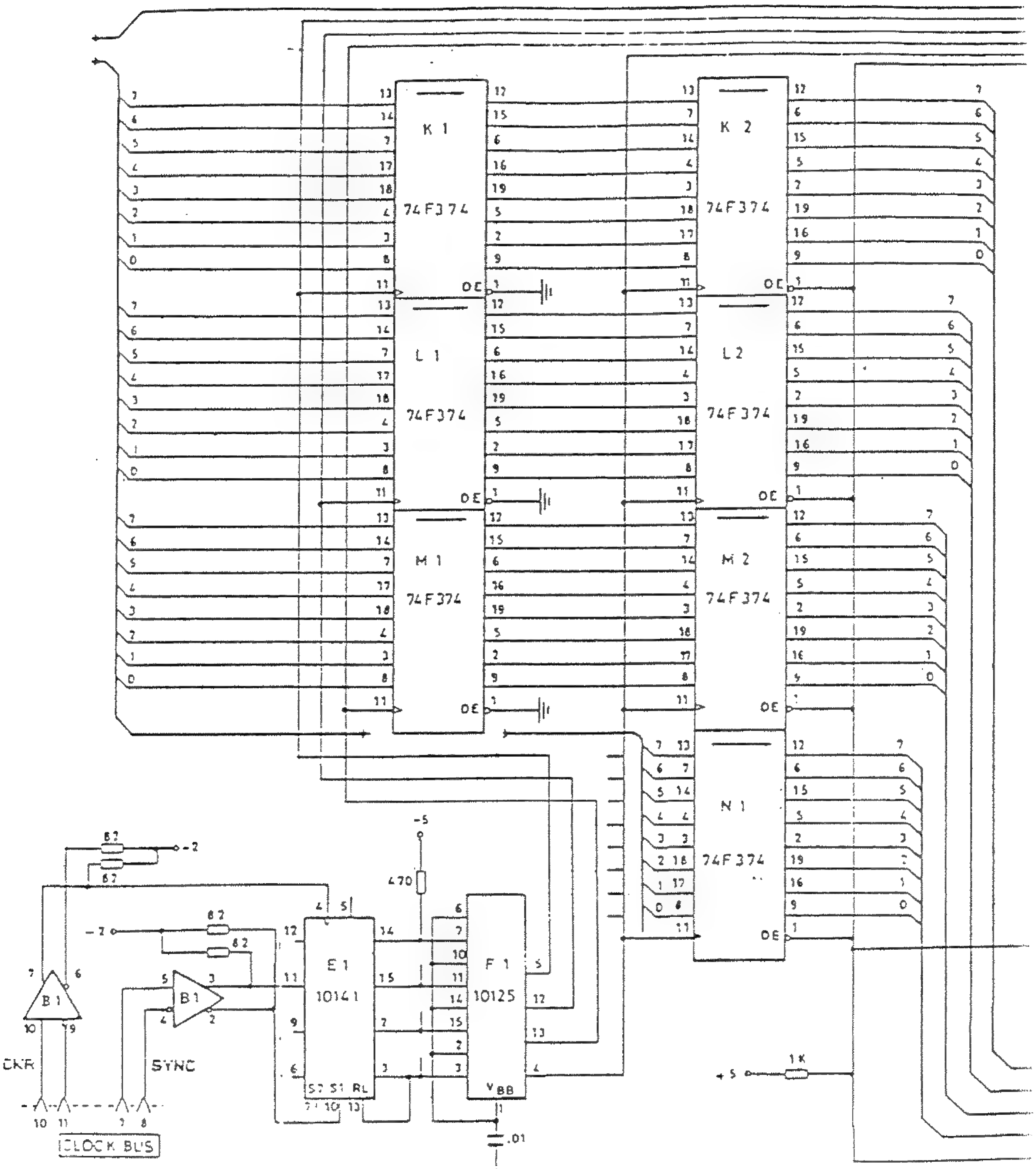
The addressing mode of the static RAMs is controlled by ACQ, via the three 74LS157 data selectors G7 H7 F14. During an acquisition the address lines of the RAMs are derived from the TA bus of the 9400-4 <1.4.15.1>, while at other times the addressing is from the 68000 BA bus.

The selection between the two banks of eight RAMs is made by W1 and W2, which control the write enables directly, and clock the 74F378 hex flip-flops via F10, in conjunction with BK6, BWR, and BAS.



SYNC (above) AND CKR SIGNALS ON CLOCK BUS

Figure 1.3.8.2



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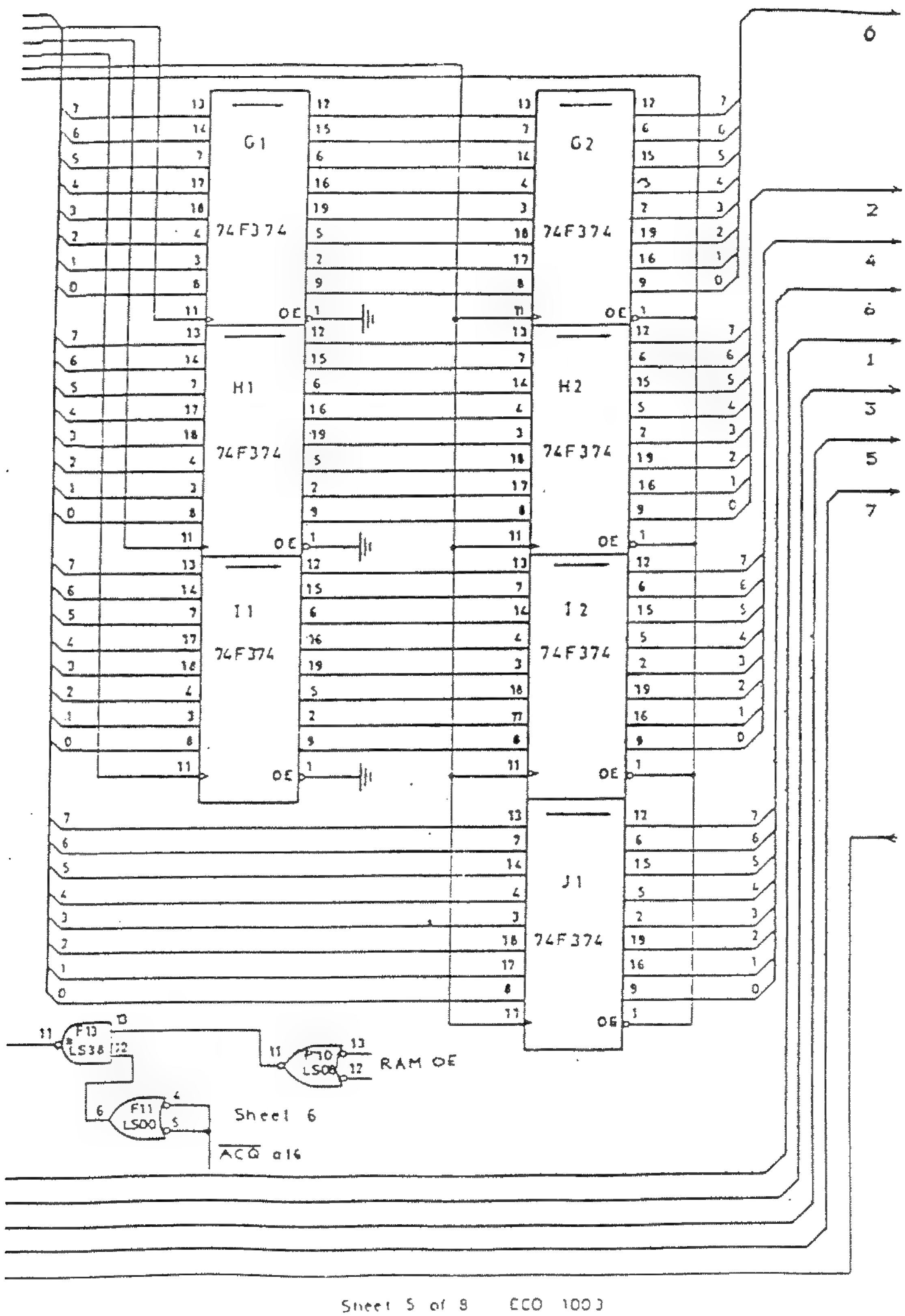
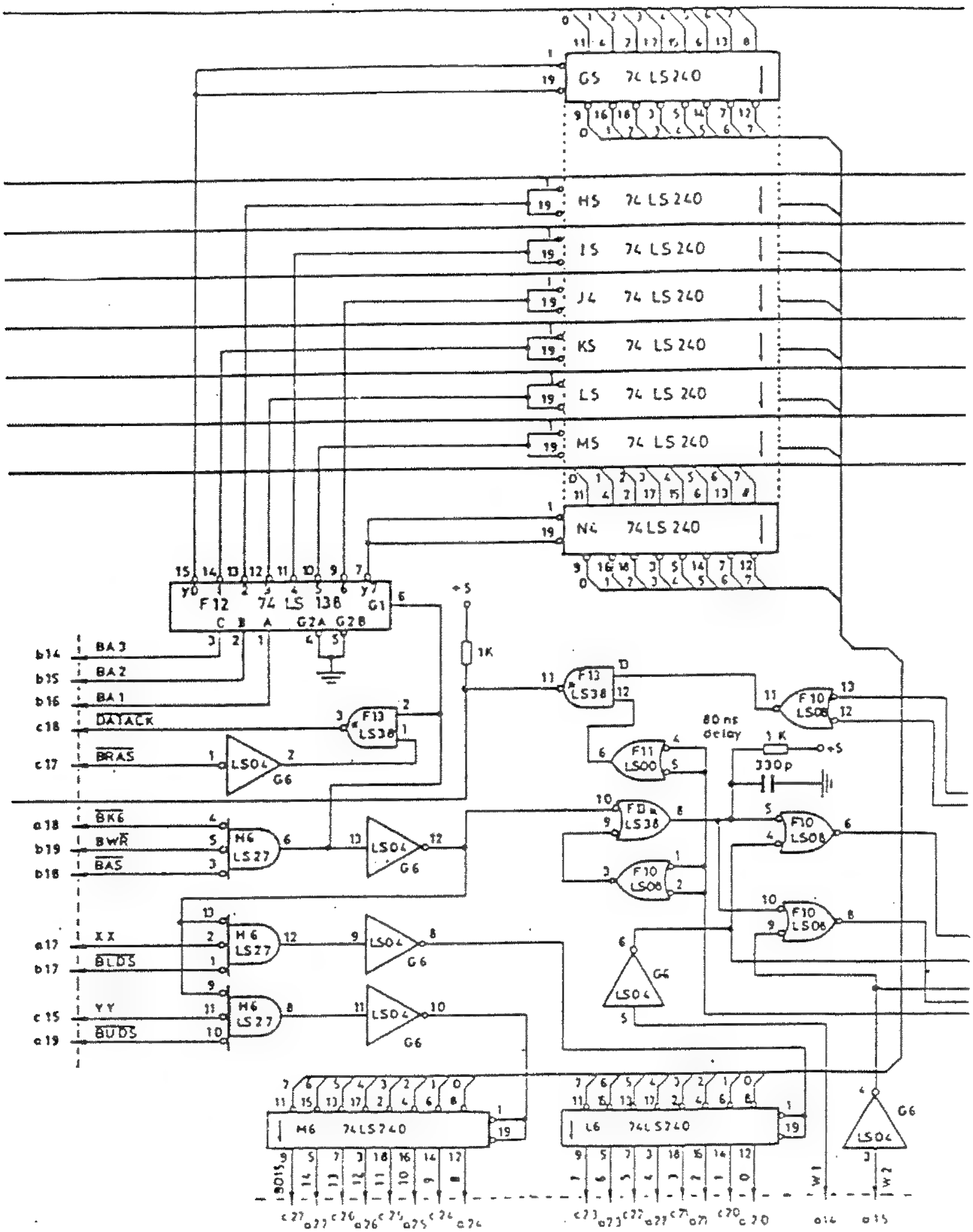
MULTIPLEXING THE DATA

Figure 1.3.9.1



MULTIPLEXING THE DATA

Figure 1.3.9.1



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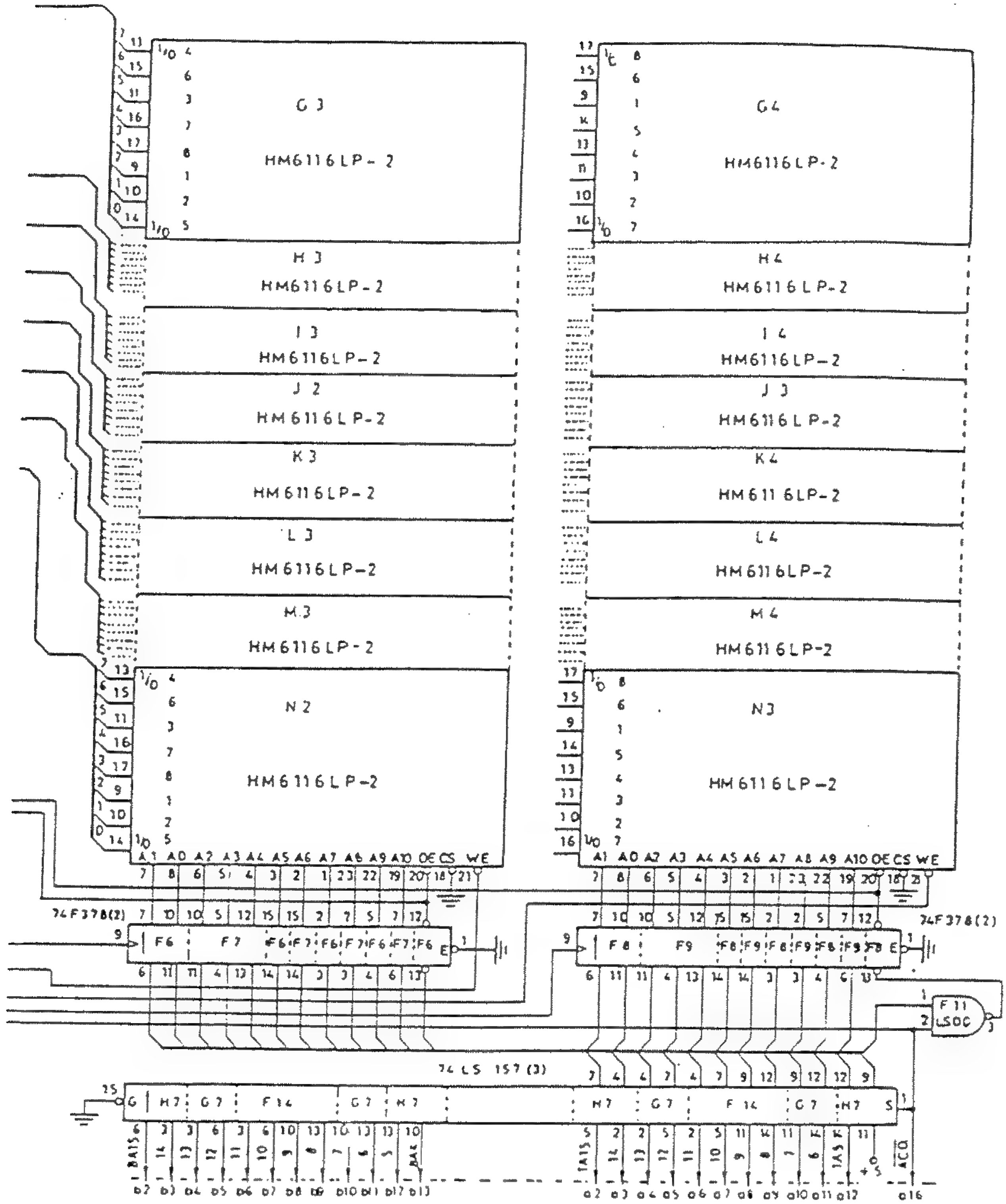

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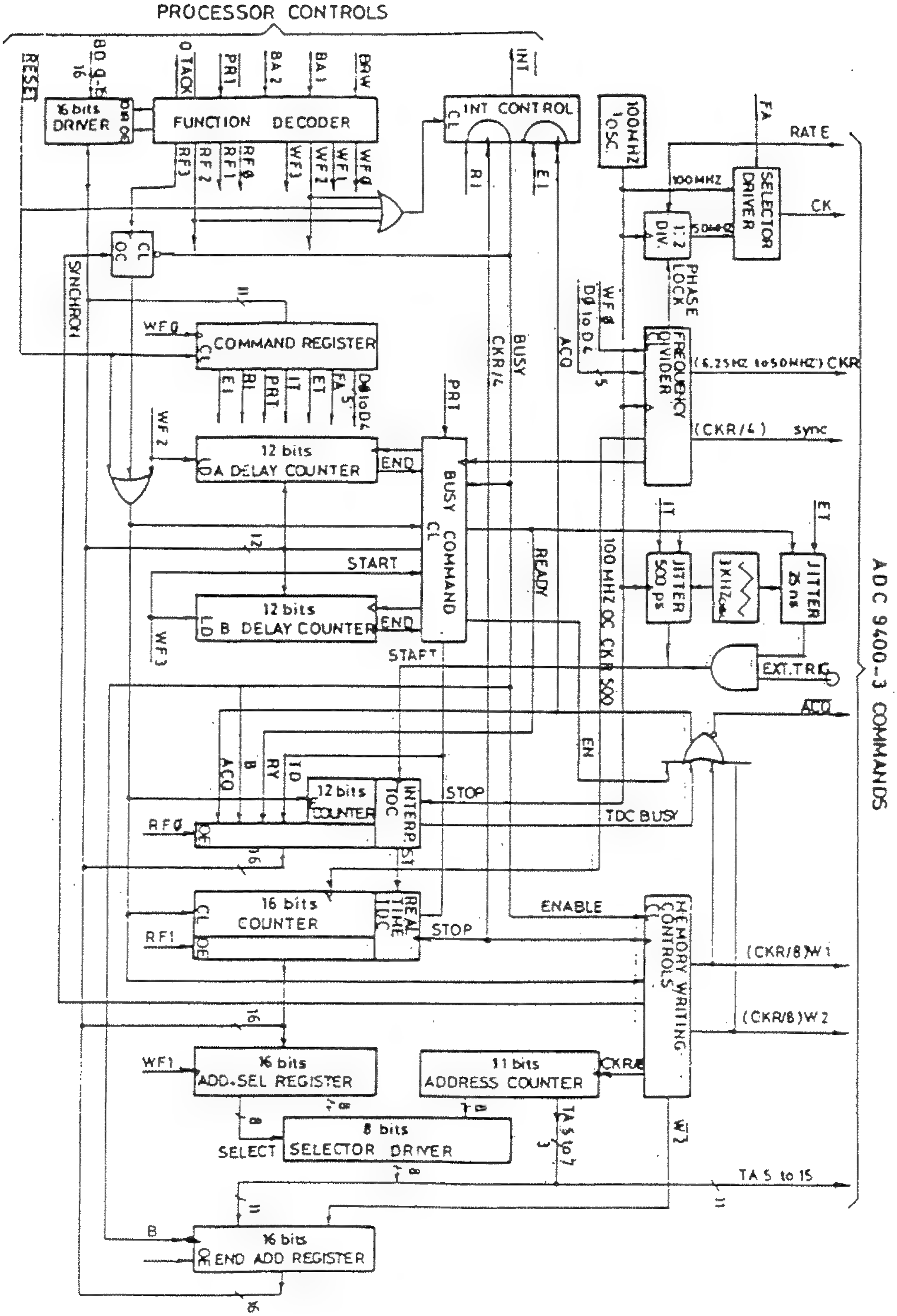
1.4 9400-4 TDC Board

Table of Contents



BLOCK DIAGRAM OF THE 9400-4 TDC BOARD

Figure 1.4.1.1

1.4.1 Introduction

The 9400-4 contains the precision timing circuits needed to clock the ADCs (1.3) and to time the external trigger with respect to the internal clock. It also contains the systems for managing the ADC memory addressing associated with post-trigger and pre-trigger operations. A block diagram <1.4.1.1> shows the functions of the 9400-4.

The main functions may be tabulated as follows:

- 100 MHz clock generator
- Clock management
- Clock distribution to:
  - ADC track-and-hold
  - ADC first and second ranks
  - ADC data latches
  - ADC multiplexers
  - ADC memory
- ADC memory address control
- Finding the trigger time relative to the sampling clock
- Finding the time to the next ADC write clock pulse
- Writing to ADC memory
- Loading end address of writing
- Trigger management

The 9400-4 is fitted in the right-most slot of the 9400-1 main board <5.0.2>, and carries a small bus, the 9400-8, at its top front corner, which carries the fast synchronizing pulses needed for the two 9400-3 ADC boards.

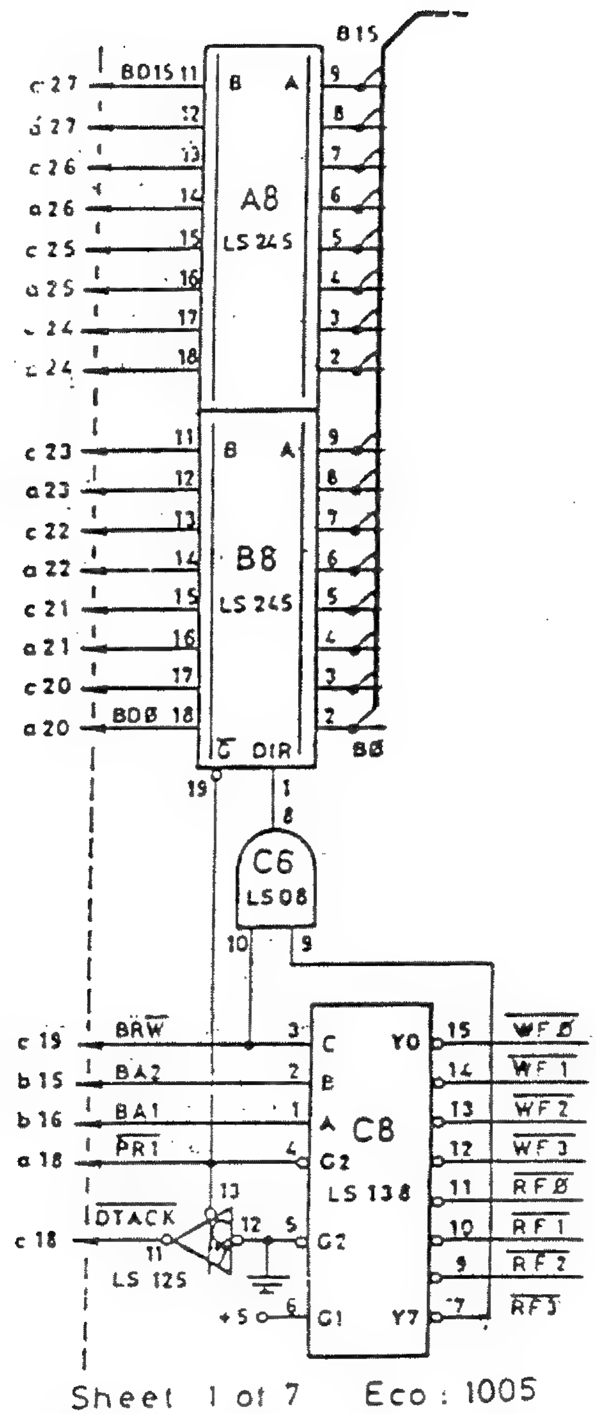
As an aid to understanding the functions of the 9400-4 and 9400-3 it may be useful to consider the memories as circular buffers in which writing or reading can continue past the end of the memory by recommencing at address 0. The 9400-4 at the end of an acquisition, loads the end address register with the last ADC memory address which was written. Note that in the post-trigger mode, the delay may be very long, so that the memory may be overwritten many times before the acquisition is terminated.

In order for the TDC board to control the acquisitions, it must respond to a trigger, and then, using the Interpolation TDC (ITDC), measure the time between this trigger and the next 100 MHz clock pulse. It is then necessary to measure a further time, to the next available memory write pulse, W1 or W2, using the RealTime TDC (RTTDC). Distinguish carefully between the measurement and conversion times of the ITDC; the conversion can be still in progress after the acquisition is all over, and is then the determining event for making the system ready for the 9400-1 to read the ADC memory.

The sequence of events for an acquisition depends on the mode, for example whether normal or roll, and pre- or post-trigger.

1.4.2 Bus Interface

The 9400-4 is interfaced to the BD0-15 data bus by the two 74LS245 octal tri-state transceivers A8, B8, controlled by PR1 (1.1.6) to the enable pin <1.4.2.1>, RF3 (1.4.6) and BRW (1.1.10) controlling direction.



BUS INTERFACE

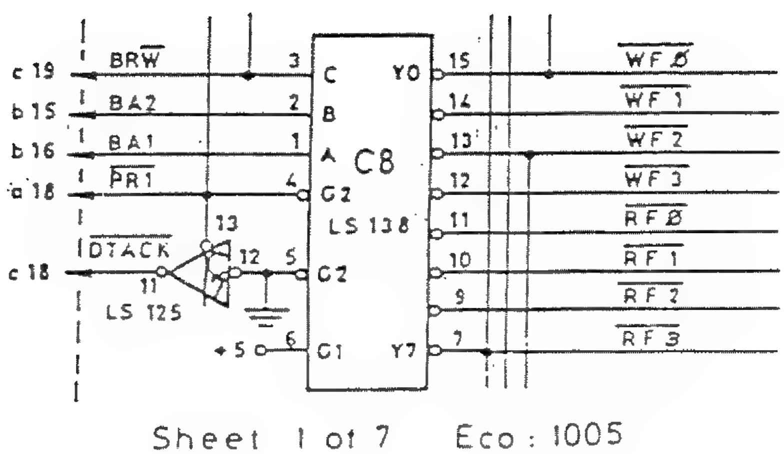
Figure 1.4.2.1

1.4.3 Function Decoder

The function decoder, based on a 74LS138 3-to-8 line decoder, C8, holds the current command to the 9400-4 board <1.4.3.1>. The eight functions comprise four for writing and four for reading:

- WF0 load the command register (1.4.4)
- WF1 load the ADC address register (1.4.14)
- WF2 load A Delay counter (1.4.10)
  general reset
- WF3 load B Delay counter (1.4.10)
  start acquisition

- RF0 read ITDC (1.4.12) and 4 state bits
- RF1 read RTTDC (1.4.13)
- RF2 read stop address from ADC memory address counter (1.4.16)
  reset INT5 (1.4.7) (1.1.7)
- RF3 stop acquisition
  reset both TDCs



FUNCTION DECODER

Figure 1.4.3.1

1.4.4 Command Register

The 16 bit bus B0-15 is latched in the 74LS273 octal D-type flip-flops A5, B5, forming the command register <1.4.4.1>. The commands and their functions are:

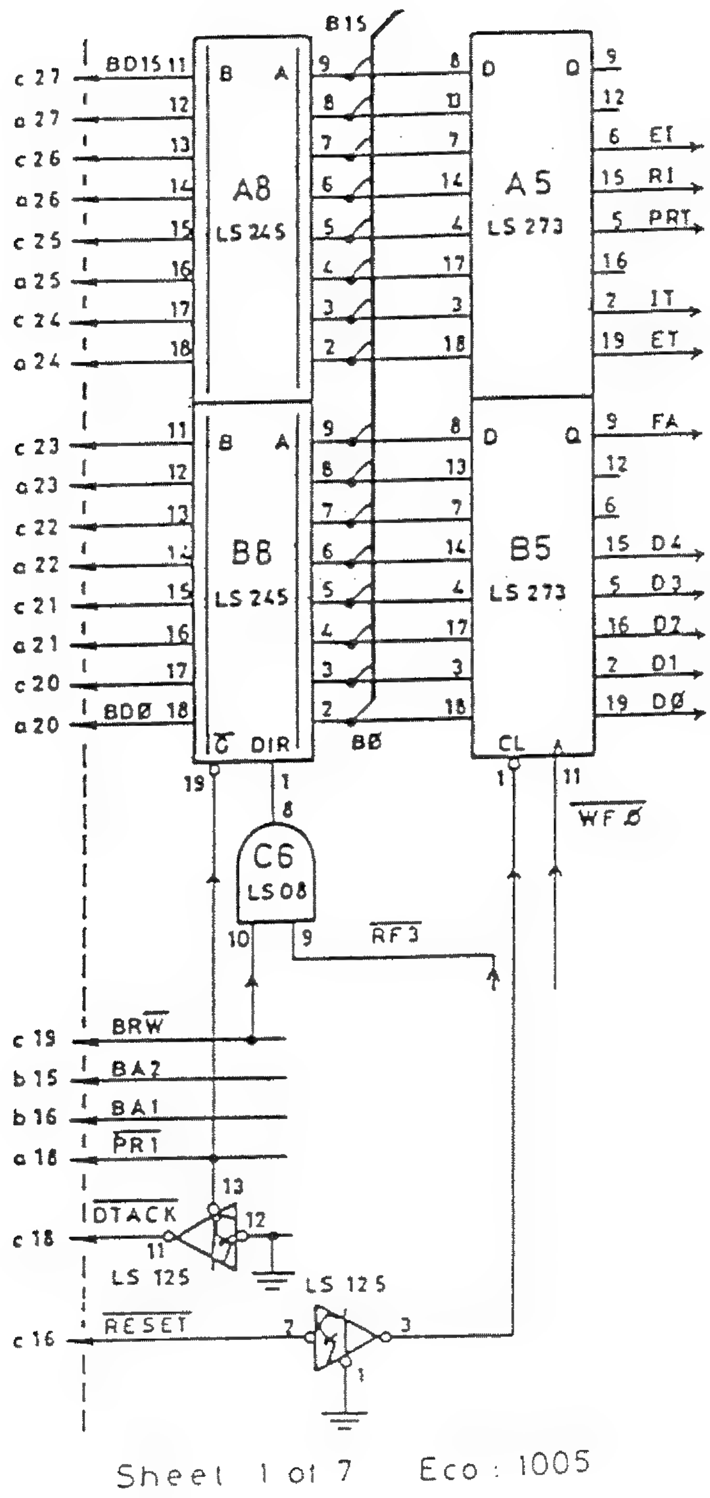
- EI end interrupt
  enable INT5 when ADC memories are full after end of acquisition AND ITDC (1.4.12) has completed conversion
- RI read interrupt
  enable INT5 for Roll mode when 8 bytes of ADC data are ready during acquisition
- PRT trigger mode:
  - PRT 0 for post-trigger
  - PRT 1 for pre-trigger

  controls mode of use of A and B delays (1.4.10) (1.4.11)
- ET select external trigger source, i.e., from 9400-1 EXT, INT, LINE (1.1.32)
- IT select internal trigger source, for random activation in the ITDC time zones near Tmin and Tmax
- FA select sampling rate - for the 9400-3 track-and-hold and flash ADC
  - 0 100 MHz sampling
  - 1 50 MHz sampling
- D select FS, FT and FM clock frequencies for the ADC memory write derived from 100 MHz clock
  - D0-1 control binary division (1.1.6)
  - D2-4 control decimal division (1.4.6)

  FS sampling frequency
  PS 1/FS

  FT counting frequency of RTTDC (1.4.13)
  PT 1/FT

  FM frequency of memory writing
  PM 1/FM

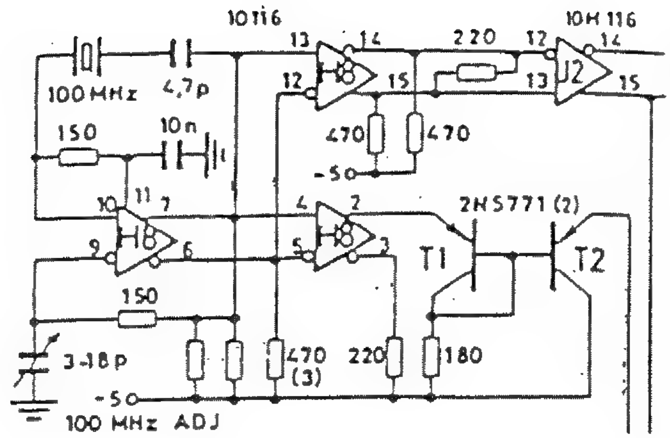


COMMAND REGISTER

Figure 1.4.4.1

1.4.5 Clock Generator

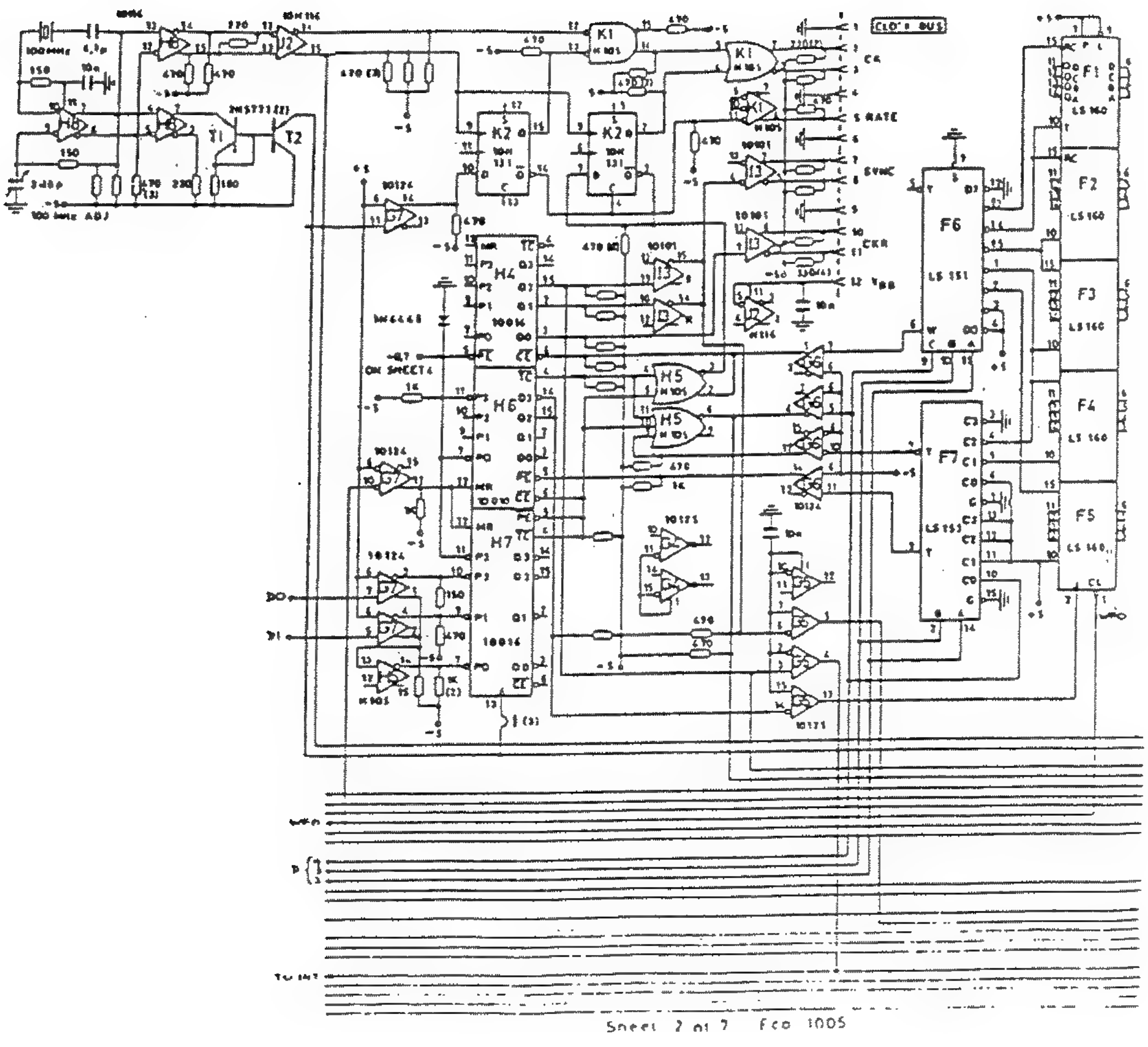
The clock generator and the faster parts of the clock system <1.4.5.1> use ECL circuits: for the parts which are relatively slow, TTL is used. The clock generator, H8, runs at 100 MHz. There is one preset control, a trim capacitor, which is adjusted during manufacture to ensure that the oscillator locks into the correct mode at power up.



CLOCK GENERATOR

Figure 1.4.5.1

The oscillator feeds two drivers, one of which, J2 and K1 <1.4.6.1>, drives the clock bus, sending synchronizing pulses to the 9400-3 ADC boards. The second driver, using T2, is heavily loaded by the long master clock track on the 9400-4. The sampling rate of the ADCs can be set at 100 Ms/s for the fastest time base speeds, and at 50 Ms/s for all other settings. No other rates are employed by the ADCs; for longer time base periods, only a fraction of the samples are sent to the ADC memories (1.3). The 50/100 Ms/s selection is made by FA (1.4.4).



DIVIDER CHAIN AND CLOCK BUS

Figure 1.4.6.1

1.4.6 Divider Chain and Clock Bus

Although the sampling rate of the ADCs takes only two values, because of the immense difficulties of optimizing all the ADC functions over a wide frequency range, the rate of writing to the ADC memories on the 9400-3 (1.3.9-10) can take many different values, corresponding to the time base settings.

The fast part of the divider chain, H7, is clocked at 100 MHz by the master clock. H7 is a binary counter whose division ratio can be set by the parallel inputs P0-2, using the lines D0-1 (1.4.4), to 1, 2, 4 or 8. H6 is a decade counter, and H4 a divide by 8.

Decades from 100 to 1000000 are made at the 74LS160 synchronous decade counters F1-5, selected by F6, a 74LS151 1-of-8 data selector/MUX, and F7, a 74LS153 dual 4-to-1 line selector/MUX, from the D2-4 lines (1.4.4), driving A,B, C(0) of F6 F7.

The divider circuit also provides the signals CKR and SYNC on the clock bus, which are used in the 9400-3 (1.3.7-8).

The relationships between the various clock frequencies is as follows (1.4.4 D):

CK — 50 MHz or 100 MHz, the frequency of sampling at the front end of the 9400-3.

CKR — Memory writing clock, which can run at many different rates. There are eight buffers on the 9400-3, feeding the static RAMs <1.3.10.1>, and one buffer and one memory is used at each transition of CKR, so that FM, the ADC memory writing frequency, is 1/4 CKR.

SYNC — Pulse train at FM <1.3.8.2>.

1.4.7 Interrupt Control

The 9400-4 board uses the fifth of the seven interrupt levels of the 68000 (1.1.7); the INT line <1.4.7.1> of the 9400-4 is connected to the INT5 line <1.1.9.1> <1.1.7.1>.

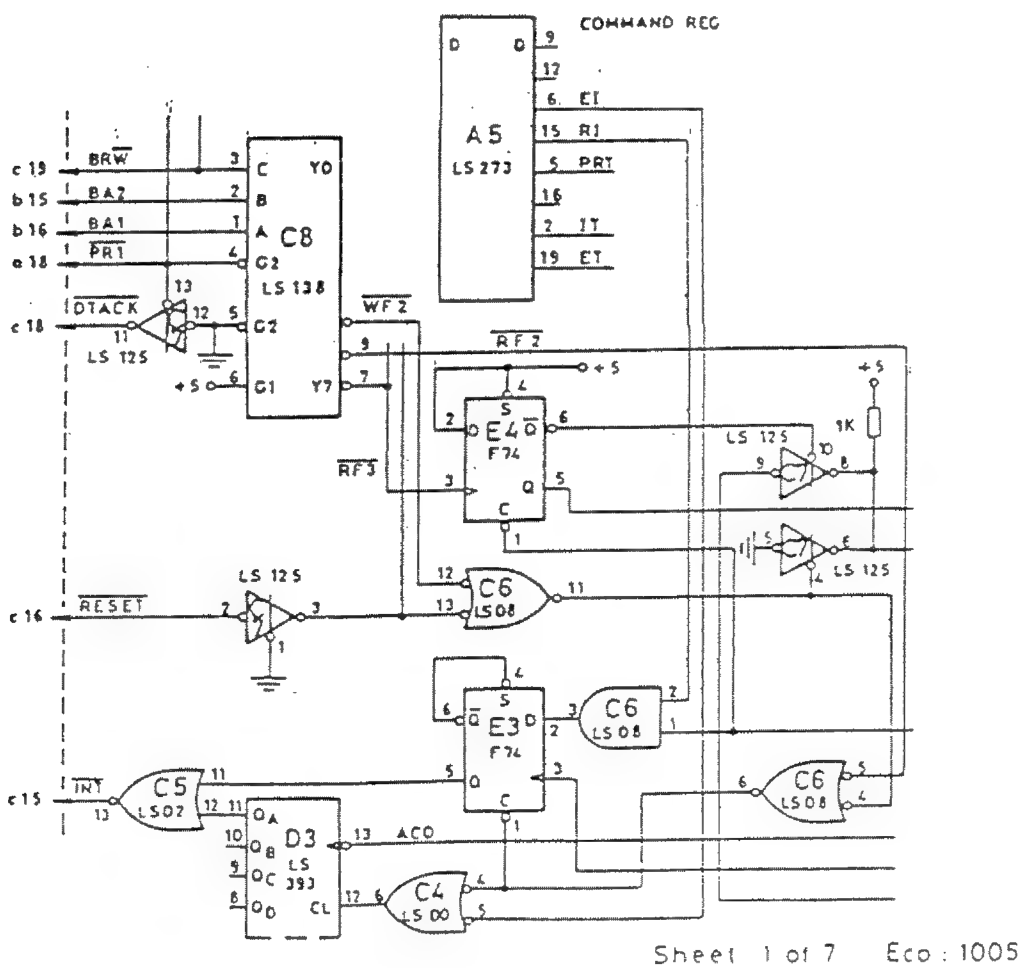
If EI=1, i.e., in normal mode and not roll mode, the 74LS393 4 bit binary counter D3 is clocked when ACQ goes low - when:

- Acquisition is complete
- AND ITDC conversion has been completed (1.4.12)

The 9400-1 can then read the ADC memory.

D3 clear is controlled by EI, depending on the current mode (1.4.4), or RF2 and general reset (1.4.3).

If RI=1, i.e., roll mode, the 74F74 D-type flip-flop E3 is clocked when FM goes high (frequency of memory writing), to instruct the 9400-1 to read one set of eight bytes from the 9400-3 (1.3.9). RF2 and general reset clears E3.



INTERRUPT CONTROLLER

Figure 1.4.7.1

1.4.8 Trigger system

Triggering can be accomplished in two ways:

- Externally, from outside the 9400-4, using signals NEG IN and POS IN from the 9400-1 (1.1.32). This is the normal mode of triggering.

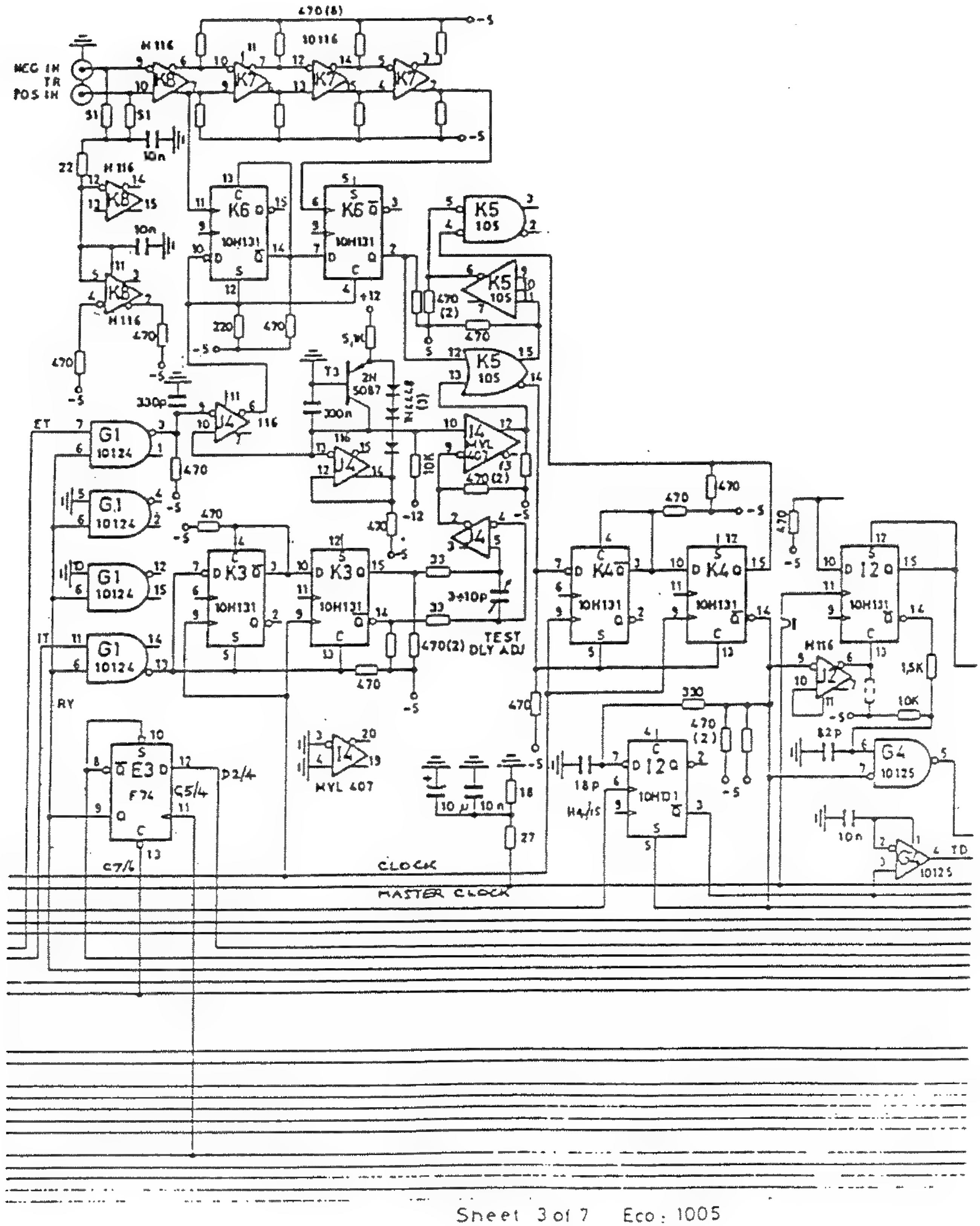
- Internally, from within the 9400-4. This mode is employed when calibration of the system is done.

Triggering is controlled by the commands ET and IT (1.4.4) in conjunction with the ready line E3 pin 9 <1.4.8.1>, which comes from pin 4 of D2 <1.4.10.1>, a 74LS157 2-to-1 line selector, the two inputs of which are derived from the BUSY line and the zero output of the A delay <1.4.10>. The selection is made by PRT (1.4.4), depending on whether pre- or post-trigger mode is required.

For external triggering the NEG IN and POS IN signals are buffered by K8 to the flip-flop K6, and to the delay K7, feeding the flip-flops K6, a system which overcomes the aliasing problem when the timing of the trigger and the enable coincide at K6. The signal then goes to K5 pin 5. The non-inverting output of K5 starts the ITDC, while the other output goes to the stop flip-flop K4 data, clocked by the 100 MHz master clock. At J4 pin 10 a jitter of 25 ns is introduced for use with Random Interleaved Sampling mode.

For internal triggering the enable from G1 feeds the flip-flops K3 which are clocked by the 100 MHz clock. Between K3 and J4 pins 4,5 is the Test delay adjust (2.4.4), which is used to adjust precisely the timing of the signal to the MVL407 I4. A jitter of 600 ps is introduced at pin 10 of the MVL407, and when the timing is precisely adjusted, the ITDC will count either 10 ns or 20 ns, which are its two extreme values, and this will show as two narrow peaks in a special test distribution in the DSO internal software <3.1.6.1>. Any error will make one peak wider than the other, because the center of the jitter range is not exactly at the point where K4 is enabled exactly at the clock transition. The point is that K4 will flip a whole clock period later when the jitter takes it past the critical time.

The selection of internal or external source is made by ET and IT at G1 in conjunction with the Ready line RY.



TRIGGER SYSTEM

Figure 1.4.8.1

1.4.9 Busy Command

The presence of a level on the Busy line, at E2 pin 9 <1.4.10.1>, shows that an acquisition is in progress, and that the ADC memories are being filled with digitized data.

E2 is clocked from G5 pin 4, at FM, the frequency of memory writing <1.4.6.1>, and gets data from E2 pin 5, EN, clocked by WF3 (1.4.3).

1.4.10 A and B delay in Post-trigger Mode, PRT=0

The A and B counters <1.4.10.1> are both based on sets of three 74LS191 synchronous up/down counters, used in count down mode. The data are loaded from the 16 bit B bus <1.4.2.1> which is buffered to the 68000 BD bus (1.1.10).

In post-trigger mode, all the data are to be acquired after the trigger, and to obtain long post-trigger delays, the A and B delays are coupled together to give a large dynamic range.

After the receipt of WF3, and which loads data into the B delay (1.4.3) the trigger is freed for receipt of an input. When a trigger is detected, the acquisition starts, and AB start to count down; when zero is reached, the acquisition is complete.

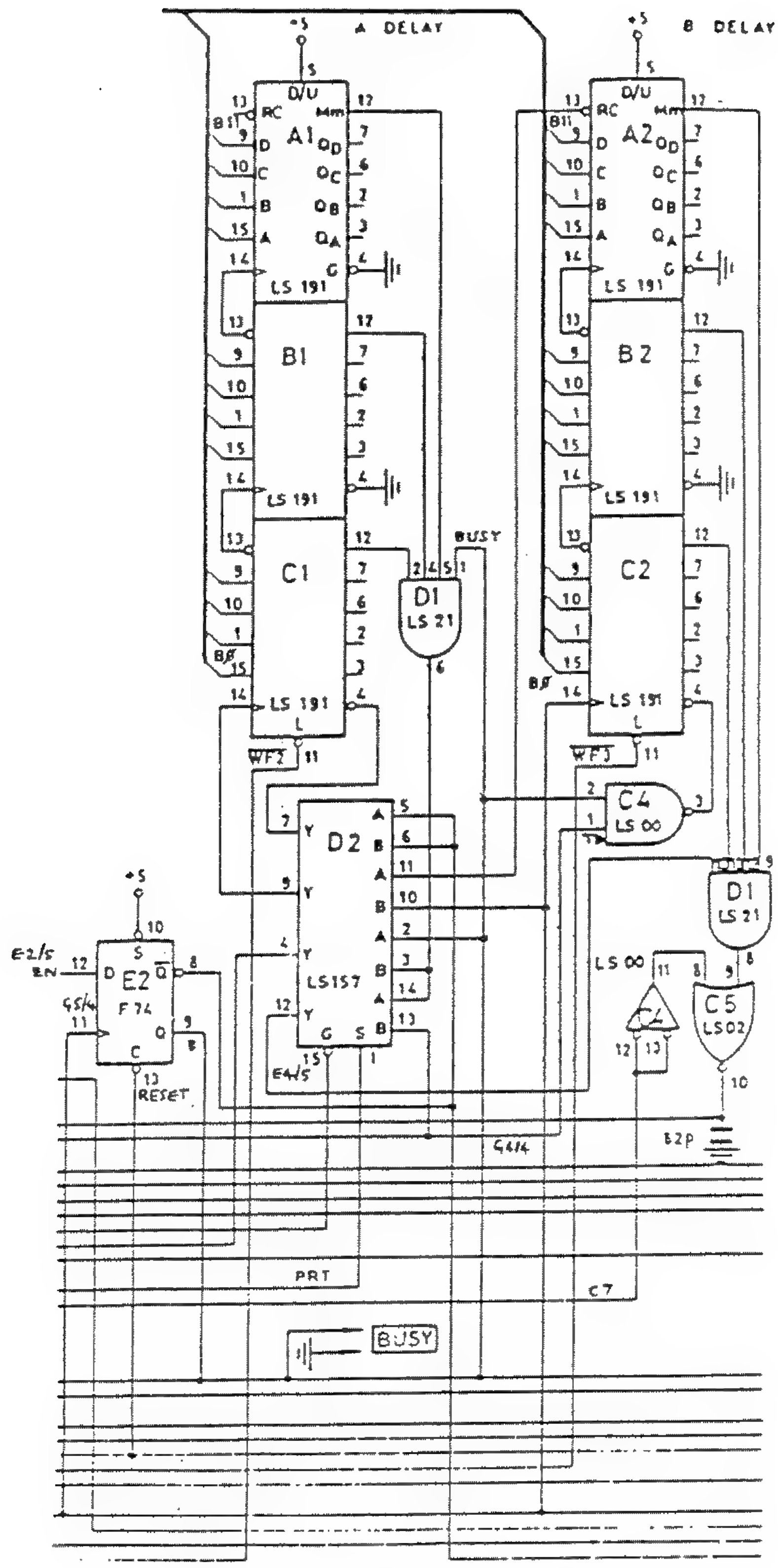
The value loaded in the AB counter must not be less than the length, 32 K, of the ADC memory, otherwise there would not be a complete set of post-trigger data in the memory.

In post-trigger mode, upon receipt of WF3, ACQ is set, followed by Busy, B, on the next clock pulse, and Ready, RD, on the next after that. When the next trigger arrives, the ITDC and RTTDC are activated (1.4.12-13), and then the AB delay is started. At the end of this delay, the acquisition stops.

1.4.11 A and B Delays in Pre-trigger Mode, PRT=1

In this mode, counter A holds the pre-trigger value, and functions as a hold off, while counter B holds the post-trigger value. Clearly the sum of the A and B data must be equal to the length, 32 K, of the ADC memories.

In pre-trigger mode, WF3 initiates an acquisition, at which time ACQ is set. The Busy, B, is set on the next clock pulse, and the A delay starts to count down. At the end of the A delay, Ready, RD, is set, and a trigger is now acceptable. When it arrives, the ITDC and RTTDC are used as described in (1.4.12-13) and the B delay begins. At the end of the B delay the acquisition stops.



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A DELAY AND B DELAY

Figure 1.4.10.1 A

1.4.12 The Interpolation TDC (ITDC)

This circuit <1.4.12.1> has the delicate task of timing the trigger with respect to the clock of the 9400-4, with sufficient accuracy to allow the creation of meaningful interleaved samples at an effective frequency of 5 GHz.

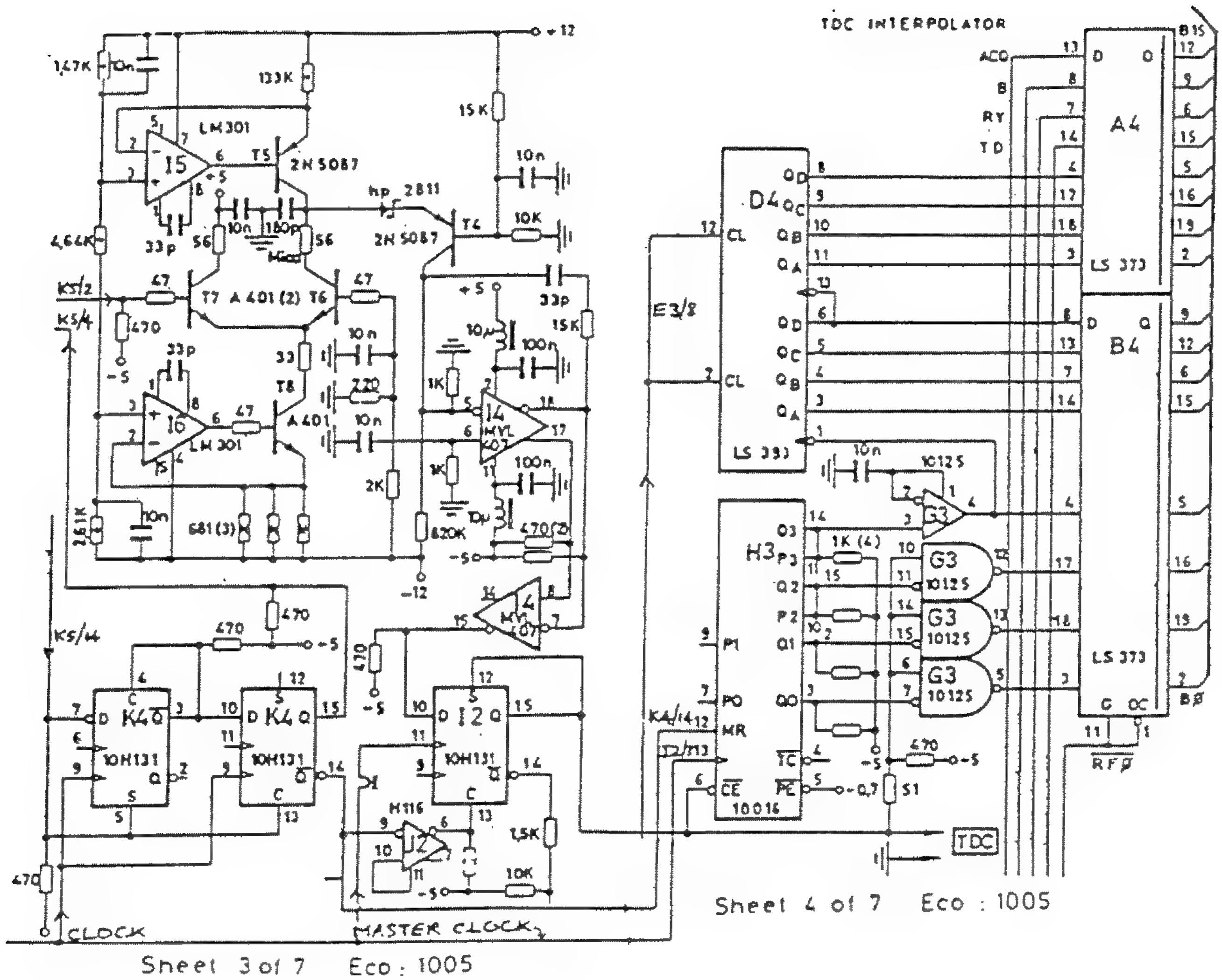
The circuit is based on the charging and discharging of a capacitor by means of an accurate constant current source and sink. By making the discharge current 1000 times as great as the charge current, small time intervals generate much larger ones which are relatively easy to measure. The counting time is so long that the ITDC may not be free when an acquisition is in other respects complete.

The measuring period is started by K6 pin 2 or I4 pin 12 and stopped by K4 pin 15. The counting period then begins, during which the counter (see below) is in operation.

The charging current is supplied by a source based on T8 and I6, the current being defined by a 227 ohm resistor. The discharge is done by T5, which with I5 forms a second constant current device. The more powerful source can be switched by K5, which uses T7 to take all the current from T8, instead of letting it pass through T6 from the 180 pF capacitor.

The capacitor potential is detected by the top section of I4, a LeCroy MVL407 discriminator, which sends data to the ECL flip-flop I2, via the lower part of I4. The arrival time of the data at I2 therefore gives a magnified representation of the original period during which the capacitor was charged.

The MVL407 supplies data to flip-flop I2, which enables the 10016 ECL binary counter H3, counting the fast LSBs, and buffered by the ECL-TTL converter G3, and the 74LS393 dual 4 bit binary counter D4, which is buffered to the B bus (1.4.2) by the two 74LS373 octal D-type latches A4, B4.



INTERPOLATION TDC (ITDC)

Figure 1.4.12.1

1.4.13 Realtime TDC (RTTDC)

The RTTDC counts, at the frequency FT, the time between the end of the ITDC (1.4.12) measuring period, and the next W1 or W2 ADC memory writing clock pulse. It is started by K4 pin 14, and is stopped by I2 pin 3.

This TDC employs the ECL binary counter H2, buffered by the ECL-TTL converter G2, for the fast LSBs, and the two 74LS393 dual 4 bit binary counters D3, C3, for the slower bits, buffered to the B bus by the 74LS244 octal buffers B3, A3.

1.4.14 ADC Memory Writing Controls

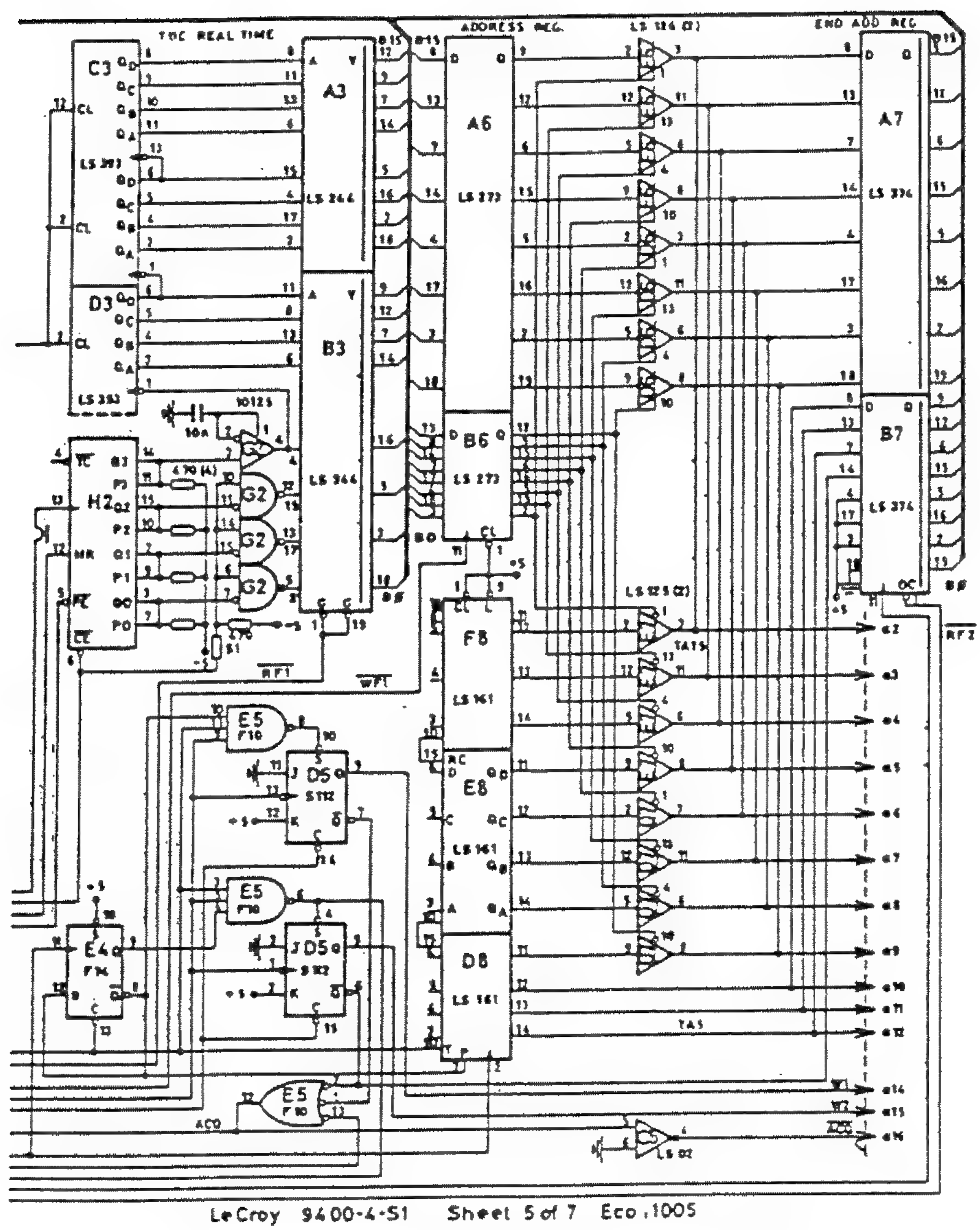
The ADC memories (1.3.10) are addressed by the 9400-4, when data are to be written which keeps track of the current address, address to stop writing (End address), writing rate, CKR, etc. These functions can be seen on the block diagram <1.4.1.1> and in <1.4.15.1>.

In addition to the address lines, the 9400-4 sends:

- W1 write enable 6116 bank 1 on 9400-3 (1.3.9)
- W2 write enable 6116 bank 2 on 9400-3 (1.3.9)
- ACQ write enable of 9400-3 ADC memories

W1 and W2 are used to send alternate batches of eight bytes to the first and second ADC memory bank respectively.

See (1.3.9-10) for subsequent processing of these lines.



ADC MEMORY WRITING CONTROLS

Figure 1.4.15.1

1.4.15 Address and Select Register

This is the pair of 74LS273 octal D-type flip-flops, A6 B6, clocked by WF1 (1.4.3), A6 selecting the address for segmentation of the ADC memory, and B6 selecting the address.

1.4.16 Address Counter

This is the set of three 74LS161 4 bit counters D-F8, clocked by G5 pin 4 (1.4.6) at the frequency FM/2.

1.4.17.1 ADC Memory Address Selector Driver

This circuit (D-E)(6-7) uses two pairs of buffers, 74LS125 and 74LS126, with opposite enable polarities, to select data from the address counter, D8 - F8, or from the Address and select register, A6.

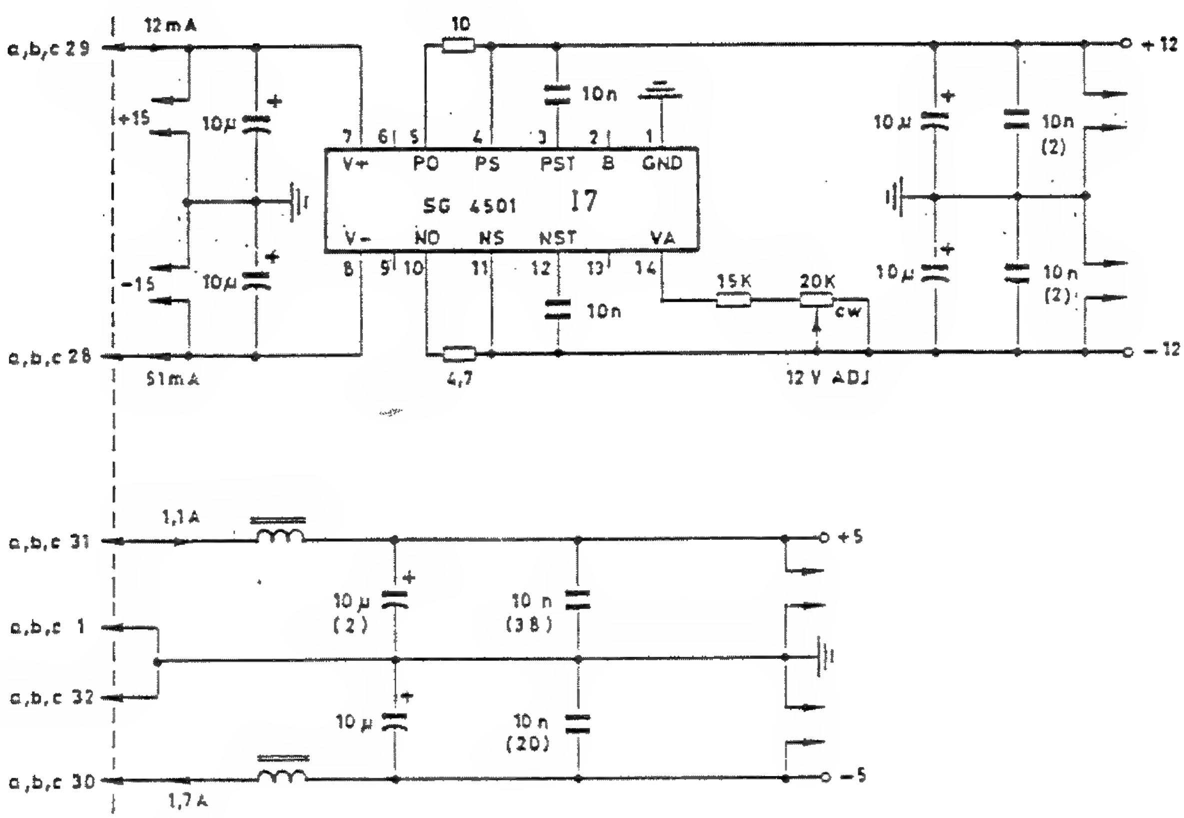
1.4.18 End Address Register

The end address register is used at the end of an acquisition to store the ADC memory address at which writing stopped.

This register (END ADD REG) uses two 74LS374 octal D-type flip-flops, A-B7, whose outputs to the B bus are controlled by RF2; they are clocked by the end of enable from E2 pin 8 <1.4.10.1>.

1.4.19 Power Supplies

The 9400-4 takes the standard 9400 power lines from the slot, and also creates its own stabilized +12 V and -12 V supplies <1.4.19.1> for the precison analog circuits. These supplies use the SG4501 tracking regulator.



TDC POWER SUPPLIES

Figure 1.4.19.1

These diagrams show timings of the main functions of the 9400-4 for the following circumstances:

- showing 9400-4 functions:

    - <1.4.20.1> 100 Ms/s post-trigger mode
    - <1.4.20.2> 100 Ms/s pre-trigger mode

- showing clock, sync and memory timings:

    - <1.4.20.3> 100 Ms/s post-trigger mode
    - <1.4.20.4> 100 Ms/s pre-trigger mode

- showing ADC memory addressing and loading:

    - <1.4.20.1> 100 Ms/s pre-trigger mode
    - <1.4.20.6> 50 Ms/s pre-trigger mode

1.5 9400-5 Front Panel Board

Table of Contents

1.5 Front Panel Board 9400-5

1.5.1 Introduction

This board carries all the frequently used controls of the 9400 DSO. There are four main parts of the circuit <1.5.1.1>:

- Potentiometers
- Push button switches
- Rotary switches
- LED indicators

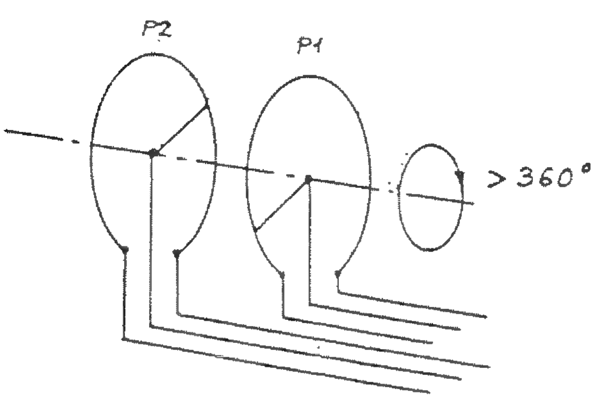
Note that the line power switch at the lower right corner of the front panel is not a part of this section: it is fed from the 9400-9B board on the rear panel (1.9). Section 1.5 should be read in conjunction with (1.1.21).

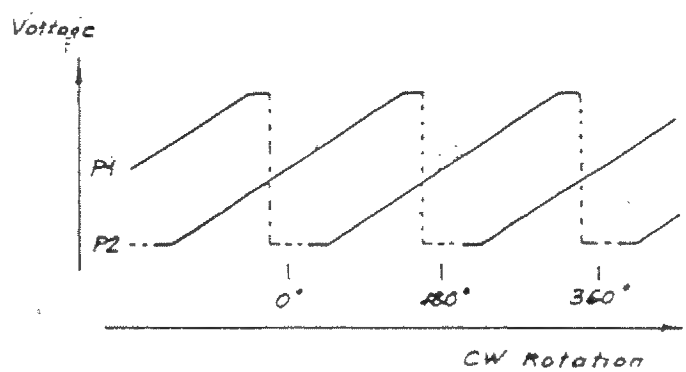
1.5.2 Potentiometer Circuit

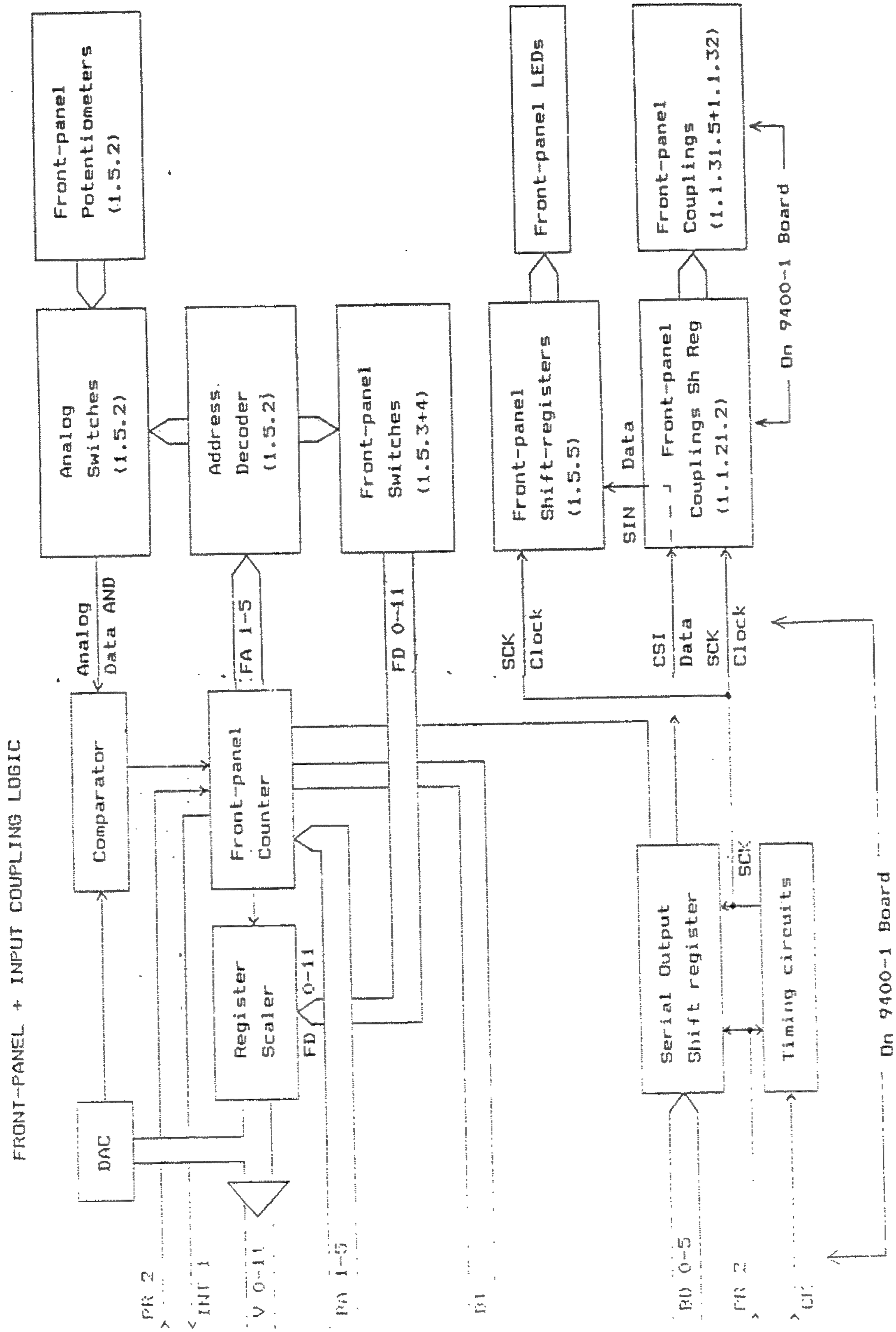
The potentiometers <1.5.2.1> are supplied with DC levels NREF, 0 V, and PREF, +5 V, from the 9400-1 board (1.1.21.3), and not from the local power supplies, so that errors are not caused by voltages induced by currents in the rails. Those controls which are required to rotate continuously without limit have two potentiometers ganged in opposite orientation, so that at least one slider is always on its track. Each slider feeds one input of a DG508 eight-fold analog switch. The eight channels of a DG508 are scanned by FA1 - FA3, with a dwell time of 1.8 ms, and the three ICs are addressed by the values 0, 1 and 2 of FA4 - FA5, the value 3 being used for the switches (1.5.3), so that the four ICs are scanned in the order C D E A.

The outputs of the three analog switches are wire ORed to AN0, which carries the multiplexed levels back to the ADC on the 9400-1 (1.1.21). Of the 24 available lines, five are used for the analog signals ANI38 - ANI46, which come from the frontend section of the 9400-1 (1.1.21.3).

The analog data stream at CDE pin 8 is shown in <1.5.2.2>, which shows just over one complete set of data.

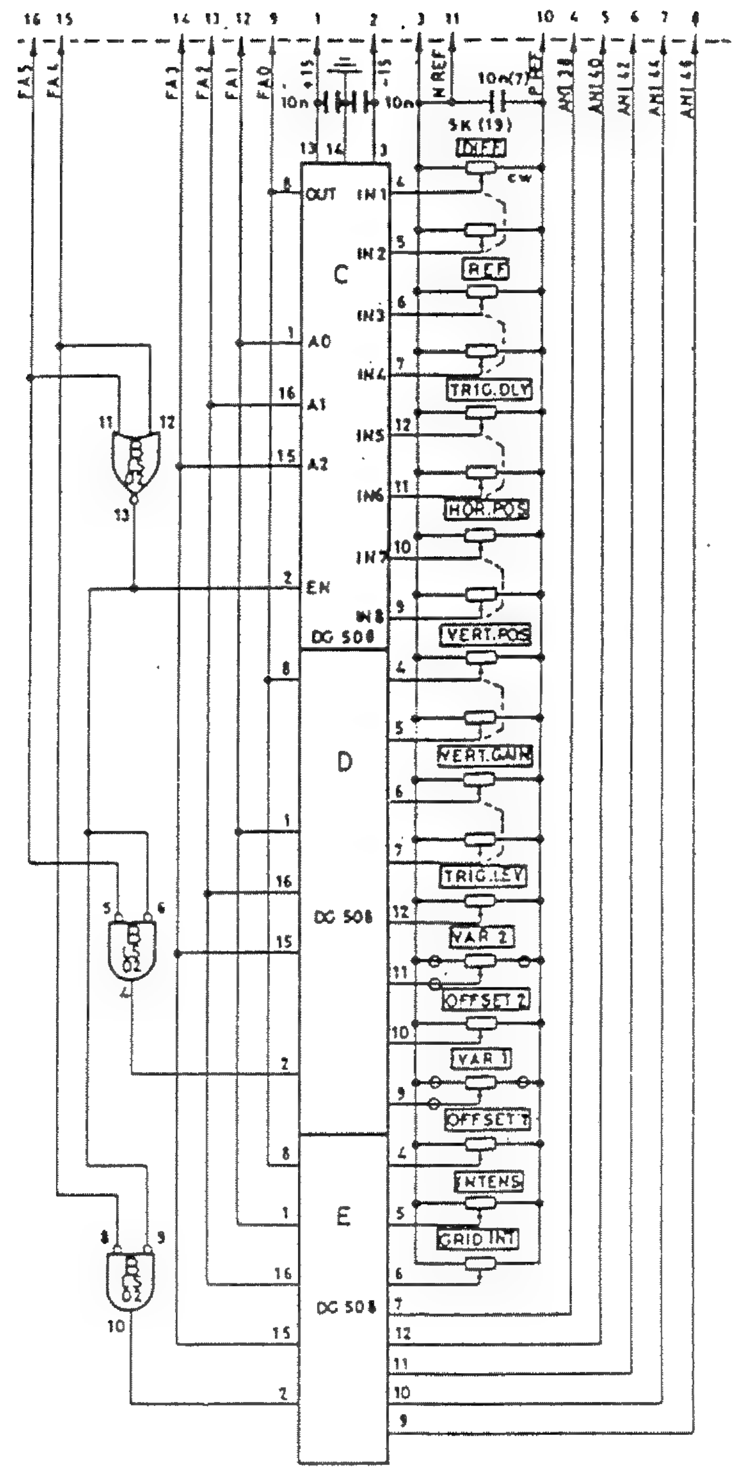






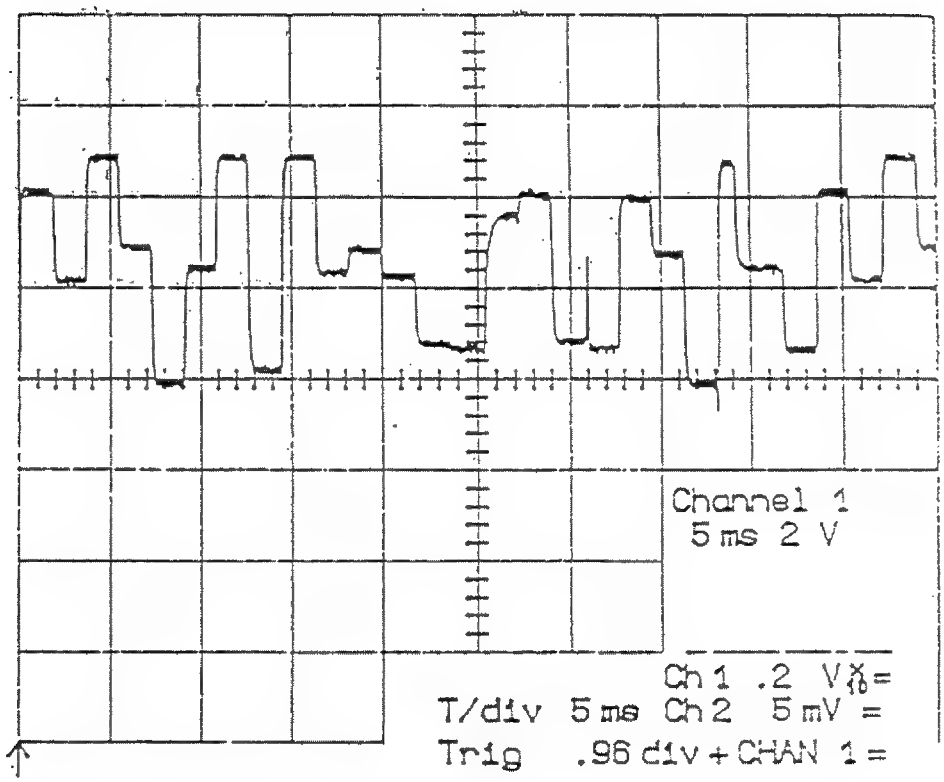
FRONT-PANEL + INPUT COUPLING LOGIC

Figure 1.5.1.1



CIRCUIT FOR POTENTIOMETERS

Figure 1.5.2.1



DATA STREAM AT PIN 8 OF C D E

Figure 1.5.2.2

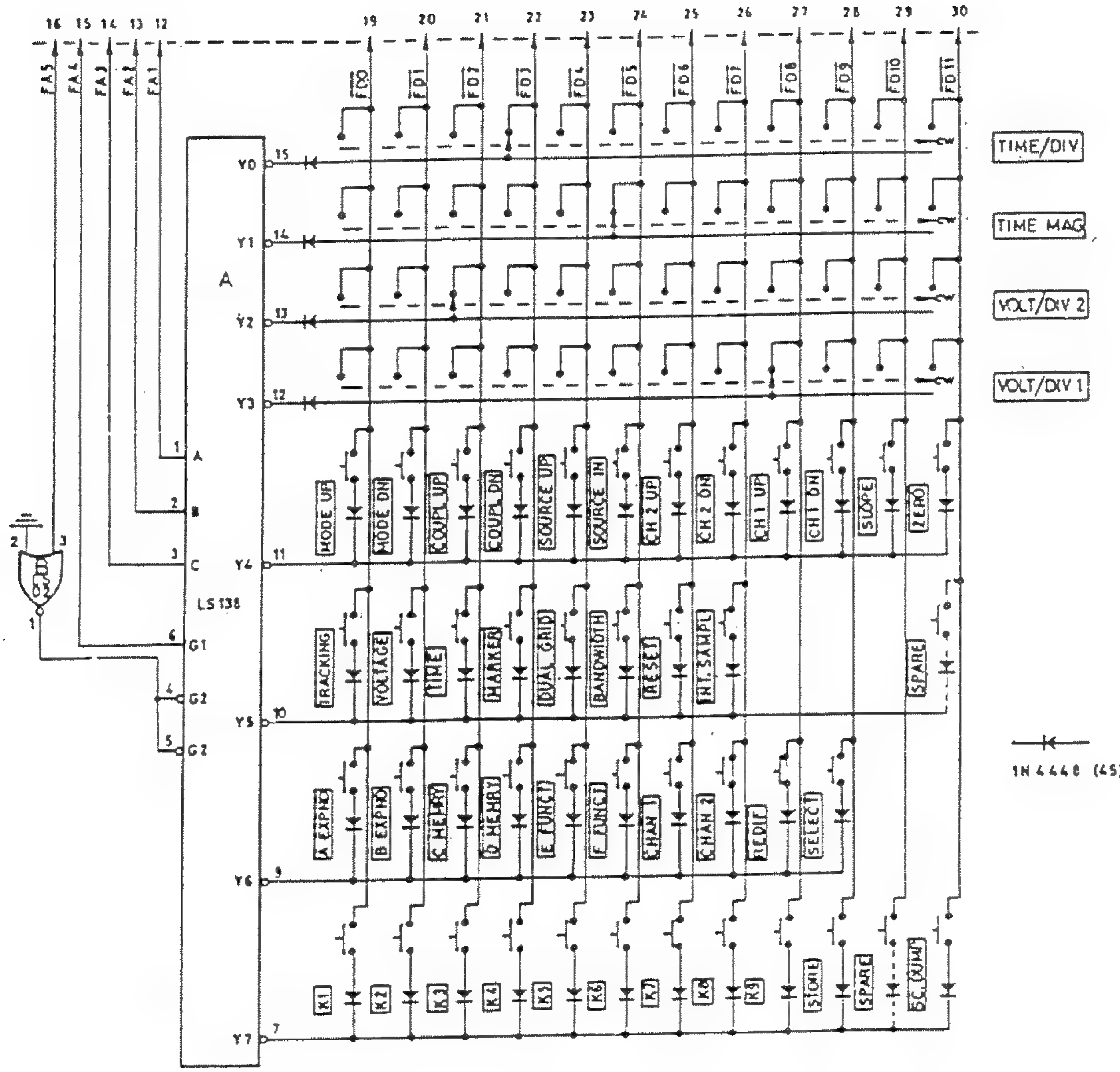
1.5.3 Push Button Switches

These are all normally open push-to-make switches, which, together with the rotary switches (1.5.4), form a matrix controlled by the 74LS138 3-to-8 line decoder A, which is addressed by FA1 - FA3 with a dwell time of 1.8 ms per channel <1.5.3.1>. The resulting digital word on FD0 - FD11 is transmitted to the BD bus of the 9400-1 (1.1.21.4).

The type of signal on the FD bus is shown in <1.5.3.2>, which shows at top, the repetition at about 46 ms intervals of the pull downs at the Y outputs of IC A, in this case by looking at FD0 with the "TRACKING" and "EXPAND A" buttons pressed. The middle trace is FD0 with the same two buttons pressed, to show that each matrix row is exercised for about 2.8 µsec, while the bottom trace shows the case of "TRACKING" only.

1.5.4 Rotary Switches

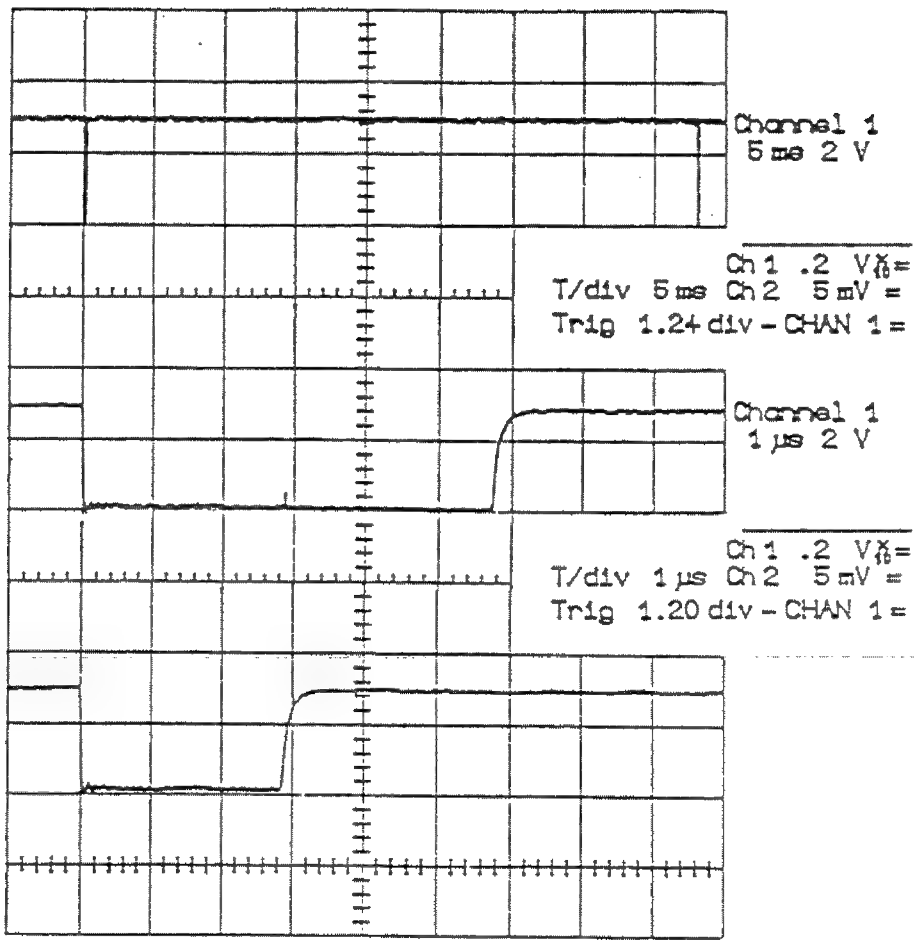
These are all 1-pole, 12-way switches, which are treated in the same way as the push button switches (1.5.3).



SWITCH CONTROL CIRCUIT

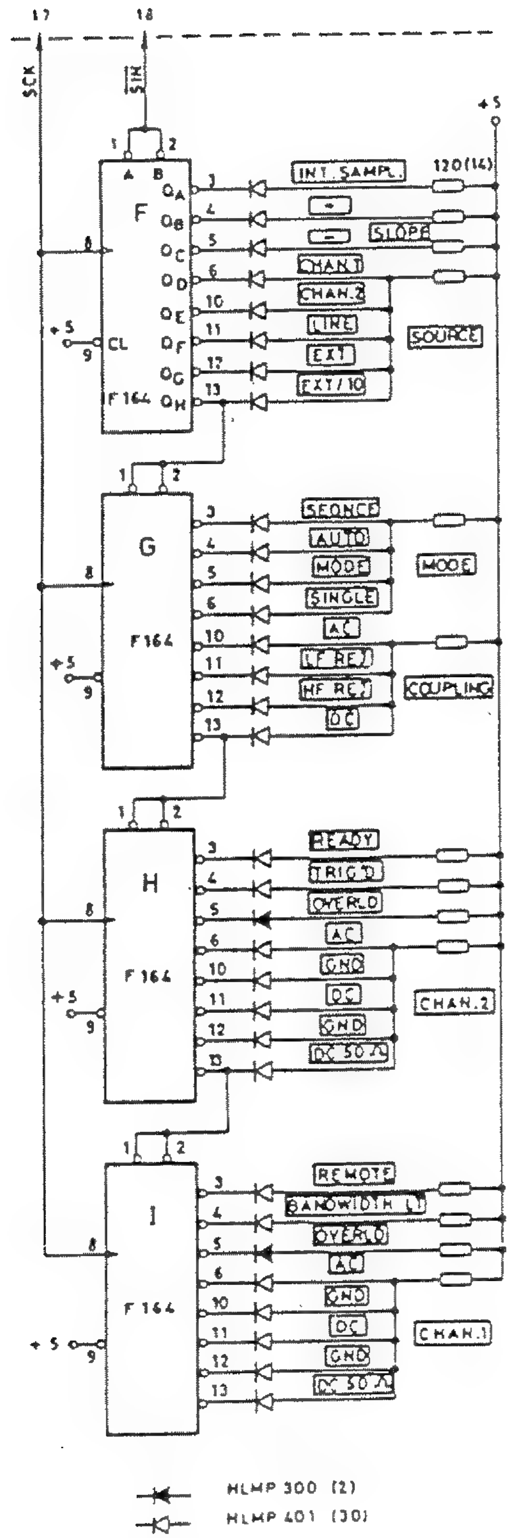
Figure 1.5.3.1

This diagram shows an example of a signal on the FD bus. The waveforms are all from FDO. The top one is for the case when both the "TRACKING" and "EXPAND A" buttons were pressed, showing the signal repeating every 46 ms, the next waveform is one pulse on an expanded scale, and the bottom one shows only the "TRACKING" button pressed, showing the dwell of 2.8 μsec per button.



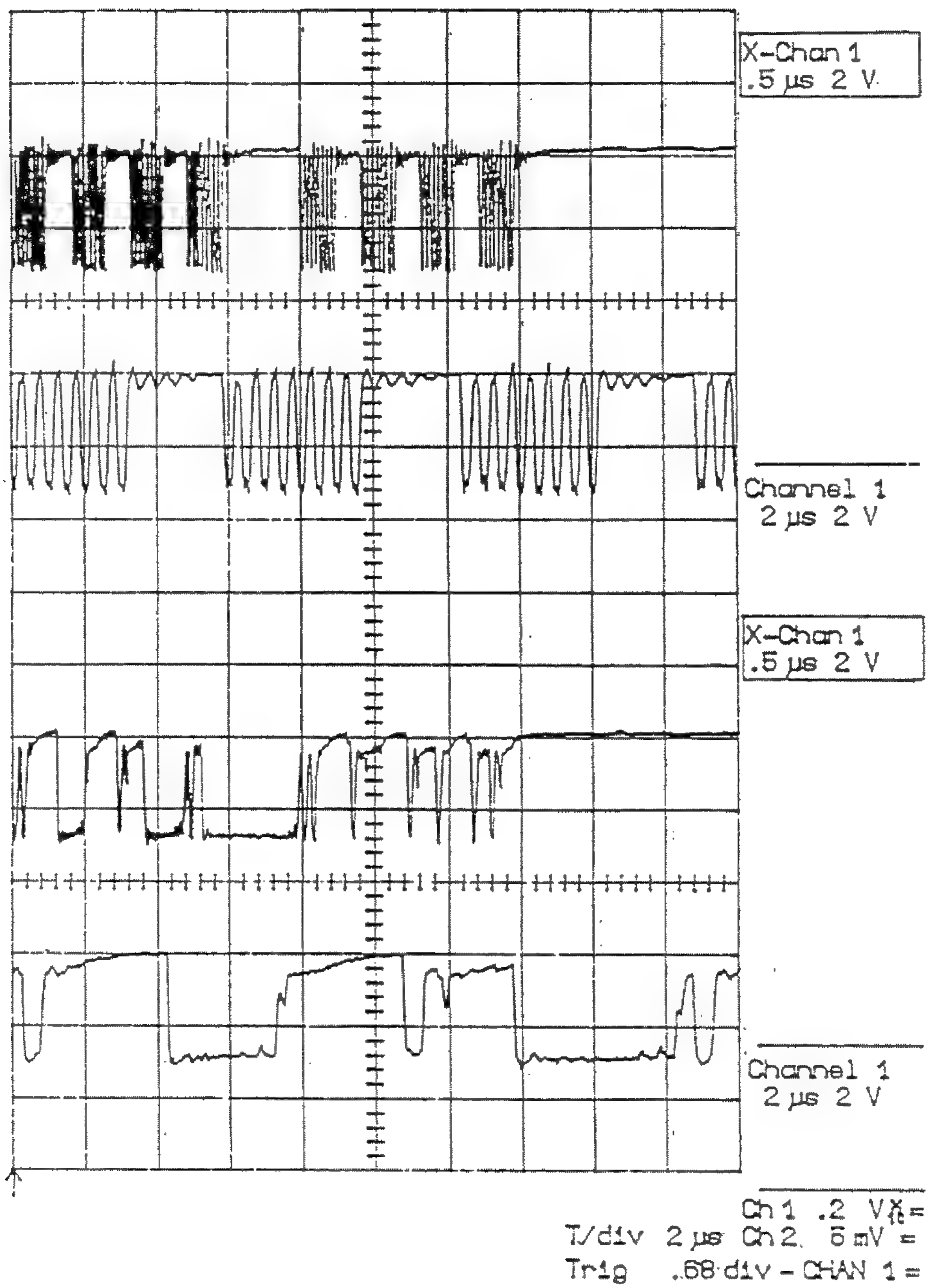
WAVEFORMS ON THE FD BUS, FDO AS EXAMPLE

Figure 1.5.3.2



LED CONTROL CIRCUIT

Figure 1.5.4.1



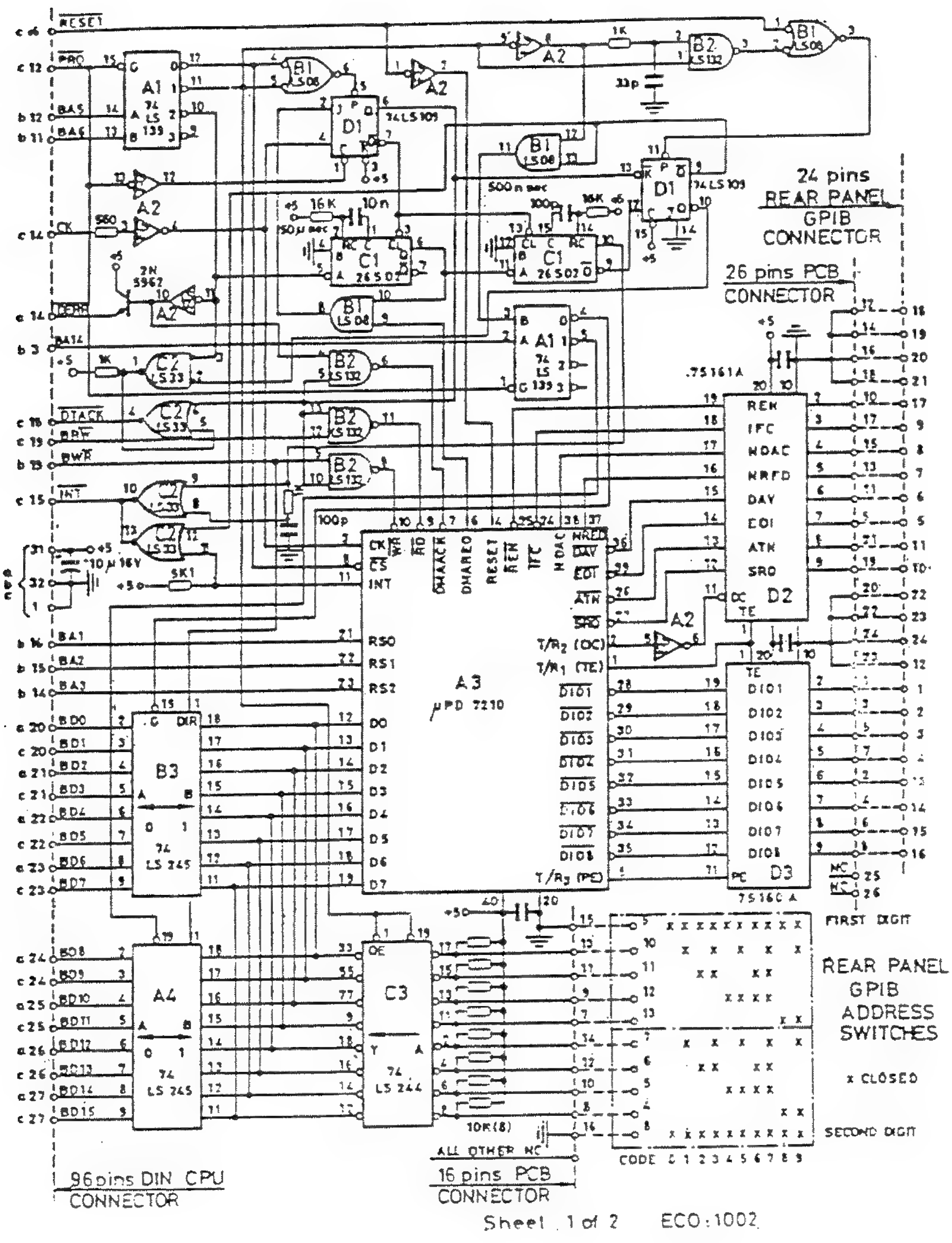
WAVEFORMS IN THE LED CONTROL CIRCUIT

Figure 1.5.4.2

1.5.5 LED Indicators

These are controlled <1.5.4.1> by a set of four serial-to-parallel shift registers, F to I, 74F164s, which are clocked by SCK, and fed with serial data by SIN, from the 9400-1 (1.1.21.2). The signals are sent only when any LED needs to be toggled, or when a frontend analog level needs changing, because the bit stream includes data for the frontend. The LED data are in the second set of 32 bytes; the diagram <1.5.4.2> shows the clock pulses, SCK, and the data stream, SIN. A 9400 DSO cannot be used to inspect its own SIN and SCK, because they are only active when something is to be changed - during an acquisition this cannot be the case. To force a DSO to make the data, set it on AUTO, so that the READY and TRIGG'D lights toggle continually. Then another scope can be used to look at the signals.

Note that one series resistor is provided for any mutually exclusive group of LEDs. All the LEDs in any 9400 DSO are matched for color, except the two red overload lights. The LEDs are sorted into greenish-yellow, yellow, and orange-yellow, which are referred to as "green", "yellow" and "orange". The differences are small, but unacceptable when two different LEDs are placed in the same set on the panel.



9400-6 GPIB INTERFACE BOARD

Figure 1.6.2.1

1.6 9400-6 GPIB INTERFACE BOARD

1.6.1 Introduction

This board has the sole function of controlling the GPIB interface; in 9400 DSO's with the WP01 option the GPIB interface shares a 9401-2 board with extra DRAM and a realtime clock.

A block diagram of the 9400-6 is given in <1.6.1.1>. The board is based on a dedicated microcomputer, a PD7210, which controls the following functions:

- 8 bit GPIB data bus
- 8 GPIB control lines
- 8 bit bus to 9400-1
- addressing from 9400-1
- control lines from 9400-1

1.6.2 Functions

Data are buffered <1.6.2.1> to the BD bus by the two 74LS245 octal bus transceivers, A4, B3, which can be coupled to the 8 bit bus of the microprocessor, or to the GPIB address buffer, C3, a 74LS244 octal buffer. The GPIB address switch is on the back panel.

The buffering of the GPIB lines is done by a 75160A for the 8 bit data, and a 75160A for the control lines.

The processor is addressed by BA1-3,5-6,14.

The processor generates a level 6 interrupt to the 9400-1 (1.1.7). A diagram of the GPIB connector is given in Chapter 4.

1.7 9400-7 Board - CRT Services

This board transmits the luminance signal (Z) from the 9400-2 display board to the cathode of the CRT, with the appropriate level shift and gain. The board also carries the parts which set the static electrode potentials for brilliance, initial acceleration and focusing.

Much of the circuitry on the 9400-7 is concerned with protection of the CRT. Other protection circuitry is present on the 9400-2 board.

This section should be read in conjunction with (1.2), which describes the 9400-2 display board.

A schematic of the 9400-7 board is given in <1.7.1.1>.

1.7.1 Luminance Transmission (Z)

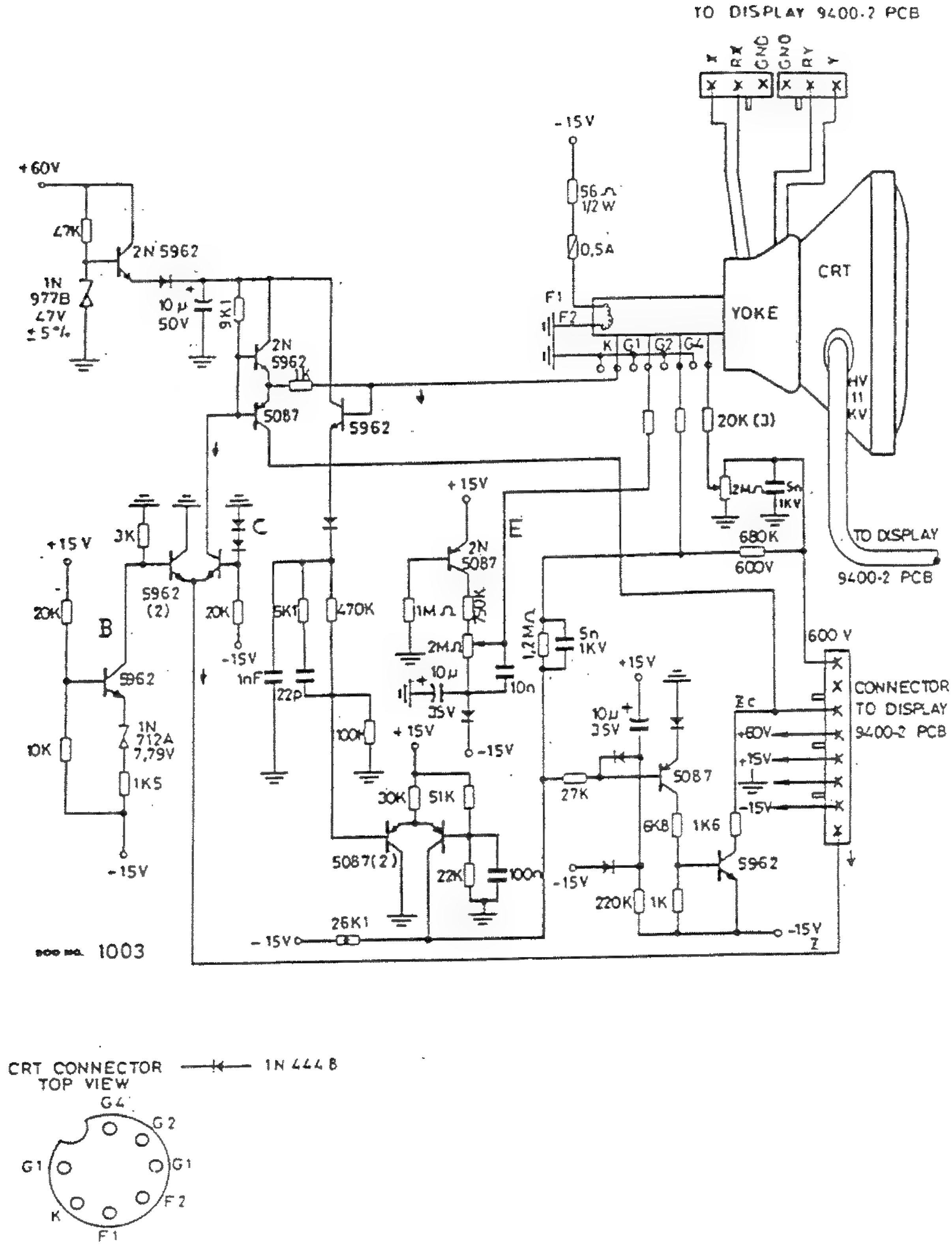
The luminance signal (Z) comes from the I-bar output of the DAC J3 (DAC 08), an 8 bit DAC, on the 9400-2 board. The signal drives the emitter of one of a pair of 2N5962, the other being part of the protection system. An in-phase voltage appears at the collector, to drive the complementary emitter follower which feeds the cathode. Note that the current from the EHT and HT supplies of the CRT emerge at the cathode, and pass through the 2N5087, to the point ZC, which feeds a signal back to the 9400-2 board, as part of the stabilization system. The arrows drawn on the data lines represent voltage changes corresponding to an increase in brightness.

1.7.2 Focus and Brightness

The focus of the tube is adjusted by means of the potential on G4 of the tube, using a 2 M potentiometer from 600 V to ground. The overall brilliance level is set by a 2 M potentiometer essentially from +15 V to -15 V, with intervening protection circuits.

1.7.3 Protection Circuitry

The function of these sections is to prevent, under all foreseeable circumstances, the occurrence of a beam current large enough to impair the function of the phosphor, or even to burn a mark on the screen. Present 9400 DSOs do NOT have a system to detect absence of scan current, so that it is imperative that the leads from the 9400-2 board to the deflection yoke NEVER be removed while EHT is applied to the CRT.



CRT BOARD

Figure 1.7.1

Situations which need to be considered are:

- Loss of +5 V supply
- Loss of +15 V supply
- Loss of -15 V supply
- Loss of two or more supplies
- Conditions during power up
- Conditions during power down

1.7.3.1 Loss of +5 V Line

This eventuality is covered by the 9400-2 board (1.2.5).

1.7.3.2 Loss of +15 V Supply

This is covered by the circuit shown in <1.7.1.B>. The upper 2N5962 is biased off. Should the +15 V supply fail, the lower 2N2962 would be cut off, allowing the upper one to turn on. The other half of the long-tail pair will cut off, killing the beam current.

1.7.3.3 Loss of -15 V Supply

In the event of the -15 V supply failing, both halves of the long-tail pair will lose their base pull downs, but the voltage drop in the two diodes <1.7.1.C>, given the small base current, will be larger than that of the 3 K resistor, and the beam current pass transistor will be cut off.

1.7.3.4 Loss of Two or More Supplies

The protection circuits will act in a fail-safe mode in any combination of failures.

1.7.3.5 Conditions During Power Up

The protection circuitry must act correctly during power on, but must not be so powerful that after this abnormal period the CRT is never allowed to turn on.

1.7.3.6 Conditions During Power Down

During power down one problem is that the cathode temperature falls quite slowly, and even though the electron emissivity is a strong function of the temperature, the grid cathode potential must be strictly controlled during this period. The 10 µF capacitor <1.7.1.E> in the G1 brightness circuit controls the rate of change of the grid potential to prevent a surge in cathode current at power down.

1.8 Clock Bus Board

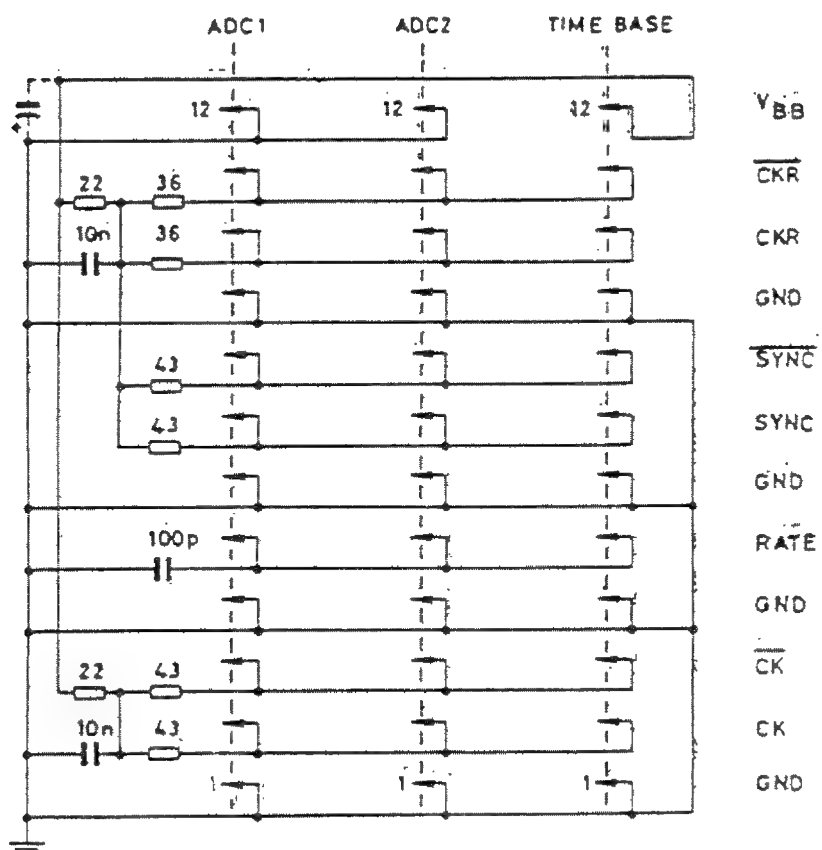
The 9400-8 clock bus is the small board which fits on top of the 9400-3s and the 9400-4 <5.0.2> <1.8.1>.

Its function is to distribute the precision clocks needed by the 9400-3 ADC boards.

The lines have the following functions:

- CK and CK — fast clock at 50 MHz or 100 MHz to clock the sample-and-holds and the ADCs
- RATE — ECL level which is
  0 for 50 MHz
  1 for 100 MHz
- CKR — clock which controls writing to memory
- SYNC — sync pulse at 1/4 of CKR frequency with duty cycle 1/4
- Vbb — Pull down for ECL terminations

CKR and SYNC are shown in <1.3.8.2>.



CLOCK BUS

Figure 1.8.1

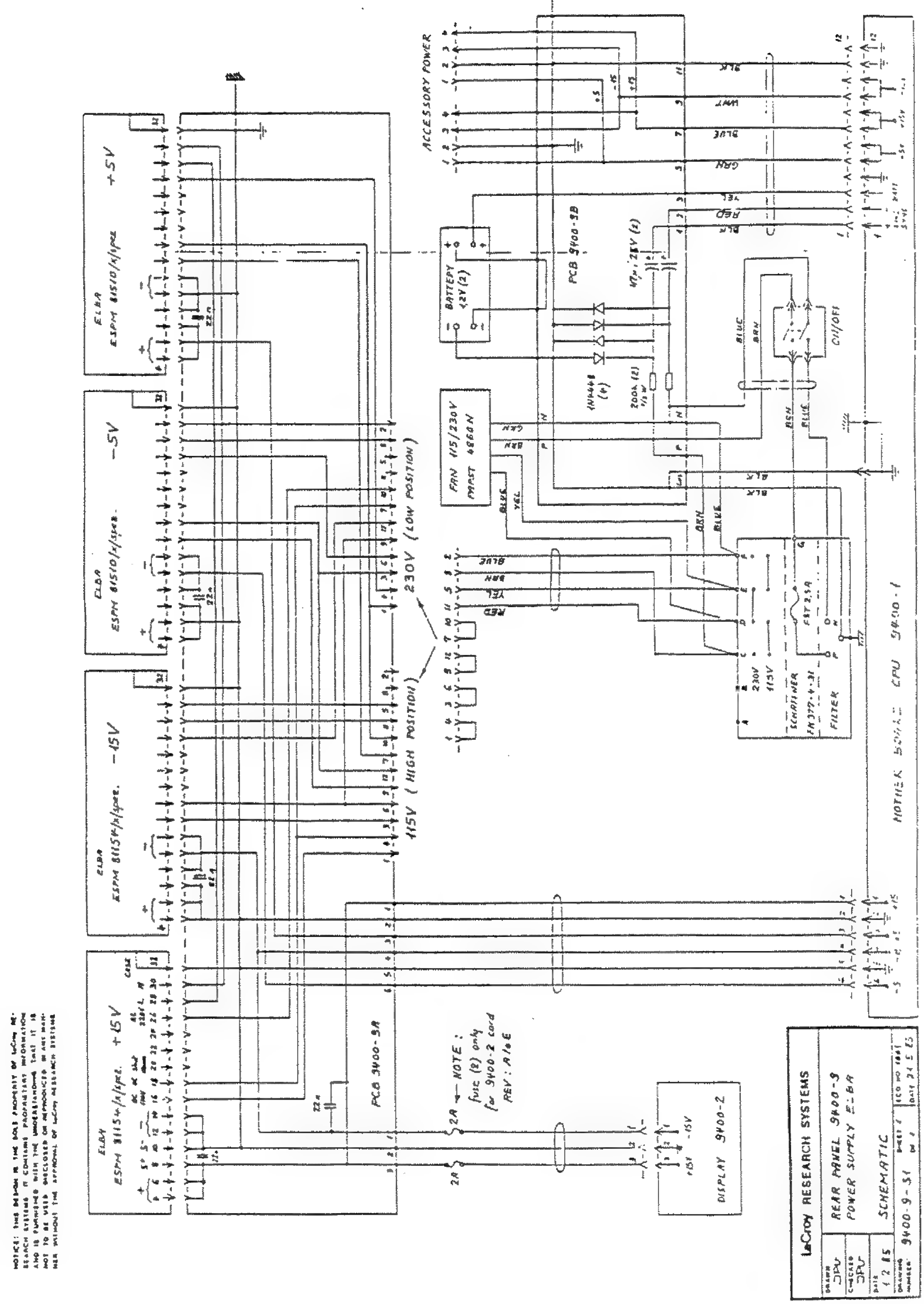
1.9 9400-9 and Power Supplies

The power supply sections of the 9400 DSO are shown in <1.9.1>. The basic supplies used by the 9400 are the four DC levels +15 V, -15 V, +5 V and -5 V, which on some boards are used to generate separate stabilized supplies for special functions. These four supplies are switched mode types, which do not have large external magnetic fields which could disturb the CRT beam.

The 50 Hz/60 Hz line current enters through an RF filter built into the socket on the back panel, and then passes through a fuse to a four wire cable which carries the current to the front panel power switch and back to the 9400-9B board on the back panel. From there the main current goes to the voltage selector and then to the four low voltage supply modules. A resistive bleed supplies a trickle current to the back up battery on the back panel. Current is also supplied to a dual voltage fan on the back panel. The two accessory power sockets are supplied from the 9400-9A board.

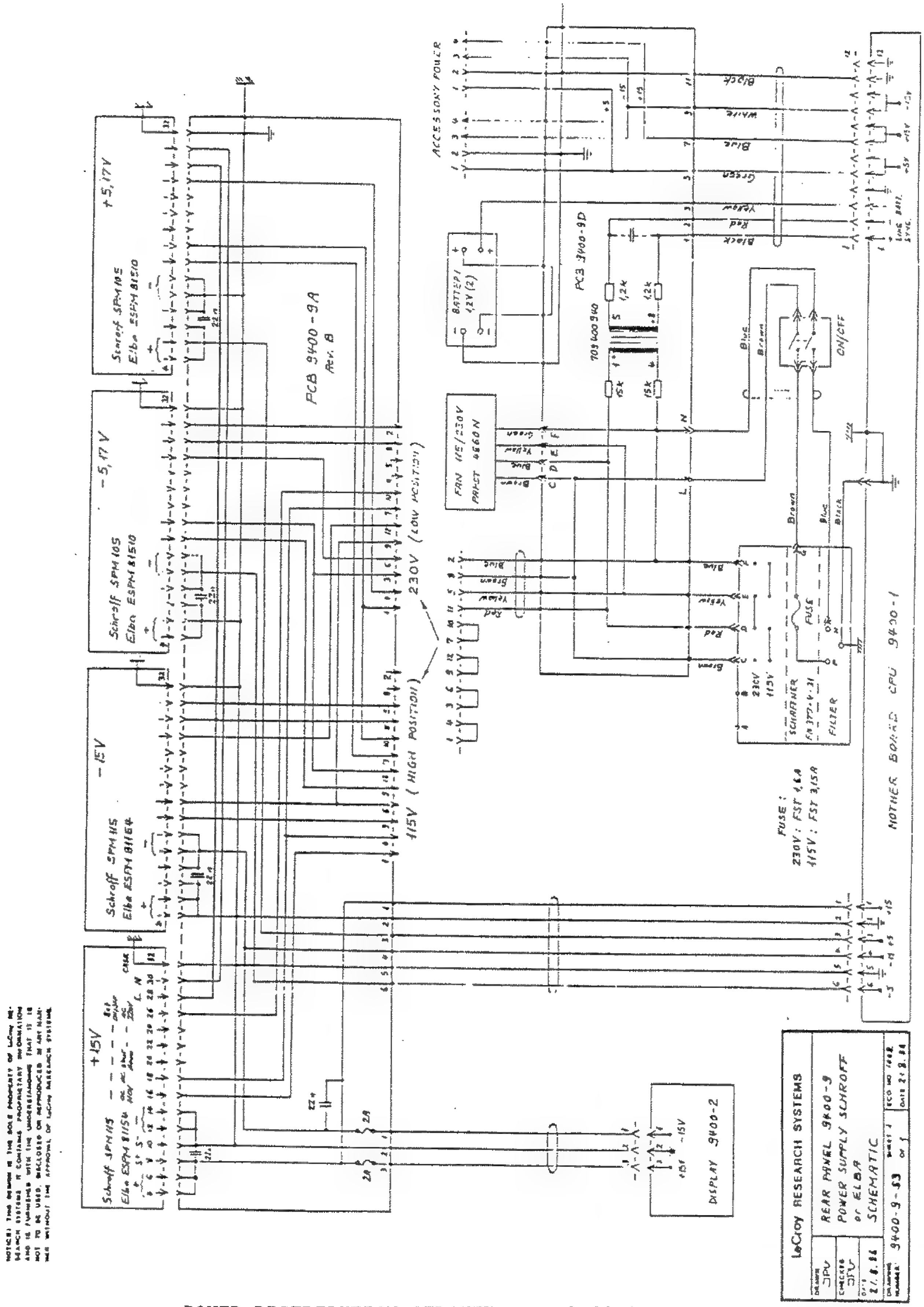
Power is distributed to the 9400 DSO from the 9400-9A board on the front of the four power modules.

The location of circuit elements on the back panel is shown in <1.9.2>.



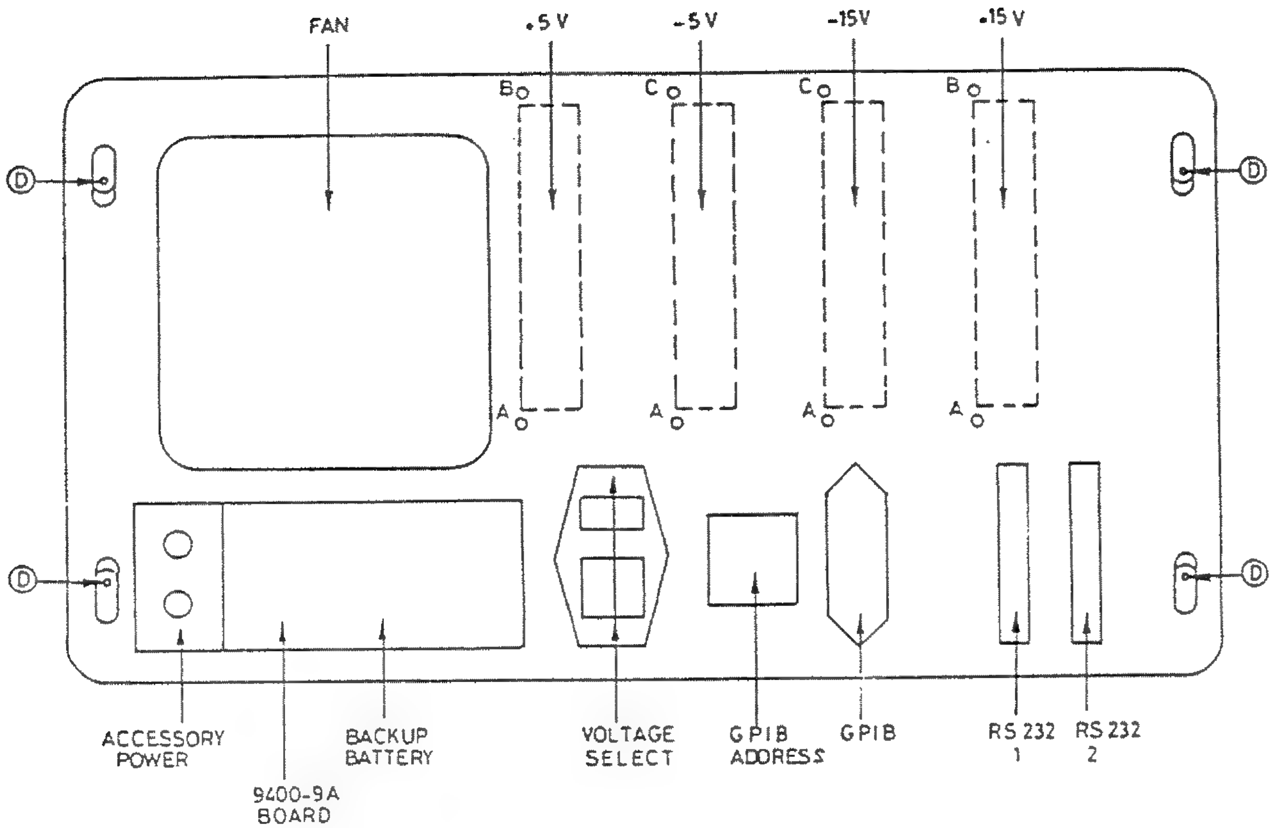
POWER DISTRIBUTION CIRCUIT WITH 9400-9B

Figure 1.9.1



POWER DISTRIBUTION CIRCUIT WITH 9400-9D

Figure 1.9.1A



BACK PANEL LAYOUT

Figure 1.9.2

1.12 9401-2 Board, GPIB, Extra DRAM

1.12.1 Introduction

The 9401-2 board sits in the DMA slot of the 9400, and carries some or all of the following functions, depending on the version. The available versions are:

9401-2 GBIB
9401-2/1 GPIB and DRAM

and the functions are:

GPIB/IEEE-488 interface
Extra DRAM for waveform processing options
Slot for 4928 tester

Note: The basic version of the 9400A has no GPIB board. See Section 1.1.25 for a description of how to make the DSO work with the present standard software, V2.06 STD.

1.12.2 GPIB Interface

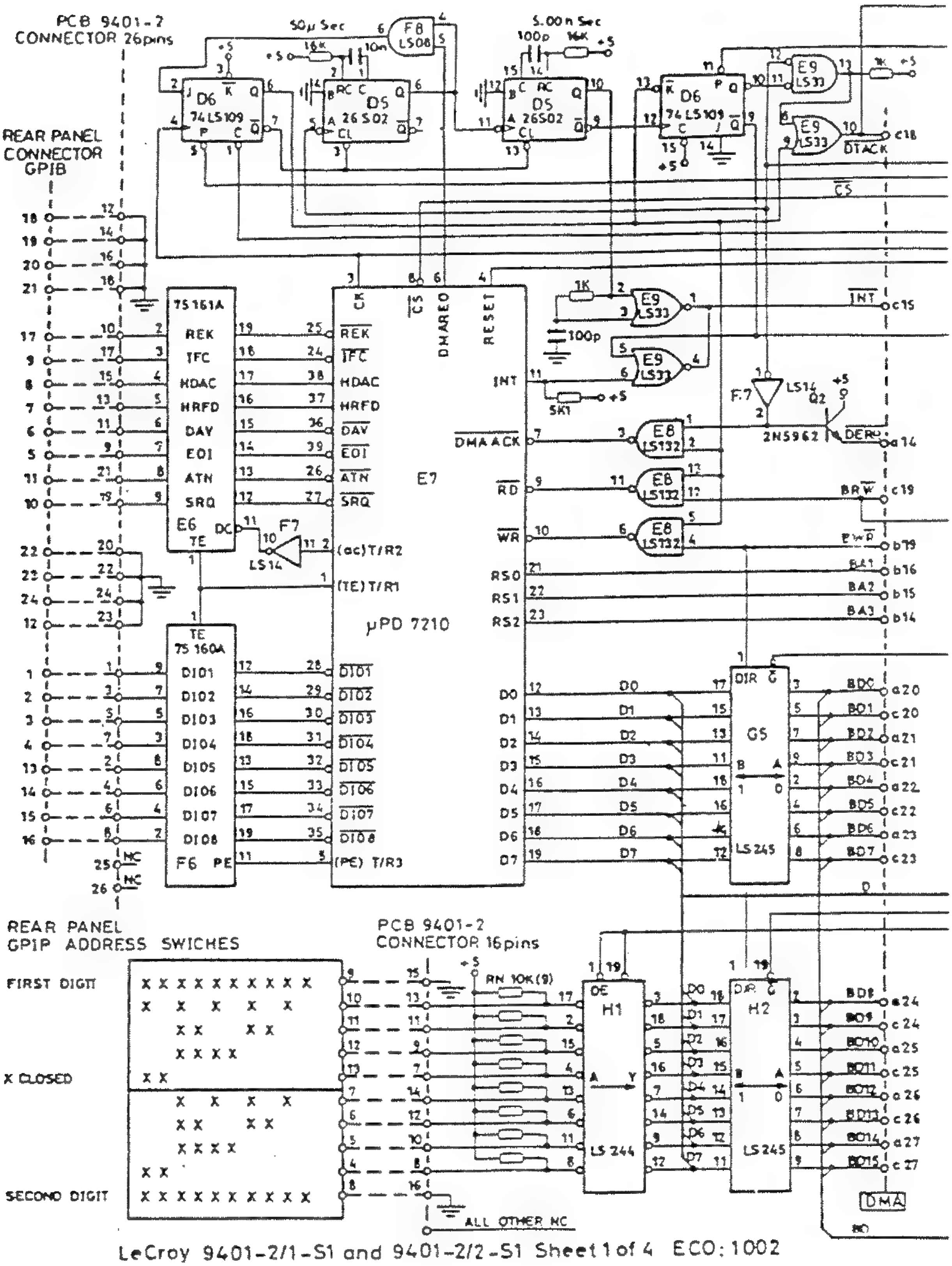
This is similar to the one on the 9400-6 board which was used in earlier 9400s (1.6) in the same (DMA) slot. The schematic is <1.12.2.>. For a brief description of the GPIB system see (1.23).

1.12.3 Extra DRAM

The DRAM controller on the 9401-2 is similar to that of the 9400-1 (1.1.12-1.1.14) and is shown in <1.12.3.1>. The DRAMs are 256 kilobit ICs, arranged to make 128K 32-bit words = 4 x 32K. The extra DRAM is called into play by BK7 (1.1.5) and BAS at C10. BWR gives the read/write control, BLDS and BHDS, select high or low byte of the 68000 word, while the 8 MHz clock, CK, is used via A2 to generate the row and column address strobes, RAS and CAS. The system is similar to the one used in the 9400-1 (1.1.12).

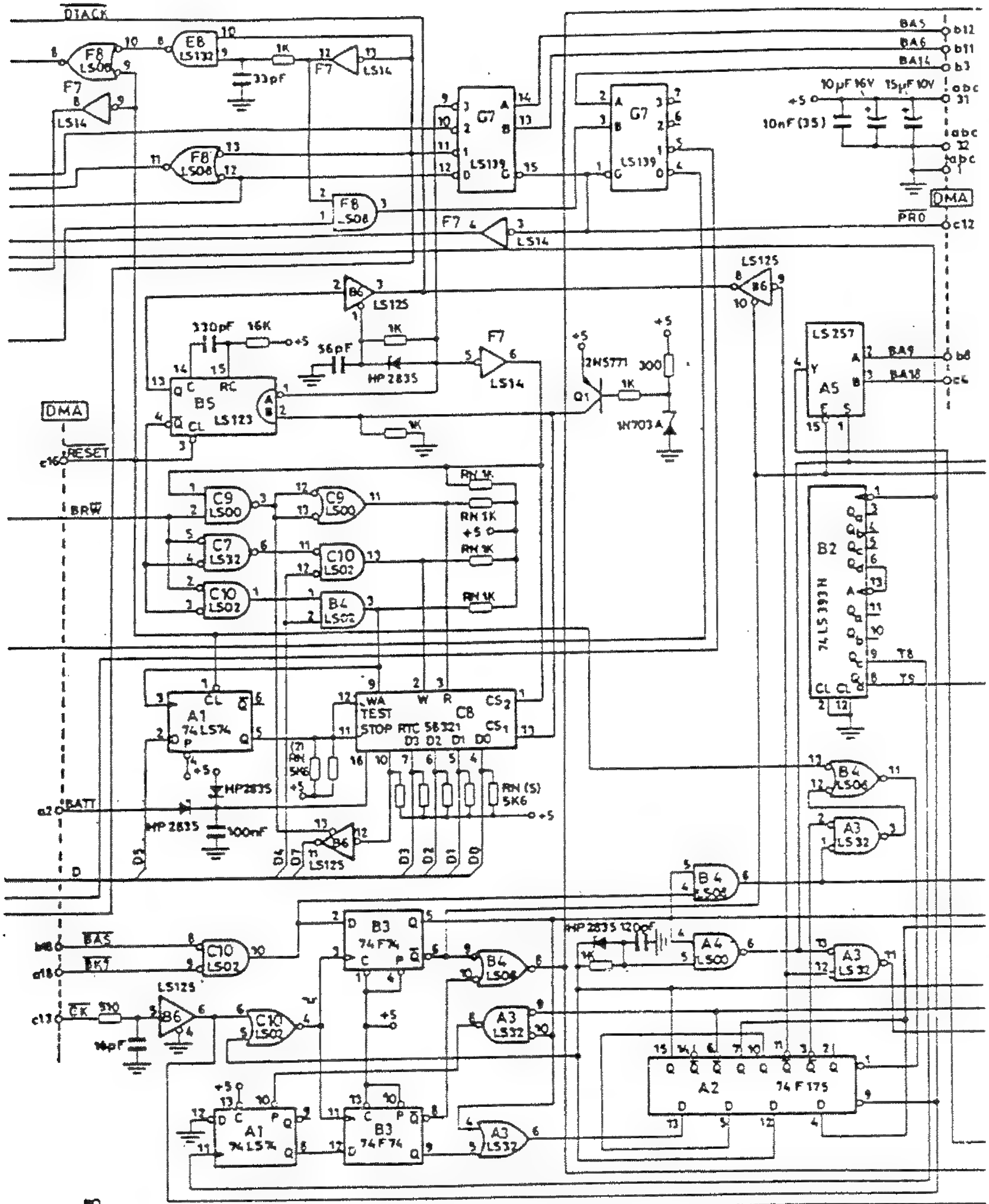
1.12.5 4928 Tester

The 4928 tester is used in conjunction with a LeCroy 3500 microcomputer for testing the 9400. A description of the testing system is given in (3.2). The 4928 board simply fits on top of the 9401-2, and enables the 3500 to take control of the 9400, halting the 68000, which plays no part in the test procedure.

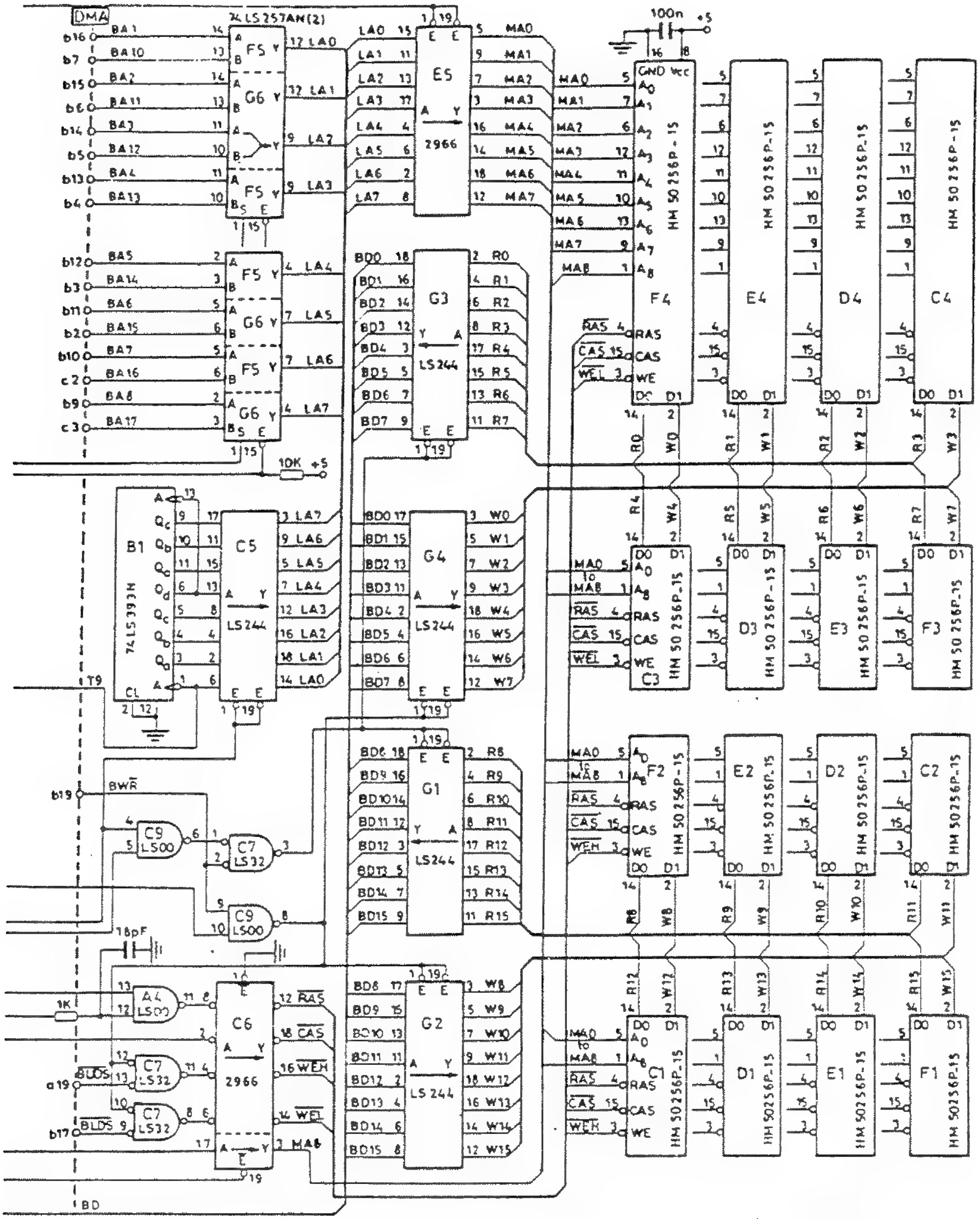


GPIB INTERFACE ON 9401-2

Figure 1.12.2.1



LeCroy 9401-2/1-S1 and 9401-2/2-S1 Sheet 2 of 4 ECO:1002



LeCroy 9401-2/1-S1 and 9401-2/2-S1 Sheet 3 of 4 ECO:1002

EXTRA DRAM CIRCUITS ON 9401-2

Figure 1.12.3.1

1.20 Line finder

The 9400 DSO is a fairly complex piece of equipment with numerous boards, and a great many data lines. This list is intended to simplify the search for the source of labeled data lines. It gives sources with the name of the line, and destinations on subsequent lines with no name. To simplify preparation, negative assertion signals do not have the bar included - this should not in practice cause any trouble. Each entry includes the board number and sheet number on the main schematic (8), the IC and pin number, and the figure number in this manual. A typical use of the list would arise in the case where a line is behaving wrongly, e.g., always high, and in the case of a line like DTACK, there are many possible sources of trouble.

Name	Board	Sht	IC	Pin	Figure	Function B=buffered
ACAL	9400-1	6	J21	15	1.1.17.1	Analog S+H DAC Output voltage
	9400-1	11	H4	16	1.1.31.3	Front End Control
	9400-1	11	H4	16	1.1.34.1	Calibration System
ACALP	9400-1	11	H4	1	1.1.17.1	Analog Calibration Data
	9400-1	11	H3	2	1.1.17.1	
	9400-1	11	H3	2	1.1.31.3	Analog Front End Data
	9400-1	11	H3	2	1.1.34.1	Analog Calibration Data
ACQ	9400-4	5	E5	12	1.4.14.1	Acquisition Mode
	9400-3	6	F10	1,2	1.3.9.1	TDC-ADC Acquisition Mode
	9400-3	7	F11	2	1.3.10.1	ADC Memory Control
	9400-3	6	F11	4,5	1.3.9.1	Multiplexing ADC Control
	9400-3	7	F14	1	1.3.10.1	ADC Memory Control
	9400-3	7	G7	1	1.3.10.1	
	9400-3	7	H7	1	1.3.10.1	
	9400-4	4	A4	13	1.4.12.1	Int TDC
	9400-4	5	C5	5	1.4.15.1	ADC Memory Control
	9400-4	1	D3	13	1.4.7.1	Interrupt Controller
ACQ bar	9400-4	5	C5	4	1.4.15.1	ADC Memory Control
ADC1	9400-1	14	C4	22	1.1.31.2	Front End Output
	9400-3	1	A4	8	1.3.3.2	ADC Board Input
ADC2	9400-1	15	A4	22	1.1.31.2	Front End Output
	9400-3	1	A4	8	1.3.3.2	ADC Board Input
AMPLOFF	9400-2	2	Q	e	1.2.5.1	Kill Trace
	9400-2	6	Q41	e	1.2.5.1	
	9400-2	6	Q52	b	1.2.5.1	
AMPX	9400-2	3	J2	7	1.2.7.1	X Amp Input
	9400-2	5	Q60	b	1.2.8.1	Power Amplifier

AMPY	9400-2	4	J1	7	1.2.7.1(J2)	Y Amp Input
	9400-2	6	Q33	b	1.2.8.1(Q60)	Power Amplifier
AND	9400-5	1	CDE	8	1.5.2.1	Analog Data (Serial)
	9400-1	9	C17	2	1.1.21.1	Front Panel Control
ANI38	9400-1	11	F7	6	1.1.36.1	Front Panel Analog Input
	9400-5	1	E	7	1.5.2.1	Front Panel Control
ANI40	9400-1	11	G7	6	1.1.36.1	Input Overload CHAN1
	9400-5	1	E	12	1.5.2.1	Front Panel Control
ANI42	9400-1	13	C13	7	1.1.32.1	Trigger
	9400-5	1	E	11	1.5.2.1	Front Panel Control
ANI44	9400-1	9	NT6		1.1.21.1	Temperature Check
	9400-5	1	E	10	1.5.2.1	Front Panel Control
ANI46	9400-1	10	Pot1		1.1.35.1	Probe Calibrator
	9400-5	1	E	9	1.5.2.1	Front Panel Control
AS	9400-1	2	H29	6	1.1.1.2	Address Strobe (A1-A23 Valid)
	9400-1	2	E28	2	1.1.10.1	Bus Buffer
	9400-1	1	I18	4	1.1.6.1	Peripheral Decoder
	9400-1	1	I19	1	1.1.4.1	EPROM Strobe
	9400-1	4	J14	6	1.1.12.1	DRAM Controller
B	9400-4	4	A4	8	1.4.12.1	TDC Busy
	9400-4	4	C4	2	1.4.10.1	A+B Delay
	9400-4	1	C6	1	1.4.7.1	Interrupt Controller
	9400-4	4	D1	1	1.4.10.1	A+B Delay
	9400-4	4	D2	2	1.4.10.1	A+B Delay
	9400-4	5	D8	10	1.4.15.1	ADC Memory Controls
	9400-4	4	E2	9	1.4.10.1	A+B Delay
	9400-4	5	E4	13	1.4.15.1	ADC Memory Controls
	9400-4	5	E5	3	1.4.15.1	
	9400-4	5	E5	13	1.4.15.1	
BACK	9400-1	a15	slot	DMA	1.1.11.1	DMA Transfer Bus Acknowledge
	9400-1	2	E28	1	1.1.10.1	Buffer Direction
	9400-1	2	H29	12	1.1.1.2	68000 CPU
	9400-1	1	K13	11	1.1.5.1	Bank Decoder
BAS	9400-1	2	E28	18	1.1.10.1	Buffered AS
	9400-1	7	H15	12	1.1.19.1	Min/max Timing
	9400-1	7	J13	8	1.1.19.1	
	9400-1	4	K16	9	1.1.15.1	Clock Gen
	9400-1	4	K17	5	1.1.15.1	
	9400-1	1	I13	12	1.1.6.1	Peripheral Decoder
	9400-1	1	J19	9	1.1.2.1	Non-reboot Pulse
	9400-1	2	K15	9	1.1.9.1	Time Out Pulse
	9400-3	6	H6	3	1.3.9.1	ADC Board
	9401-2n	2	C10	8	1.12.3.1	Extra DRAM
BATT	9400-1	7	Battery		1.1.22.1	Battery Supply
	9401-n	2	C8	16	1.12.3.1	Extra DRAM
BERR	9400-1	2	H29	27	1.1.1.2	Bus Error
BG	9400-1	2	H29	11	1.1.1.2	DMA Transfer Bus Grant
	DMA slot		a17		1.1.11.1	

BK 0-7	9400-1	1	I17		1.1.5.1	Individual Decoded Bank Address Space
0	9400-1	1	I19	2	1.1.4.1	EPROMs
1						
2						
3	9400-1	1	I18	5	1.1.6.1	Peripheral Decoder
4	9400-1	4	J14	5	1.1.12.1	DRAM Controller
5						
6	9400-3	6	H6	4	1.3.9.1	ADC Board
7	9401-2/n	2	C10	9	1.12.3.1	Extra DRAM
7	DMA slot	a18			1.1.11.1	
BLDS	9400-1	2	E28	16	1.1.10.1	Buffered LDS
	9400-1	4	L17	10	1.1.12.1	RAM Controller
	9400-3	6	H6	1		ADC Board
	9400-2/n	3	C7	9	1.12.3.1	Extra DRAM
BR						DMA Transfer Bus Request
	9400-1	2	H29	13	1.1.1.2	
BRAS	9400-1	4	K16	6	1.1.16.1	Delayed BAS (by 1 CPU clock)
	9400-1	4	K16	8	1.1.15.1	Battery Backup
	9400-1	6	G20	5,9	1.1.22.1	RS232 Interfaces
	9400-3		G6	1	1.3.9.1	ADC Board
BRW	9400-1	2	E28	15	1.1.10.1	Buffered R/W
	9400-1	7	B21	19	1.1.22.1	Battery Backup
	9400-1	9	G19	12	1.1.20.1	Front Panel Control
	9400-1	4	K10	12	1.1.12.1	RAM Select
	9400-1	4	L17	2	1.1.16.1	Display Controller
	9400-4	1	C8	3	1.4.2.1	TDC Bus Interface
	9400-6	1	B2	12	1.6.2.1	GPIB
	9401-2/n	2	C7	5	1.12.3.1	Extra DRAM
	9401-2/n	2	C9	2	1.12.3.1	
	9401-2/n	2	C10	2	1.12.3.1	
BUDS	9400-1	2	E28	17	1.1.10.1	Select
	9400-1	4	L17	13	1.1.12.1	RAM Controller
	9400-3	6	H66	10	1.3.9.1	ADC Board
	9401-2/n	3	C7	13	1.12.3.1	Extra DRAM
BW	9400-1	7	H16	6	1.1.19.1	Min/max Bytes WORD Mode
	9400-1	8	I13	5	1.1.20.1	Min/max/multiply
	9400-1	8	J13	3	1.1.20.1	
	9400-1	8	J13	6	1.1.20.1	

BWR	9400-1	2	C20	7	1.1.10.1	Inverted Buffered Write Line
	9400-1	9	G17	4,9	1.1.24.1	Timer
	9400-1	9	G19	9	1.1.21.1	Front Panel Control
	9400-1	7	H12	13	1.1.19.1	m-M/M Timing
	9400-1	6	L3	1	1.1.18.1	RS232 Port 1
	9400-1	6	L4	13	1.1.18.1	RS232 Port 1
	9400-1	6	L6	13	1.1.18.1	RS232 Port 2
	9400-1	4	L17	4	1.1.16.1	Display Controller
	9400-3	6	H6	5	1.3.9.1	ADC Board
	9400-6	1	B2	9	1.6.2.1	GPIB
	9400-6	1	B3	1	1.6.2.1	
	9401-2/n	3	C5	1,19	1.12.3.1	Extra DRAM
	9401-2/n	3	C9	4	1.12.3.1	Extra DRAM
BW1	9400-1	13	F5	8	1.1.32.1	Bandwidth Control
	9400-1	14	C4	25	1.1.31.1	
BW1 bar	9400-1	13	E6	5	1.1.32.1	Bandwidth Control
	9400-1	14	C4	26	1.1.31.1	
BW2	9400-1	13	F3	6	1.1.31.1	Bandwidth Control
	9400-1	15	A4	25	1.1.31.1	
BW2 bar	9400-1	13	E6	6	1.1.31.1	Bandwidth Control
	9400-1	15	A4	26	1.1.31.1	
BYDIS	9400-1	4	L15	8	1.1.12.1	Display DRAM Access
	9400-2	1	B4	1	1.2.2.1	
BYVEC	9400-2	2	D1	12	1.2.4.1	
	9400-2	1	B4	2	1.2.2.1	
B/W	9400-1	7	H16	6	1.1.19.1	Min/max Bytes Word Mode S+H Memorized Select Address
CA1-3	9400-1	5	J22		1.1.17.1	Calibration Codes
	9400-1	11	H4		1.1.17.1	Calibration Codes
	9400-1	11	H4		1.1.31.3	Frontend Control
	9400-1	11	H4		1.1.34.1	Calibration System
CAC	9400-1	13	E12	12	1.1.32.1	AC Trig Select
	9400-1	13	switch	7	1.1.32.1	
CACLR	9400-1	13	E12	13	1.1.32.1	LF Rej Trig Select
	9400-1	13	switch	8	1.1.32.1	
CALEN	9400-1	6	F18	12	1.1.17.1	S+H Load Strobe
	9400-1	11	H4	9	1.1.17.1	
	9400-1	11	H4	9	1.1.31.1	Frontend Control
	9400-1	11	H4	9	1.1.34.1	Calibration System
CALENP	9400-1	11	H4	8	1.1.17.1	
	9400-1	11	H3	2	1.1.17.1	
	9400-1	11	H3	2	1.1.31.3	Calibration System
	9400-1	11	H3	2	1.1.34.1	Frontend Control
CAL1	9400-1	11	G6	1,14	1.1.31.3	Calibration CHAN1
	9400-1	14	C4	44	1.1.31.2	Calibration Input
CAL2	9400-1	11	G6	7,8	1.1.31.3	Calibration CHAN2
CAS	9400-1	15	A4	44	1.1.31.3	Calibration Input
	9400-1	4	K21	5	1.1.12.1	DRAM Column Addr Strobe
	9400-1	5	K23-	15	1.1.14.1	Dynamic RAM
	9400-1	5	-L30	15	1.1.14.1	
CDC	9400-1	13	E12	10	1.1.32.1	DC Trigger Select
	9400-1	13	switch	5	1.1.32.1	

CDCHR	9400-1	13	E12	11	1.1.32.1	HF Rej Trigger Sel
	9400-1	13	switch 6		1.1.32.1	
CK 8MHz	9400-1	4	K17	10	1.1.15.1	Main 8 MHz CPU Clock
CKbar	9400-1	4	K17	9	1.1.15.1	8 MHz Clock
	9400-1	9	F17	1	1.1.21.1	Front Panel Control
	9400-1	9	G18	14	1.1.21.1	Front Panel Control
	9400-1	2	H29	15	1.1.1.2	CPU Clock
	9400-1	4	K12	9	1.1.12.1	DRAM Controller
	9400-1	4	K14	9	1.1.12.1	DRAM Controller
	9400-2	1	A2	2	1.2.2.1	
	9400-2	1	A4	2	1.2.2.1	Display Board
	9400-2	1	B2	3	1.2.2.1	
	9400-6	1	A2	3	1.6.2.1	TDC Clock Divider
	9400-2/n	2	B6	5	1.12.3.1	
CK (Samp)	9400-4	2	K1	2,3	1.4.6.1	100/50 MHz Clock
	9400-3	1	A1	9,10	1.3.2.1	ADC Board
CK BUF	9400-2	2	D1	13	1.2.3.1	Display Board
	9400-2	2	C1	10	1.2.3.1	
	9400-2	2	E1	20	1.2.3.1	
	9400-2	2	E2	20	1.2.3.1	
	9400-2	2	E3,F1	11	1.2.3.1	
	9400-2	2	G5,H1	11	1.2.3.1	
CKD	9400-1	7	I14	2	1.1.19.1	min/max Decision Clock
	9400-1	8	J11	9	1.1.20.1	
CKM	9400-1	7	I11	6	1.1.19.1	Multiplicator Clock
	9400-1	8	I3	7	1.1.20.1	
	9400-1	8	J3	7	1.1.20.1	
CKR	9400-4	2	I3	3,6	1.4.3.1	Sample Clock
	9400-3	3	B1	9,10	1.3.9.1	Data Multiplexer
CKS	9400-1	7	I11	8	1.1.19.1	Multiplicator Shift Clock min/max Load Clock
	9400-1	8	I8	12	1.1.20.1	min/max/mult
	9400-1	8	I9	12	1.1.20.1	
	9400-1	8	J8	12	1.1.20.1	
	9400-1	8	J9	12	1.1.20.1	
CLEAR						General Clear Line (for Display and S+H)
	9400-1	4	L14	12	1.1.12.1	DRAM Controller
	9400-1	4	L15	12	1.1.12.1	DRAM Controller
CRP	9400-9B					50/60 Hz Sync
	9400-1	1	J17	10	1.1.8.1	Sync and Line Trig
	9400-1	1	J17	11	1.1.8.1	Sync and Line Trig
CSI	9400-1	9	H9	7	1.1.21.1	Front Panel Data Shift in
	9400-1	11	H4	11	1.1.17.1	Calibration Controller
	9400-1	11	H4	11	1.1.31.3	Analog Frontend Control
	9400-1	9	H9	1	1.1.21.1	Front Panel Control
CSIP	9400-1	11	H4	6	1.1.31.3	Serial Frontend Data
	9400-1	12	F4	1,2	1.1.31.2	Frontend Digital Control
CSO	9400-1	13	E12	13	1.1.32.1	Front Panel Data Shift Out
	9400-1	9	G17	2	1.1.21.1	Front Panel Control
CTC1	9400-1	13	E12	3	1.1.32.1	Int Trig CHAN1 Control
	9400-1	13	swit.3		1.1.32.1	

CTC2	9400-1	13	E12	4	1.1.32.1	Int Trig CHAN2 Control
	9400-1	13	swit.2		1.1.32.1	
CTE	9400-1	13	E12	5	1.1.32.1	Ext Trig Control
	9400-1	13	swit.1		1.1.32.1	
CTL	9400-1	13	E12	6	1.1.32.1	Line Trigger Control
	9400-1	13	swit	4	1.1.32.1	
CTN	9400-1	13	E6	11	1.1.32.1	Neg Trig Select
	9400-1	13	A13	7	1.1.32.1	
CTP	9400-1	13	E6	12	1.1.32.1	Pos Trig Select
	9400-1	13	A13	5	1.1.32.1	
D0-4	9400-4	2	B5	1	1.4.4.1	Bidirectional CPU Data Bus
0	9400-4	2	G7	7	1.4.6.1	TDC Clock Divider
1	9400-4	2	G7	5	1.4.6.1	
2	9400-4	2	F6	11	1.4.6.1	
2	9400-4	2	F7	14	1.4.6.1	
3	9400-4	2	F6	10	1.4.6.1	
3	9400-4	2	F7	2	1.4.6.1	
4	9400-4	2	F6	9	1.4.6.1	
4	9400-4	2	F7	10	1.4.6.1	
4	9400-4	2	G6	5	1.4.6.1	
DDIS	9400-2	1	A2	14	1.2.2.1	Display DRAM Access Demand
	9400-1	4	L15	11	1.1.12.1	DRAM Controller
DERR	9400-6	1	A2	10	1.6.2.1	Hardware DMA Bus Error
	9401-2	1	Q2	e	1.12.2.1	
	9400-1	2	E28	8	1.1.10.1	Bus Buffer
	9400-1	2	E28	11	1.1.10.1	Bus Buffer
DTACK	9400-1	9	G17	8	1.1.21.1	Data Transfer Acknowledge on CPU Bus
	9400-1	9	G20	3	1.1.21.1	Front Panel Control
	9400-1	7	G20	8	1.1.22.1	Backup RAM
	9400-1	7	H15	3	1.1.19.1	Min/max/mult
	9400-1	4	J15	3	1.1.12.1	DRAM Controller
	9400-1	6	J15	6	1.1.18.1	RS232 Interfaces
	9400-1	1	J15	11	1.1.4.1	EPROM Addressing
	9400-1	4	K16	6	1.1.16.1	Display Controller
	9400-3	6	F13	3	1.3.10.1	ADC Memory Control
	9400-4	1	C7	11	1.4.4.1	TDC Command Register
	9400-6	1	C2	4	1.6.2.1	GPIB
	9401-2	1	E9	10	1.12.2.1	GPIB
	9401-2	2	B6	3,10	1.12.3.1	
	9400-1	2	H29	10	1.1.1.2	CPU DTACK Input
EI	9400-4	1	A5	6	1.4.4.1	Enable Interrupt
	9400-4	1	C4	5	1.4.7.1	Interrupt Controller
EOVX	9400-2	3	Q29	C	1.2.6.1	End of Vector X
	9400-2	2	D2	1	1.2.3.1	WRVEC
EOVY	9400-2	4	Q14	C	1.2.6.1	End of Vector Y
	9400-2	2	D2	1	1.2.3.1	WRVEC
ERR	9400-1	2	L15	6	1.1.9.1	General Hardware Bus Error
	9400-1	2	E28	9	1.1.10.1	Bus Buffer
	9400-1	2	E28	12	1.1.10.1	Bus Buffer
ET	9400-4	1	A5	19	1.4.4.1	Ext Trigger Select
	9400-4	3	G1	7	1.4.8.1	Trigger System

ETR	9400-1	10	Q5	E	1.1.33.1	External Trigger
	9400-1	3	switch1		1.1.32.1	
EXT	9400-1	10	Front panel		1.1.33.1	External Trigger in
FA	9400-4	1	B5	9	1.4.4.1	50/100 MHz Select
	9400-4	2	G7	11	1.4.6.1	
FA 1-5						Front Panel Address Read Bus
1	9400-5	1	CDE	1	1.5.2.1	Potentiometers
2	9400-5	1	CDE	16	1.5.2.1	
3	9400-5	1	CDE	15	1.5.2.1	
4	9400-5	2	A	6	1.5.3.1	Switcher
4	9400-5	1	B	8,12	1.5.2.1	Potentiometers
5	9400-5	1	B	3,5,11	1.5.2.1	
1-5	9400-1	9	C18		1.1.21.1	
4	9400-1	9	F19	4	1.1.21.1	Front Panel Control
5	9400-1	9	F19	5	1.1.21.1	Front Panel Control
FA 0	9400-5	1	CDE	8	1.5.2.1	Analog Serial Bus
see AN 0	9400-1	9	C17	2	1.1.21.1	
FC	9400-1	1	K13	8	1.1.5.1	CPU Function Code Mode Data Transfer
	9400-1	1	I17	7	1.1.5.1	
	9400-1	1	L13	13	1.1.5.1	
FC 0-2	9400-1	2	H29	26+	1.1.1.2	CPU Function Code (data -interrupt)
0-1	9400-1	1	K13	9+	1.1.5.1	Block Decoder
GAIN1	9400-1	11	G5	14	1.1.31.3	Gain CHAN 1
	9400-1	14	C4	20	1.1.31.2	Frontend Gain
GAIN2	9400-1	11	G5	8	1.1.31.3	Gain CHAN 2
	9400-1	15	A4	20	1.1.31.2	Frontend Gain
GBUS	9400-1	4	K11	14	1.1.12.1	CPU Bus DRAM Access
	9400-1	5	C21	5.15	1.1.13.1	
	9400-1	4	J15	1	1.1.12.1	
	9400-1	4	K10	10	1.1.12.1	
	9400-1	4	K13	3	1.1.12.1	
	9400-1	4	L11	1+	1.1.12.1	
GCAL	9400-1	4	K10	6	1.1.12.1	S+H DAC DRAM Access
	9400-1	4	F18	9	1.1.17.1	Calibration Controller
	9400-1	4	L13	1	1.1.12.1	
	9400-1	5	L20	15	1.1.13.1	RAM Address Select
	9400-1	5	K21	1	1.1.13.1	
GDIS	9400-1	4	K10	8	1.1.12.1	Display DRAM Access
	9400-1	4	L13	5	1.1.12.1	
	9400-1	5	L18	15	1.1.13.1	RAM Address Select
	9400-1	5	L19	15	1.1.13.1	
GNDCAL	9400-1	6	GND		1.1.17.1	S+H Reference Ground
GRAM	9400-1	4	L12	6	1.1.12.1	General DRAM Access
	9400-1	5	K22	1+	1.1.13.1	RAM Address Select
GREF	9400-1	4	L11	8	1.1.12.1	Refresh DRAM Access
	9400-1	4	K13	13	1.1.12.1	
	9400-1	4	L10	13	1.1.12.1	
	9400-1	5	L18		1.1.13.1	RAM Address Select
	9400-1	5	L22		1.1.13.1	RAM Address Select

HALT	9400-1	1	J17	1	1.1.3.1	General Halt Line (boot with RESET)
	9400-1	2	H29	17	1.1.1.2	CPU Halt
	9400-1	2	L15	2	1.1.9.1	Time Out
IN CHAN1	9400-1	14	Front panel		1.1.31.2	CHAN 1 Input
IN CHAN2	9400-1	15	Front panel		1.1.31.2	CHAN 2 Input
INT1	9400-1	9	H16	9	1.1.21.1	Individual Interrupt Request
INT2	DMA slot		a12		1.1.11.1	DMA Interrupt
INT3	9400-1	6	L4	18	1.1.18.1	RS232-1 Interrupt
INT4	9400-1	6	L6	18	1.1.18.1	RS232-2 Interrupt
INT5	9400-4	1	C5	13	1.4.7.1	TDC Interrupt
INT6	9400-6	1	C2	1	1.6.2.1	GPIB Interrupt
INT7	DMA slot		a13		1.1.11.1	Test Interrupt
	9400-1	1	H20	1	1.1.7.1	Interrupt Decoder
IPL 0	9400-1	1	H20	6-9	1.1.7.1	External Coded CPU Interrupt Priority Level
	9400-1	2	H29	23+	1.1.1.2	CPU Int Inputs
IT	9400-4	1	A5	2	1.4.4.1	Random Trig Enable
	9400-4	3	G1	11	1.4.8.1	
LDS	9400-1	2	H29	8	1.1.1.2	Lower Byte Data Bus Strobe (word transf with UDS)
	9400-1	2	E28	4	1.1.10.1	Bus Buffer
LTR	9400-1	1	J17	13	1.1.8.1	Line Synchronization
	9400-1	13	switch	4	1.1.32.1	
MCL	9400-1	7	H15	11	1.1.19.1	
	9400-1	7	G17	13	1.1.19.1	
	9400-1	7	H11	1	1.1.19.1	
	9400-1	7	H16	3	1.1.19.1	
	9400-1	8	I3	1	1.1.20.1	m-M/M
	9400-1	7	I15	1	1.1.19.1	
	9400-1	8	J3	1	1.1.20.1	m-M/M
MER	9400-1	7	H12	11	1.1.19.1	min/max Product Enable Read
	9400-1	8	I7	1+	1.1.20.1	
	9400-1	8	J7	1+	1.1.20.1	
MEW	9400-1	7	H13	3	1.1.19.1	min/max Mult Write Enable
	9400-1	8	I6	1+	1.1.20.1	
	9400-1	7	I10	3	1.1.19.1	
	9400-1	7	I11	4	1.1.19.1	
	9400-1	8	J6	1+	1.1.20.1	
	9400-1	7	J10	3	1.1.19.1	
MIN	9400-1	7	H12	5	1.1.19.1	max/min Test
	9400-1	7	I12	10	1.1.19.1	
	9400-1	8	J11	1	1.1.20.1	
	9400-1	8	J12	2,4	1.1.20.1	
MLL	9400-1	7	J13	10	1.1.19.1	min/max Mult Input DATA Strobe

MNE	9400-1	7	I12	8	1.1.19.1	Internal Min Product Enable Read
	9400-1	8	I8	3	1.1.20.1	
MNH 0-1	9400-1	7	J10		1.1.19.1	Upper Byte Min Load Mult CTE Load Shift Command
0	9400-1	8	J8	1	1.1.20.1	
1	9400-1	8	J8	19	1.1.20.1	
MNL 0-1	9400-1	7	I10		1.1.19.1	Lower Byte Min Load Mult CTE Load Shift Command
0	9400-1	8	I8	1	1.1.20.1	
1	9400-1	8	I8	19	1.1.20.1	
MXE	9400-1	7	I12	6	1.1.19.1	Internal Max Read Enable
	9400-1	8	I9	3	1.1.20.1	
	9400-1	8		3	1.1.20.1	
MXH 0-1	9400-1	7	J10		1.1.19.1	Upper Byte Max Load Command
0	9400-1	8		1	1.1.20.1	
1	9400-1	8		19	1.1.20.1	
MXL 0-1	9400-1	7	I10		1.1.19.1	Lower Byte Max Load Command
0	9400-1	8	I9	1	1.1.20.1	
1	9400-1	8	I9	19	1.1.20.1	
NEG IN	9400-4	3	See TR		1.4.8.1	Neg Trigger Pulse
NREF	9400-1	9	Conn 3		1.1.12.1	Front Panel Neg Reference
	9400-5	1		1	1.5.2.1	Pots Anticlockwise End
OFFSET1	9400-1	11	G5	1	1.1.31.3	Offset CHAN 1
	9400-1	14	C4	13	1.1.31.2	Offset Control
OFFSET2	9400-1	11	G5	7	1.1.31.1	Offset CHAN 2
	9400-1	15	A4	13	1.1.31.2	Offset Control
PCAL	9400-1	4	K10	11	1.1.12.1	S+H DAC Data Strobe
	9400-1	4	L14	13	1.1.12.1	
PCL	9400-1	11	G4	7	1.1.31.3	Probe Calibration Level
	9400-1	10	E1	4	1.1.35.1	
PDIS	9400-1	4	L13	6	1.1.12.1	Display Data Strobe
	9400-1	4	L15	13	1.1.12.1	
	9400-2	1	A4	12	1.2.2.1	Display Board
	9400-2	1	A4	13	1.2.2.1	
	9400-2	1	B5	11	1.2.2.1	
PGD						Display Board Present
	9400-1	4	K16	5	1.1.16.1	Display Controller
PGDIS	9400-2	1	B4	6	1.2.2.1	Display End of Page
	9400-1	4	040	b	1.1.16.1	Display Controller
	9400-2	1	I3	8	1.2.2.1	
	9400-2	1	H2	8	1.2.2.1	
PGM						EPROM Program Signal or A14 Address
	9400-1	1	EPROM patch		1.1.4.1	
	9400-1	1	L1-4	27	1.1.6.1	
	9400-1	1	U1-4	27	1.1.6.1	
POS IN	9400-1	3	See TR		1.4.8.1	Pos Trig Pulse

PRCAL	9400-1	13	E6	3	1.1.32.1	
	9400-1	10	E1	6	1.1.35.1	
PROBECAL	9400-1	Front	panel		1.1.5.1	Probe Calibration Output
PREF	9400-1	9	Conn	10	1.1.21.1	Front Panel ref +5 V
	9400-5	1		1	1.5.2.1	Pots Clockwise End
PR 0-7	9400-1	1	I18		1.1.6.1	Peripheral Decode
0	9400-6	1	A1	1	1.6.2.1	
0	9400-6	1	A1	15	1.6.2.1	
0	9400-6	1	A2	13	1.6.2.1	
1	9400-4	1	C8	4	1.4.3.1	
2	9400-1	9	G19	10	1.1.20.1	Front Panel Control
2	9400-1	9	G19	13	1.1.20.1	Front Panel Control
2	9400-1	9	G20	1	1.1.20.1	Front Panel Control
3	9400-1	6	J15	4	1.1.18.1	RS232 Interfaces
3	9400-1	6	L3	19	1.1.18.1	RS232 Interfaces
3	9400-1	6	L10	1,4	1.1.18.1	RS232 Interfaces
4	9400-1	7	H15	4	1.1.19.1	Min/max Timing
5	9400-1	7	G20	4+	1.1.22.1	Battery Backup
6	9400-1	4	K16	4	1.1.16.1	Display Controller
6	9400-1	4	L17	1,5	1.1.16.1	Display Controller
7	9400-1	9	G17	6+	1.1.24.1	Timer
PRT	9400-4	1	A5	5	1.4.4.1	Post/pre Trig Select
	9400-4	4	D2	1	1.4.10.1	
RAS	9400-1	4	K21	9	1.1.12.1	DRAM Row Address Strobe
	9400-1	5	K23-	4	1.1.14.1	Dynamic RAM
	9400-1	5	-L30	4	1.1.14.1	
RATE	9400-1	2	K1	6	1.4.3.1	100/50 MHz Select
	9400-3	1	A2	4	1.3.2.1	ADC Board
RESET	9400-1	1	J17	2	1.1.3.1	General Reset Line (Boot with HALT)
RESET	9400-1	2	H29	18	1.1.1.2	General Reset
	9400-1	9	F17	13	1.1.21.1	Front Panel Control
	9400-1	9	F19	12	1.1.21.1	Front Panel Control
	9400-1	2	J15	9	1.1.9.1	
	9400-1	6	K8	10	1.1.18.1	RS232 Interfaces
	9400-1	4	K14	4	1.1.12.1	RAM Controller
	9400-1	2	K15	11	1.1.9.1	
	9400-1	4	L12	12	1.1.12.1	RAM Controller
	9400-1	4	L16	1+	1.1.16.1	Display Controller
	9400-2	1	A2	1	1.2.2.1	Display Board
	9400-2	1	C4	1	1.2.3.1	Display Board
	9400-2	2	Trans	2	1.2.5.1	
	9400-4	1	C7	2	1.4.4.1	
	9400-6	1	A2	1	1.6.2.1	
	9400-6	1	B1	1	1.6.2.1	
	9400-2/n	2	B5	3	1.12.3.1	

RF 0-3	9400-4	1	C8		1.4.4.1	Read Functions
0	9400-4	4	B4	1,11	1.4.12.1	
1	9400-4	5	B3	1,19	1.4.15.1	
2	9400-4	5	B7	1	1.4.15.1	
2	9400-4	1	C6	5	1.4.4.1	
3	9400-4	1	C6	9	1.4.4.1	
3	9400-4	1	E4	3	1.4.7.1	
I	9400-4	1	A5	15	1.4.4.1	Enable Int Roll Mode
	9400-4	1	C6	2	1.4.7.1	
RSEL	9400-1	4	K12	2	1.1.12.1	Internal DRAM Select
	9400-1	6	F18	10	1.1.17.1	Calibration Controller
	9400-1	4	K11	1	1.1.12.1	DRAM Controller
	9400-1	4	K12	5	1.1.12.1	
	9400-1	4	K13	2	1.1.12.1	
	9400-1	4	L12	10	1.1.12.1	
Y	9400-4	3	E3	8	1.4.8.1	Ready
	9400-4	4	A4	7	1.4.12.1	Interpolation TDC
	9400-4	3	G1	6	1.4.8.1	Trigger System
/W	9400-1	2	H29	9	1.1.1.2	Read Write CPU Bus (dir of data)
	9400-1	2	E28	5	1.1.10.1	Bus Buffer
	9400-1	1	I19	3	1.1.4.1	
SCK	9400-1	9	F17	6	1.1.21.1	Front Panel Shift Clock
	9400-1	11	H4	10	1.1.17.1	Calibration Controller
	9400-1	11	H4	10	1.1.31.3	Analog Frontend Control
	9400-1	9	H9	2	1.1.20.1	Front Panel Control
SCKP	9400-1	11	H4	7	1.1.31.3	Front Panel Control Clock
	9400-1	12	F4	9	1.1.31.2	Frontend Control CHAN1
	9400-1	12	F12	8	1.1.31.2	Frontend Control CHAN2
SEX	9400-1	7	H16	5	1.1.19.1	Signed Multiplicator
SIN	9400-1	9	G17	3	1.1.21.1	Front Serial Data Shift in
SINT	9400-1	1	H20	14	1.1.7.1	ORed Interrupt Request
	9400-1	3	DMA slot c10			
SRC	9400-1	4	K13	12	1.1.12.1	Select DRAM Row Col Mux Address
	9400-1	5	C21	1	1.1.13.1	RAM Address Select
	9400-1	5	F21	1	1.1.13.1	
	9400-1	5	K21	8	1.1.13.1	
	9400-1	5	L20	1	1.1.13.1	
	9400-1	4	L10	10	1.1.12.1	RAM Sequencer
SSE	9400-1	7	H10	8	1.1.19.1	Signed Mult CTE
	9400-1	7	I15	5	1.1.19.1	Min/max Timing
	9400-1	8	J9	11	1.1.20.1	Min/max/multiply
STVEC	9400-2	1	B1	9	1.2.2.1	Start Vector
	9400-2	2	D1	10	1.2.3.1	X and Y DACs
SYDIS	9400-1	2	K15	13	1.1.8.1	Display Line Synchronization
	9400-2	1	B2	2	1.2.3.1	Display Board
SYNC	9400-4	2	I3	2,5	1.4.6.1	Sample Sync
	9400-3	3	B1	4,5	1.3.1.1	ADC Board
T	9400-1	A13	See TR		1.1.32.1	Trig to 9400-4 TDC
TCH1	9400-1	14	Q13	Em	1.1.31.1	CHAN 1 Trigger
	9400-1	13	switch 3		1.1.32.1	

TCH2	9400-1	15	Q10	Em	1.1.31.1	CHAN 2 Trigger
	9400-1	13	switch 2		1.1.32.1	
TCL	9400-1	4	L16	5	1.1.16.1	Clear State Abort
	9400-1	4	K16	2	1.1.16.1	
	9400-1	4	L16	12	1.1.16.1	
	9400-1	1	J17	9	1.1.3.1	Power on Reset
TD	9400-4	3	G4	4	1.4.8.1	Trigger System
	9400-4	4	A4	14	1.4.12.1	Interpolation TDC
	9400-4	4	C4	1	1.4.10.1	A and B Delay
	9400-4	4	C4	13		
TEST	DMA	3	slot a3		1.1.11.1	Test Mode for 4928 Tester (disable auto reboot)
	9400-1	1	J19	3	1.1.3.1	
TR	9400-1	13	A13	3	1.1.32.1	Pos Trig to 9400-4
	9400-4		K8	10	1.4.8.1	Triger System
TR bar	9400-1	13	A13	2	1.1.32.1	Neg Trig to 9400-4
TRIGHI	9400-1	11	G4	14	1.1.31.3	High Trig Threshold
	9400-1	13	B13	8	1.1.32.1	
TRIGLO	9400-1	11	G4	8	1.1.31.3	Low Trig Threshold
	9400-1	13	B13	5	1.1.32.1	
T2	9400-1	4	K17	13	1.1.15.1	4 MHz Clock
T3	9400-1	4	K17	6	1.1.15.1	2 MHz Clock
	9400-1	4	K18	13	1.1.15.1	
T 4-11	9400-1	4	K18		1.1.15.1	Derived Clocks
8	9400-1	4	L14	3	1.1.12.1	
8	9401-2/n	2	A1	11	1.12.3.1	
9	9401-2/n	3	B1	1	1.13.3.1	
9	9401-2/n	3	C5	6	1.12.3.1	
11	9400-1	4	L14	11	1.1.12.1	
T 12-15	9400-1	4	K20		1.1.15.1	Derived Clocks
12-14	9400-1	5	J22		1.1.17.1	
12-14	9400-1	5	L20		1.1.13.1	
14	9400-1	9	F19	9	1.1.24.1	
14	9400-1	9	H7	1	1.1.24.1	
14	9400-1	10	E1	9	1.1.35.1	
UDS	9400-1	2	H29	7	1.1.1.2	Upper Byte Data Bus Strobe (word transf with LDS)
	9400-1	2	E28	3	1.1.10.1	
VPA	9400-1	1	L13	11	1.1.5.1	Valid 68000 Mode Interrupt Peripheral Address
	9400-1	2	H29	21	1.1.1.2	
VX	9400-2	2	G3	2	1.2.3.1	X Velocity
	9400-2	3	Q19		1.2.6.2	X Integrator
	9400-2	3	Q20		1.2.6.2	
	9400-2	3	Q22	c	1.2.6.2	
VY	9400-2	2	G1	2	1.2.3.1	Y Velocity
	9400-2	4	Q4		1.2.6.2*	Integrator
	9400-2	4	Q5		1.2.6.2*	
	9400-2	4	Q7	c	1.2.6.2*	

WEL	9400-1	4	K21	7	1.1.12.1	DRAM Lower Byte Write Strobe
WEU	9400-1	4	K21	3	1.1.12.1	DRAM Upper Byte Write Strobe
WF0-3	9400-4	1	C8		1.4.3.1	Write Functions
WRVEC	9400-2	3	Same as		EOVX and EOVY	
WTVEC	9400-2	2	C2	10	1.2.4.1	
X	9400-2	2	G4	2	1.2.3.1	X DAC Output
XX	9400-1	ADC slot		a17	1.1.11.1	ADC Slot Select
	9400-3	6	H6	2	1.3.10.1	
Y	9400-2	2	G2	2	1.2.3.1	Y DAC Output
YY	9400-1	ADC slot		c15	1.1.11.1	ADC Slot Select
	9400-3	6	H6	11	1.3.10.1	
Z	9400-2	2	J3	2	1.2.4.1	Z DAC Output
ZC	9400-7	1	Conn		1.7.1.1	Z Cutoff
+3 V	9400-1	16	G10	out	1.1.37.1	Analog Power
-3 V	9400-1	16	E10	out	1.1.37.1	Analog Power
+12 V	9400-1	16	F10	out	1.1.37.1	Analog Power
-12 V	9400-1	16	F11	out	1.1.37.1	Analog Power
+12 V	9400-4	6	I7	4	1.4.19.1	Analog Power
-12 V	9400-4	6	I7	11	1.4.19.1	Analog Power

1.21 Bus Finder

This section lists the buses of the 9400 DSO and their sources and destinations to board level and page number of schematic.

A	1-23	Address bus (unbuffered) of the 6800 CPU		
	19-21	9400-1	1	Address space bank decoder
	1-17	9400-1	1	EPROMS
	16-18	9400-1	1	Peripheral decoder
	1-23	9400-1	2	68000 CPU
	1-23	9400-1	2	Adress buffer
ANI	38-46	Analog bus - analog data from frontend and front panel to ADC		
	38-46	9400-1	9	Front panel logic
	38-40	9400-1	11	50 ohm overload detection
	42	9400-1	13	Trigger signal
	44	9400-1	9	Temperature measurement
	46	9400-1	10	Probe calibrator control
	38-46	9400-5	1	Front panel board
BA	1-23	Address bus (buffered) of the 68000 CPU		
	1-23	9400-1	3	DMA slot
	1-16	9400-1	5	RAM address select
	1-3	9400-1	6	RS232 interfaces
	1-11	9400-1	7	Backup RAM
	1-5	9400-1	9	Front panel logic - see FA
	1-3	9400-3	6	ADC boards
	4-15	9400-3	7	ADC boards
	1-2	9400-4	1	TDC board
	1-3 5-6 14	9400-6	1	GPIB board
	1-3 5-6 14	9401-2	1	GPIB board
	9 18	9401-2	2	Extra RAM
	2-17	9401-2	3	Extra RAM
BD	0-15	Data bus (buffered) of the 68000 CPU		
	0-15	9400-1	2	Data buffer
	0-15	9400-1	2	Terminations
	0-15	9400-1	3	ADC slots
	0-15	9400-1	3	DMA slot
	0-15	9400-1	3	TDC slot
	0-1	9400-1	4	Display controller
	0-15	9400-1	5	DRAM
	8-15	9400-1	6	RS232 interfaces
	0-7	9400-1	7	Backup RAM
	1 22-23	9400-1	7	Min/max/mult timing
	0-15	9400-1	8	Min/max/mult

	0-11	9400-1	9	Front panel logic - see FD/V
	0-15	9400-1	9	Timer
	0-15	9400-3	6	ADC boards a20-27 + c20-27
	0-15	9400-4	1	TDC board
	0-15	9400-6	1	GPIB board
	0-15	9401-2	1	GPIB board
	0-15	9401-2	3	Extra RAM
BK	0-7	Address space banks		
		9400-1	1	Bank decoder
	0	9400-1	1	EPROMs
	0	9400-1	2	Data bus buffer
	1			Spare
	2			Spare
	3	9400-1	1	Peripheral decoder
	4	9400-1	4	DRAM controller
	4	9400-1	2	Data bus buffer
	5			Spare
	6	9400-1	3	ADC slots
	6	9400-3	6	ADC boards
	7	9400-1	3	DMA slot
	7	9401-2	2	Extra RAM
BKPR		Banks and peripherals BK + PR - see under BK and PR for details		
		9400-1	1	Bank and peripheral decoders
BS		BACK BATT CK HALT RESET SYDIS TCL T2-15		
		9400-1	4	RAM controller
		9400-1	7	Backup RAM
		9400-1	7	Min/max/mult timing
		9400-1	9	Front panel logic
BT		BAS BLDS BUDS BRW BWR		
		9400-1	2	Buffered memory controls
		9400-1	4	Clock generator
		9400-1	4	Display controller
		9400-1	9	Front panel logic
		9400-3	6	ADC boards
		9400-4	1	TDC board
		9401-2	2	Extra RAM
		9401-2	3	Extra RAM
C	11-28	Frontend Attenuation and couplings		
	11-13	9400-1	12	Q1-3 Couplings
	11-13	9400-1	14	Relays Couplings
	16-18	9400-1	12	F4 Attenuation
	16-18	9400-1	14	C4 Attenuation
	21-23	9400-1	12	Q33-35 Couplings
	21-23	9400-1	15	Relays Couplings
	26-28	9400-1	12	F12 Attenuation
	26-28	9400-1	15	A4 Attenuation

CA	1-3	Address bus for analog frontend control		
		9400-1	5	Calibration register
		9400-1	11	Analog frontend control
CAL		ACAL GNDCAL CA CALEN CD		
		9400-1	5	Calibration register
		9400-1	6	Calibration DAC
CD	0-12	Digital data for calibration system		
	0-12	9400-1	5	Calibration register
	0-11	9400-1	6	Calibration DAC
CS	11-28	Frontend controls		
	11-18	9400-1	12	Digital frontend controller
	11-18	9400-1	14	Frontend hybrids control
	21-28	9400-1	15	
	0	9400-1	9	Front panel serial data line
D	0-15	Data bus (unbuffered) of the 68000 CPU		
	0-15	9400-1	1	EPROMs
	0-15	9400-1	2	68000 CPU
	0-15	9400-1	2	Data buffer
DA	1-14	Address bus for display controller		
	1-14	9400-1	4	Display controller
	1-14	9400-1	5	RAM address select
FA	1-5	Front panel address		
	1-5	9400-1	9	Front panel address
	1-5	9400-5	1	Front panel board
FC	0-1			
	0-1	9400-1	1	Bank decoder control
	0-1	9400-1	2	Bank decoder control
FD	0-11	Front panel data		
	0-11	9400-1	9	Front panel logic
	0-11	9400-5	2	Front panel board
INT	1-7	Interrupt lines		
		9400-1	1	Interrupt decoder
	1	9400-1	9	Front panel logic
	2	9400-1	3	DMA slot
	3	9400-1	6	RS232 interface port 1
	4	9400-1	6	RS232 interface port 2
	5	9400-1	3	TDC slot
	5	9400-4	1	TDC board
	6	9400-1	3	GPIB slot
	6	9400-6	1	GPIB board
	6	9401-2	1	GPIB board
	7	9400-1	3	Test slot
IPL	0-2	Encoded interrupt bus		
	0-2	9400-1	1	Int lines from int decoder
	0-2	9400-1	2	Int lines to 68000

LA	0-7	Address bus in RAM address select		
	0-7	9400-1	5	RAM address select
LD	0-15	Data bus for min/max/mult circuit		
	0-15	9400-1	8	Min/max/mult circuit
MA	0-7	DRAM multiplexed address bus		
	0-7	9400-1	5	RAM address select
	0-7	9400-1	5	DRAM address pins
MD	0-15	Data bus for min/max/mult		
	0-15	9400-1	8	Min/max/mult
PR	0-7	Peripherals addressing		
		9400-1	1	Peripheral decoder
	1	9400-1	3	RDC slot
	1	9400-4	1	TDC board
	2	9400-1	9	Front panel logic
	3	9400-1	6	RS232 interfaces
	4	9400-1	7	Min/max/mult timing
	5	9400-1	7	Backup RAM
	6	9400-1	4	Display controller
	7	9400-1	9	Timer
RR	0-15	Data read bus		
	0-15	9400-1	2	Bus buffer
	0-12	9400-1	5	Calibration register
	0-15	9400-1	5	DRAM
	0-15	9400-1	4	Display slot
	0-15	9400-2	1	Display board
S	0-7	RS232 data		
	0-7	9400-1	6	RS232 select/buffer
	0-7	9400-1	6	RS232 port 1
	0-7	9400-1	6	RS232 port 2
T	2-15	9400-1	4	Clock generator
	12-14	9400-1	5	Calibration register
	14	9400-1	10	Probe calibrator
	14	9400-1	9	Timer
TA	5-15	Address bus from 9400-4 to 9400-3 boards		
	5-15	9400-1	3	ADC and TDC slots
	5-15	9400-3	7	ADC boards
	5-15	9400-4	5	TDC board
V	0-15	Data for front panel and calibration		
	4-11	9400-1	9	ADC for front panel/frontend
	0-11	9400-1	9	Data bus for FD to front panel

1.23 GPIB or IEEE-488 Interface

1.23.1 Introduction

This section is a simple description of the GPIB interface as an aid to understanding the interface in the 9400 DSO: it is not intended as a complete specification of the system.

The GPIB system is designed for the interaction of a number of interacting devices, which may transmit or receive information as required. The system includes data lines over which the actual data are sent, bus management lines for control, and handshake lines to ensure correct acceptance of data at the right destination. The main features of the bus are summarized below:

Maximum number of devices	15	
Maximum bus length	20	meters or
	2	meters per device, whichever is less
Connection		star or chain

Note that more than half of any connected devices must be powered up, even if they will not be used.

Data lines	8	DIO 1 to 8
Handshake lines	DAV	Data available
	NRFD	Not ready for data
	NDAC	Not data accepted
Bus management lines	EOI	End or identity
	IFC	Interface clear
	SRQ	Service request
	ATN	Attention
	REN	Remote enable
Active level	+0.4 V	
Inactive level	+3.3 V	

Note that all signal lines are active low, and that they are wire ORed to allow participation by all devices.

In addition, there are 8 ground lines, making a total of 24 lines. A diagram of the connector will be found in Section 4, Connectors and Cables.

1.23.2 Functions in the GPIB

In order to allow satisfactory interconnection of several devices the following functions must be provided -

- Enabling any device to transmit data
- Preventing any device from transmitting data
- Enabling any device to receive data
- Preventing any device from receiving data
- Transmitting data to a specific device
- Ensuring that only one device is transmitting
- Ensuring that transmitting takes place only when reception is possible
- Enabling any device to request servicing
- Identify type of data to be sent

Any device can be activated into the "talk" or "listen" state, and can be de-activated by the commands "untalk" and "unlisten". Also a device can be a "controller".

Maximum number of current talkers	1
Maximum number of current listeners	14
Maximum number of current controllers	1

Function of bus lines:

- DAV Data AVailable; talker says the data on the line are valid.

- NRFD Not Ready For Data; listener says it is not ready for more data. All listeners must release the NRFD line, i.e., let it go high, before talker can send.

- NDAC Not Data Accepted; listener says it has not yet accepted the data. Talker must hold all data lines steady until all listeners have released this line, i.e., it goes high.

Clearly, the NRFD and NDAC are easy to implement by a wired OR system, so that any one device asserting the signal prevents progress to the next step. Progress is made at the speed of the slowest listener. A simple timing diagram is given in <1.1.23.1>, and another way of presenting the system is given in <1.1.23.2>.

The bus management lines function as follows:

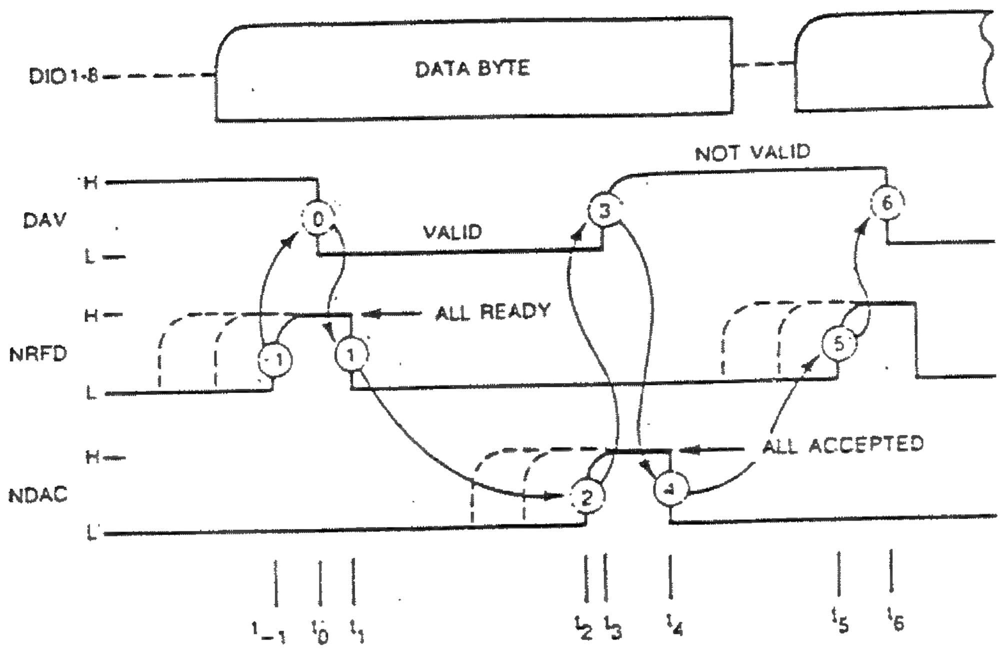
- EOI End Or Identify; talker sends this with last byte of a block transfer to indicate last byte. Also used with ATN to parallel poll devices for their Status Bit.
- IFC InterFace Clear; places the GPIB system into a quiescent state.
- SRQ Service ReQuest; any device can send it to the controller to indicate need for attention, and to request interruption of current operations.
- ATN ATteNtion; controller sends this to specify whether DIO lines are to be used for interface messages, e.g., addressing, or for data.
- REN Remote ENable; selects a device as being under local or remote control

Addressing of the devices on the GPIB bus is made by a switch which can select values from 0 to 30.

For more detailed information on the GPIB bus consult a specialized GPIB-IEEE488 document.

The principles of GPIB are quite simple - the system must wait for all users, and lines are wire ORed so that all can pull the lines down.

The handshake sequence is illustrated in two ways. In <1.1.23.1> the signal waveforms are sketched, while <1.1.23.2> is a flowchart.

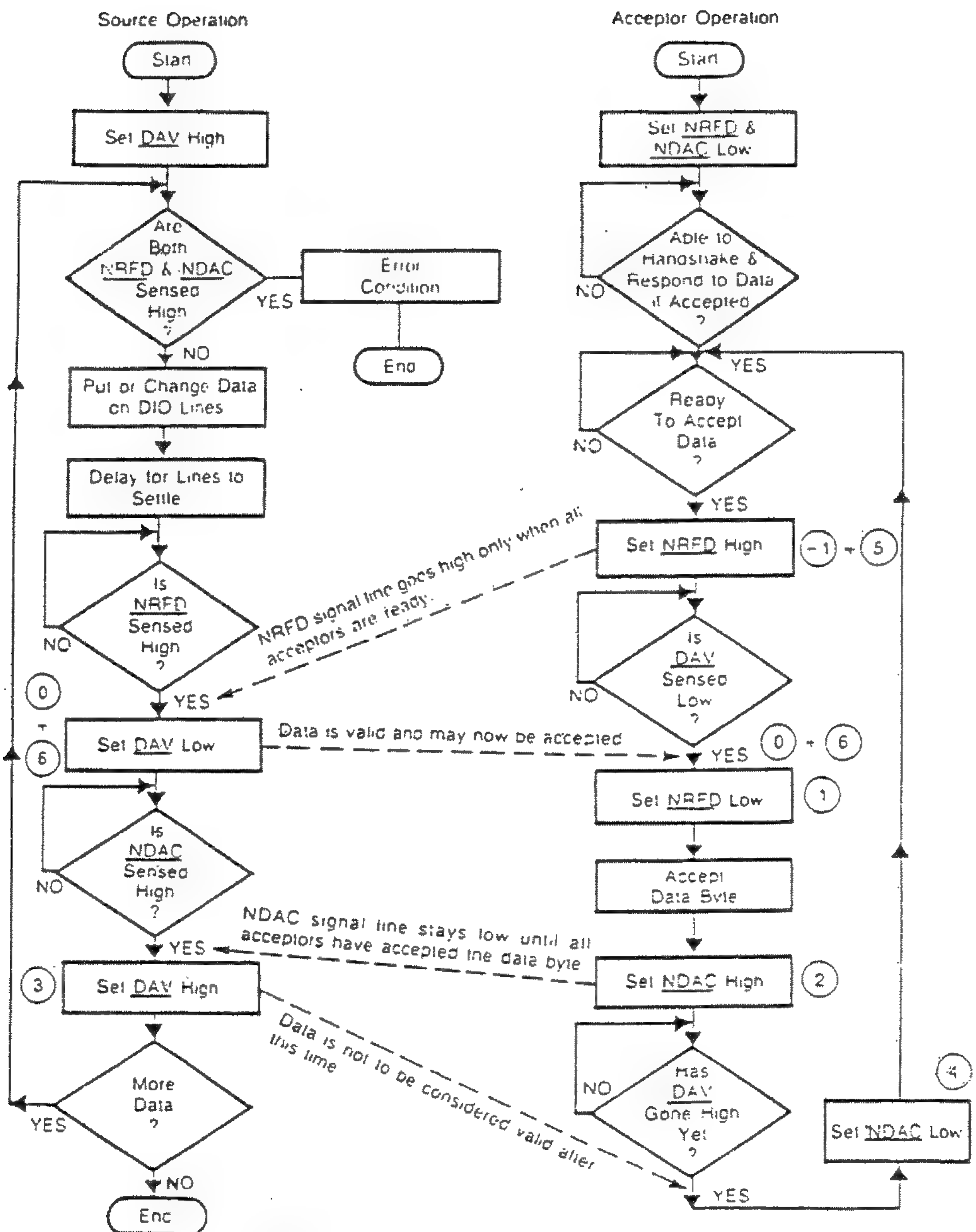


DATA BYTE TRANSFER IN GPIB IEEE-488

Figure 1.1.23.1

The handshake timing sequence proceeds as follows:

Preliminary	The source checks for presence of listeners and places the next data byte on the data lines DIO1-8.
t-1	Acceptors one by one become ready for byte. Last one allows NRFD to go high.
t0	Sources pulls down DAV to validate data.
t1	The first listener to accept the data pulls down NRFD to show it is no longer ready for a new byte.
t2	The listeners one by one accept the data, and the last one lets NDAC go high.
t3	The source sets DAV high to show this byte is no longer valid.
t4	The listeners one by one accept this, the first one pulling NDAC low for the next cycle.
t5	As for t-1.



Logical flow of events for Source and Acceptor when transferring data using the handshake process

HANDSHAKE TIMING SEQUENCE IN GPIB IEEE-488

Figure 1.1.32.2

CHAPTER 2

TEST, ADJUSTMENT, CALIBRATION, FAULT FINDING and REPAIR

Table of Contents

Note:

In this chapter, screen "division" refers to the squares or boxes, i.e. five small divisions.

2.0 Introduction

This chapter is intended primarily for those who may have to test, modify, upgrade or repair a 9400 in the field, i.e. without the specialized test gear which is available at the large LeCroy offices. It will be assumed that the reader only has the normal electronic workshop facilities, but he should have the use of the following:

- Tektronix 485 analog scope or other fast scope
- Good FET probe for the above
- Function generator
- EHT dummy load or safe receptacle for an EHT cable

Because of the complex nature of the 9400 the provision of an exhaustive diagnostic system is not feasible: what is provided here is an attempt to give enough guidance to locate a fault to the correct board, and perhaps to pin-point the fault in easy cases. The arrangement of the boards within the 9400 <5.0.2> means that access to parts of the 9400-2 and 9400-3 boards is impossible, as is access to any part of the 9400-4. The two 9400-3 boards can, of course, be interchanged for test purposes, but should generally be replaced afterwards.

To make best use of this chapter, reference to the appropriate section of Chapter 1, the functional description, may be needed.

The usefulness of this chapter could be increased as more 9400s are delivered, if anyone who has useful ideas will send them to LeCroy SA or LeCroy Corporation for forwarding. Although in principle the standard repair report is a source of data on faults, it does not normally carry many details of procedures.

BASIC PERFORMANCE TEST PROCEDURE

2.1 Introduction

This chapter describes 9400 tests which require the use of LeCroy software. The 9400 software includes a small number of test routines which can be controlled from the front panel - these are described in Section 2. Because the system is easy to use, only a few of the operations are described in detail in this section.

Note

The following sections apply only to versions V2.0 and higher. If your Model 9400 has an earlier software version (check on the upper right-hand corner of the "Memory STATUS" display page), please ask your LeCroy contact for an update of your oscilloscope's software.

For further information on the comprehensive software package CALSOFT (order code CS01, CS02) for 9400 adjustment and calibration, refer to the CALSOFT operator's manual.

2.1.1 Turn-on

1. Check that the correct line voltage is set on the rear-panel power connector.

2. Check the following:

   a) that the display comes on after about 10 sec.

   b) that the display is stable (if traces are displayed, turn them all off).

   c) that the range of INTENSITY and GRID INTENSITY is reasonable.

3. Wait about 10 minutes for the 9400 to reach a stable temperature.

2.1.2 Test for Low Frequency Noise on the Input

This test verifies that the front-end components, ADC and power supplies operate correctly. Low frequency noise may be observed if any of the power supplies oscillate.

1. Turn on the Channel 1 and 2 traces, turn the others off.

2. Set the 9400 so that a single grid is displayed on the screen.

3. Set the controls of the 9400 as follows:

   a) Input coupling: 1 MΩ, DC (Channels 1 and 2)
   b) Fixed gain: 5 mV/div (Channels 1 and 2)
   c) Variable gain: 1 (Channels 1 and 2)

   d) Trigger - Slope: pos. or neg.
   Source: LINE
   Coupling: DC
   Mode: NORM
   Delay: zero

4. Setting the time base to 10, 5, 2, 1, and 0.5 msec/div in turn, check:

   a) that the displayed waveforms are constant bands less than 2/5 of a vertical division wide.
   b) that there is no discernible periodic structure.

5. Using the offset control, move the Channel 1 and Channel 2 traces slowly through the entire range and check that there is no change in the displayed trace. This is best seen by displaying only one trace at a time.

Solution to Problems

If there is a low frequency structure of the order of 1 kHz, check the following:

a) Is the lower RF-shield of the front-end correctly installed? In some of the older versions, the screw head which holds the right-hand front foot of the lower 9400 cover may push the RF-shield towards the 9400-1 main board, creating shorts circuits. Verify that the absence of the lower 9400 cover has no effect on the noise problem.

b) Have any of the 4 supply voltages oscillations of more than 50 mV (peak-to-peak) amplitude in the frequency range of 50 Hz to 200 kHz (check for time-base settings 10 msec/div through 10 µsec/div). If this is the case, the power supply must be repaired. Note that power supply oscillations may occur particularly at high temperatures (use a heat gun to verify a repair).

2.1.3 Offset

1. Set up the 9400 as follows:

   a) Channel 1: on (turn off all the others)
   b) Volts/div: 5 mV/div
   c) Time base: 10 msec/div

   d) Trigger - Mode: Norm
   - Source: line
   - Slope: Pos. or neg.
   - Input set to GND

2. Switch the bandwidth limit on and then off again to calibrate both channels.

3. Center the trace in the middle of the screen.

4. Switching between a) 1 MΩ: DC and GND,
   b) 50 Ω: DC and GND,
   c) 50 Ω: AC input and GND,

   check that the trace does not vary more than 1 minor division, approximately 1 mV.

5. Repeat steps 1 through 4 with Channel 2 on and Channel 1 off.

6. If any channel fails the offset test, measure the input impedance in the 1 MΩ and 50.5 Ω DC modes with an ohmmeter. The readings should be within 1%.

2.1.4 Front-end Check

1. Set up the 9400 as follows:

   a) Channel 1 on, (all other traces off)
   b) Trigger - Source: Ch 1,
   - Coupling: DC coupling
   - Mode: norm
   - Delay: 0
   - trigger level: 0.00 div.
   - Slope: negative or positive

c) Channel 1: Volts/div: 1 V/div,
Time base: 0.1 µsec/div.
Signal coupling: 50 Ω

2. Connect a 6 V p-p 1 MHz square wave from a function generator (50 Ω output) to CH 1.

3. Set the interleaved sampling mode on.

4. Check the following:

   - On the rising and falling edges there should not be a large (e.g. + 20%) overshoot.

5. Repeat step 4 using a 600 mV p-p signal with Channel 1 Volts/div set to 0.1 V/div.

6. Repeat step 4 using a 60 mV p-p signal with Channel 1 Volts/div set to 10 mV/div.

7. Repeat steps 1 through 6 for CH 2 (trigger source CH 2).

8. When both channels have been checked at 50 Ω, use an in-line 50 Ω terminator and set the 9400 to 1 MΩ input, DC coupling. Repeat steps 1 to 7 for both channels using these new settings.

2.1.5 Preparation for Internal Tests

The 9400 is capable of executing a number of autonomous tests, the results of which are stored in reference memory C, and normally accessed through the (expanded) display controls. Whenever the test menu is entered (see Section 7), the entire Memory C buffer is cleared and the 9400 is set to display the expansion of Memory C under trace "EXPAND A". When each individual test is performed, the 9400 automatically expands the display and centers it on the newly acquired histogram. You may nevertheless use the manual controls of "EXPAND A" to further modify the display, if required.

2.1.6 Entering the Internal Test Menu

1. Ensure that the 9400 is in the "root" menu, i.e. only "Main Menu" should appear to the left of the grid. Otherwise push the "Return" button until this is the case.

2. While keeping the lowest menu button (the one above SCREEN DUMP) pressed, push the top button, "Main Menu". The "Test Modes" menu should appear.

3. To make sure that the 9400 triggers, set the trigger controls as follows:

    Trigger source: LINE
    Trigger mode: NORM

This ensures that the front-end is recalibrated whenever the input conditions are modified during the following test procedures.

2.1.7 Internal TDC Calibration

The 9400 calibrates the 10 psec time interpolator on the 100 MHz time base when the time base is modified. If this calibration fails (i.e. one of the peaks described below is missing), this may give rise to "jumps" in the display of INTERLEAVED waveforms at intervals of 10 nsec.

1. Push the fourth soft key "TDC-Cal, int. trig.". Within less than a second, the distribution displayed in the upper screen picture in Figure 1 should appear.

2. Check that the distribution contains 2 peaks, each at least 2 vertical divisions high.

3. Use the Position knob to center the left-hand peak on the display.

4. Turn the Time Magnifier knob clockwise to expand to 5 µsec/div.

5. Check that the width of the distribution is more than 1 horizontal division.

6. Repeat steps 3, 4 and 5 for the right-hand peak.

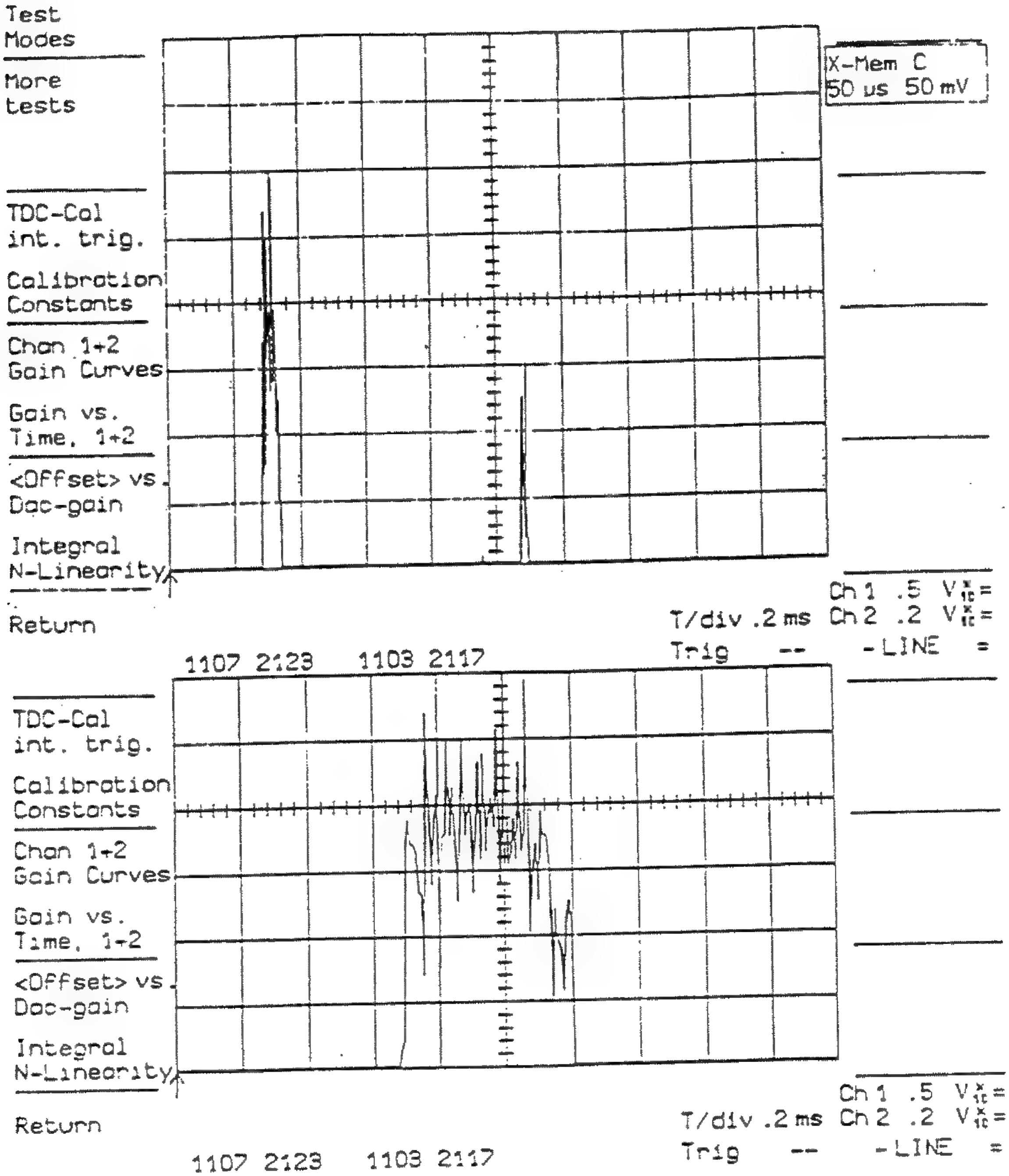
Solution to Problems

If either peak is missing or is too narrow, adjust the timing capacitor (TEST DLY ADJ) on the 9400-4 time-base card as follows:

1. Remove the top cover.

2. Locate the capacitor which is about 2 inches below the rear edge of the 9400-8 timing bus card.

3. Turn the capacitor 1/8 of a turn either way and check its effect by redoing the measurement, i.e. by pushing "TDC-Cal, int. trig."



INITIAL AND EXPANDED TDC TEST WAVEFORM

Figure 1

2.1.8 Gain Curves

This test allows the user to check whether the dynamic range of the programmable input amplifiers is sufficient. If it is not, the 9400 cannot calibrate itself correctly, and the ground line jumps when the bandwidth limit is switch on and off.

1. Set the bandwidth limit OFF.

2. Set the Channels 1 and 2 VOLTS/DIV controls to 5 mV/div.

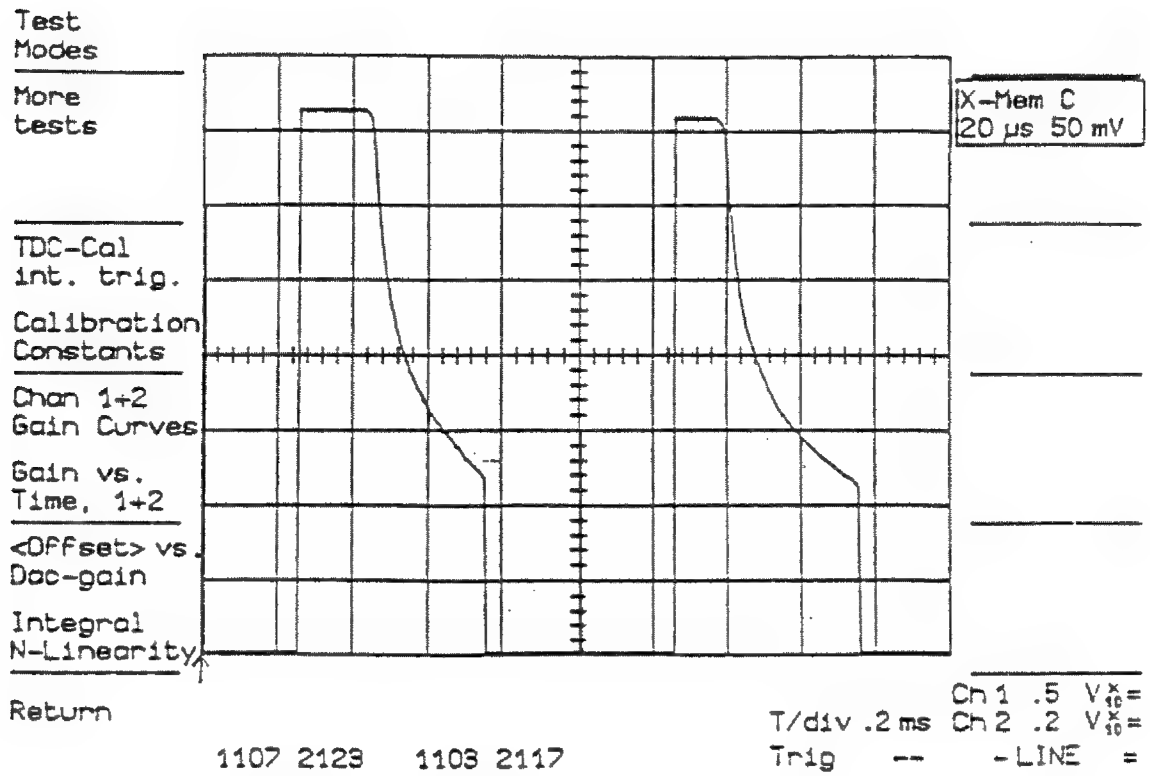
3. Push the soft key "Chan 1 and 2 Gain Curves". The gain curves should appear within 5 seconds.

4. Check that the 2 gain curves (shown in Figure 2):

   a) are at least 1/4 division above the gain = 1 line on the left flat-top.

   b) decrease to at least 1/4 division below the gain = 0.4 line.

5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:
   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF



GAIN CURVES

Figure 2

2.1.9 Gain vs. Time

This test permits the user to verify that the 9400 reliably measures the gain of the front-end amplifiers. It may not do so if there is noise present which influences the gain measurement. In this case, the calibration of the front-end may not work.

Note: this test is performed with the calibrated gain set to 1.00. The vertical scale is changed to 1 percent per division for easier observation. The absolute position of the measured gain is a measure of the precision of the gain calibration.

1. Set the Bandwidth Limit OFF.

2. Set the VOLTS/DIV control of Channels 1 and 2 to 5 mV/div.

3. Press the soft key "Gain vs. Time, 1 + 2". The new distributions should appear within 15 seconds.

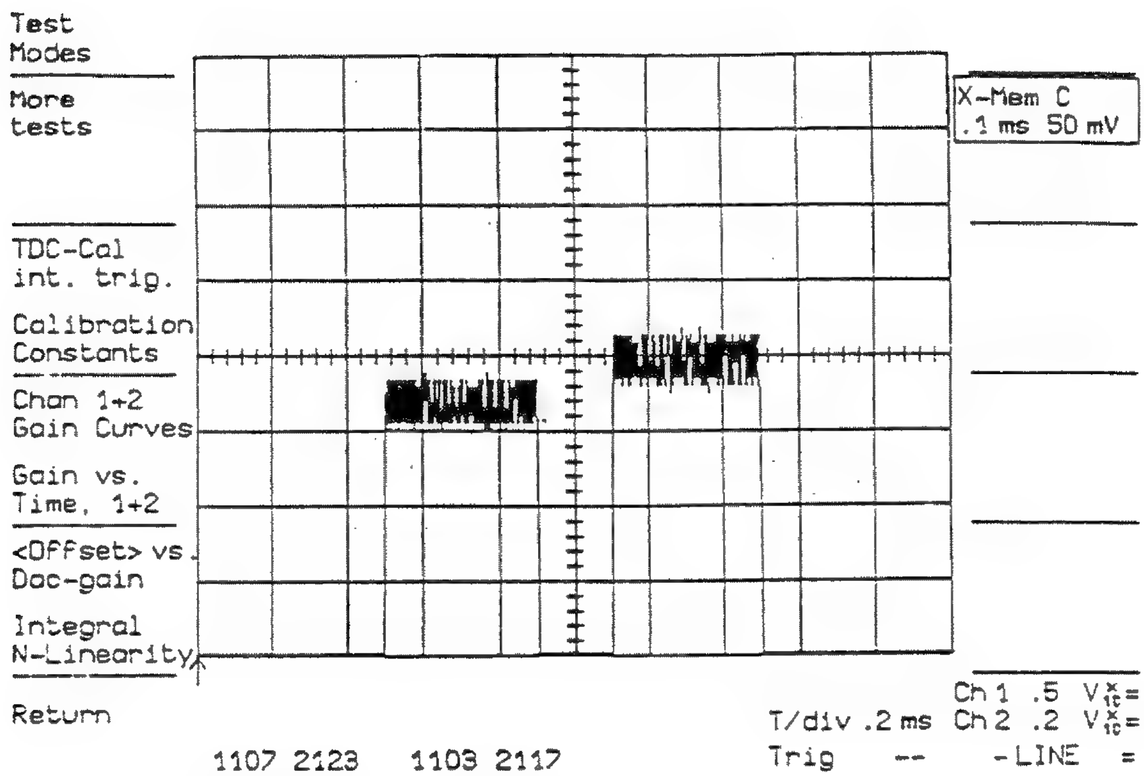
4. Check the two curves (which should resemble those shown in Figure 3) as follows:
   The deviation from the center (1.0 gain) line should be within the following limits.

Gain	1% DSO	2% DSO
5 mV/div	± 1.5%	± 2%
other	± 0.8%	± 1.5%

5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:
   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF.
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF.

Solution to Problems

If the width of the band is too large, check for low-frequency noise, (see Section 3).



GAIN VS. TIME CURVES

Figure 3

2.1.10 <Offset> vs. Gain-DAC

This test permits the user to check if the offset of the second front-end amplifier has been correctly adjusted.

1. Set the Bandwidth Limit OFF.

2. Set the VOLTS/DIV control of Channels 1 and 2 to 5 mV/div.

3. Press the menu button "<Offset> vs. Dac-gain". The new curves should appear within 20 seconds.

4. Check the two offset curves (as shown in Figure 4)

   a) the curves should be rather horizontal, i.e. the difference between the left edge and the right edge should be less than 1 vertical division.

   b) the vertical position of the curve should lie in the 4 major central divisions.

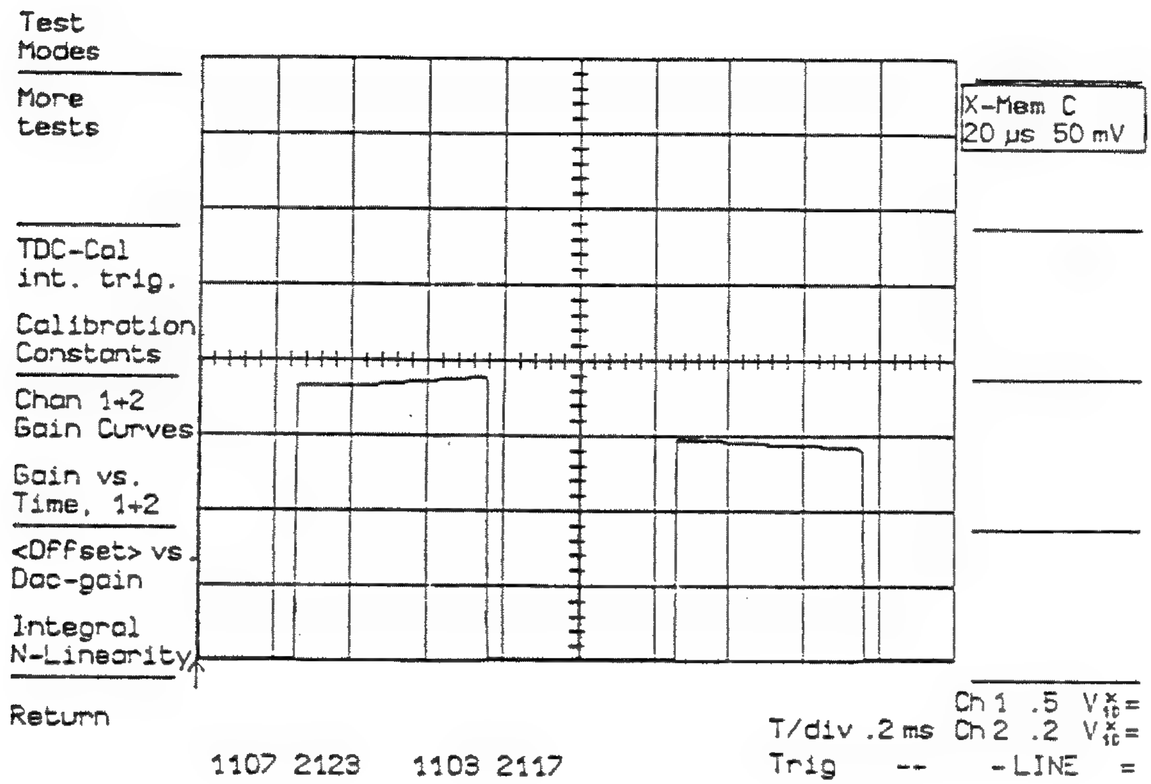
5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:

   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF.
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF.

NOTE: Since the adjustment of the output offset of the HVV200 is common to bandwidth limit ON and OFF, check that the deviations from a horizontal curve are as symmetrical as possible, i.e. by equal amounts above and below the center.

Solution to Problems

If an offset curve is not horizontal enough, the offset of the second amplifier (within the HVV200) must be readjusted. This requires a repetition of the calibration of the output offset of the corresponding HVV200.



OFFSET VS. GAIN DAC

Figure 4

2.1.11 Integral Non-Linearity

This test allows the user to check the DC integral non-linearity and the offset-calibration of the front-end amplifiers.

1. Set the Bandwidth Limit OFF.

2. Set the VOLTS/DIV control of channels 1 and 2 to 5 mV/div.

3. Press the soft key "Integral N-Linearity". The new curves should appear within about 10 seconds.

4. Check the integral non-linearity curves. (Figure 5 shows an example where the results for channel 1 are not satisfactory.)

   The curves must be within the following deviation from the center (0%) line. (1 division = 1%.)

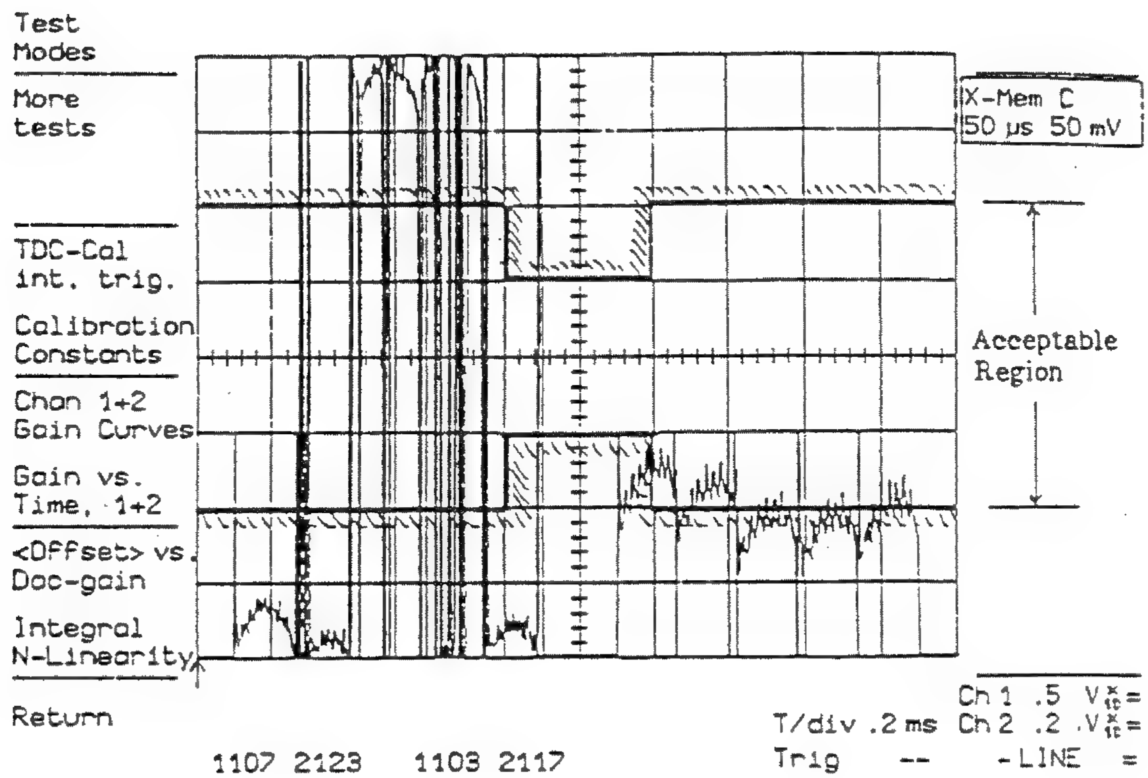
Curve	0 (leftmost)	1	2	3	4 (rightmost)
Gain					
5 mV/div	2.5%	2%	2%	2%	2.5%
other	2%	2%	1.5%	2%	2%

5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:

   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF.
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF.

Solution to Problems

If any of the curves is outside the limits, the HVV200 of the corresponding channel has an integral non-linearity out of specification and should be exchanged. However, a bad offset calibration may give rise to deviations outside this tolerance. This would show up as a systematic vertical offset of the outermost curves (of the 5 sub-curves) with respect to the other curves.



INTEGRAL NON-LINEARITY CURVES

Figure 5

2.1.12 Bandwidth Test at 50 Ω Input Impedance

The purpose of this test is ensure that the entire 9400 system has a bandwidth within specification at 50 Ω input impedance.

1. Set up a Tektronix SG 503 Leveled Sine Wave Generator or equivalent instrument as follows:

   a) Frequency: approximately 0.5 MHz
   b) Amplitude Multiplier: × 1
   c) Output Amplitude 5.0

2. Connect the output of the SG 503 to the Channel 1 input of 9400

3. Set the 9400 as follows:

   a) Channel 1 trace: On (turn off all other traces)

   b) Trigger: Slope: pos. or neg.
      Source: CHAN 1
      Coupling: DC
      Mode: NORM
      Delay: ZERO
      Level: 0.00 div

   c) Channel 1 input: Signal coupling: 50 Ω
      Gain: 1 V/div
      Var. Gain: 1
      Offset: about 0

   d) Time base: 0.5 µsec/div

   e) Interleaved sampling: ON

   f) Bandwidth Limit: OFF

4. Adjust the SG 503 Output Amplitude and Channel 1 offset to get a 5 division peak-to-peak sine wave.

5. Increase the SG 503 frequency while decreasing the Time/div until the sine wave peak-to-peak amplitude is 0.7 x 5 divisions = 3.5 divisions (3 dB point).

6. Read the frequency of the SG 503. The bandwidth specification for the 3 dB point is as follows:

	9400 [MHz]	9400A [MHz]
5 mV/div	125	150
1 V/div	140	225
Other	140	175

7. Connecting the output of the SG 503 to Channel 1 or 2 as required, repeat steps 4 to 6 for the following settings of the 9400.

   a) Channel 2, 1 V/div
   b) Channel 1 and 2, 0.5 V/div
   c) Channel 1 and 2, 0.2 V/div
   d) Channel 1 and 2, 0.1 V/div
   e) Channel 1 and 2, 50 mV/div
   f) Channel 1 and 2, 20 mV/div
   g) Channel 1 and 2, 10 mV/div
   h) Channel 1 and 2, 5 mV/div

8. Repeat steps 1 to 7 with the bandwidth limiter ON. The 3 dB point should now be at 30 MHz ± 20%.

2.1.13 Bandwidth Test at 1 MΩ Input Impedance

The purpose of this test is to ensure that the entire 9400 system has a bandwidth within specification at 1 MΩ input impedance.

1. Set up a Tektronix SG 503 Leveled Sine Wave Generator or equivalent instrument as follows:

   a) Frequency: approximately 0.5 MHz
   b) Amplitude Multiplier: × 1
   c) Output Amplitude 5.0

2. Connect the output of the SG 503 to the Channel 1 input of the 9400 through a 50 Ω feed-through terminator.

3. Set the 9400 as follows:

   a) Channel 1 trace: On (turn off all other traces)

   b) Trigger: Slope: pos. or neg.
   Source: CHAN 1
   Coupling: DC
   Mode: NORM
   Delay: ZERO
   Level: 0.00 div

   c) Channel 1 input: Signal coupling: 1 MΩ
   Gain: 1 V/div
   Var. Gain: 1
   Offset: about 0

   d) Time base: 0.5 μsec/div

   e) Interleaved sampling: ON

   f) Bandwidth Limit: OFF

4. Adjust the SG 503 Output Amplitude and Channel 1 offset to get a 5 division peak-to-peak sine wave.

5. Increase the SG 503 frequency while decreasing the Time/div until the sine wave peak-to-peak amplitude is 0.7 x 5 divisions = 3.5 divisions (3 dB point).

6. Read the frequency of the SG 503. The bandwidth specification for the 3 dB point is as follows:

	9400 [MHz]	9400A [MHz]
≥ 1 mV/div	80	80
Other	85	90

7. Connecting the output of the SG 503 to Channel 1 or 2 as required, repeat steps 4 to 6 for the following settings of the 9400.

   a) Channel 2, 1 V/div
   b) Channel 1 and 2, 0.5 V/div
   c) Channel 1 and 2, 0.2 V/div
   d) Channel 1 and 2, 0.1 V/div
   e) Channel 1 and 2, 50 mV/div
   f) Channel 1 and 2, 20 mV/div
   g) Channel 1 and 2, 10 mV/div
   h) Channel 1 and 2, 5 mV/div

8. Repeat steps 1 to 7 with the bandwidth limiter ON. The 3 dB point should now be at 30 MHz ± 20%.

2.1.14 Trigger Level Test for DC and HF REJ

1. Set up any sine wave generator capable of generating sine waves up to 100 Hz frequency, e.g. an Intron IFG-422 or TFG-8101, as follows:

   Frequency: approximately 100 Hz

2. Connect the output of the generator to the EXTERNAL input of the 9400 and to the Channel 1 input, using a coaxial T-connector (no 50 Ω feed-through terminator). The cable length between EXTERNAL and CHAN 1 should be chosen so that the propagation delay is not greater than 2 nsec.

3. Set the controls of the 9400 as follows:

   a) Full Grid

   b) Turn off all traces, except Channel 1

   c) Time base: 1 msec/div

   d) Channel 1 input: Signal coupling: 1 MΩ, DC
      Gain: 0.5 V/div
      Var. Gain: 1
      Offset: 0

   e) Trigger: Source: CHAN 1
      Mode: NORM
      Delay: 50% Pre-trigger (center of screen)
      Level: 0.00 div

4. Adjust the output amplitude of the sine wave generator to get an 8 division peak-to-peak sine wave, (corresponding to a 2 V amplitude). It is important that the offset of the input be set to zero (use the Panel STATUS menu to verify). Use the offset adjustment of the sine wave generator to center the signal in relation to the screen. Later, the test on the external trigger level requires that the signal should have an absolute range of ± 2 V.

5. Check the sine wave. It should pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position zero (vertical center) within ± 0.6 division.

6. Adjust the 9400 settings as listed first in (a) and then in (b) below. For each, check the resulting sine wave:

   It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position + 3 div (i.e. the second line from the top) within ± 0.6 division.

   a) Trigger Coupling: DC
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: + 3.00 div

   b) Trigger Coupling: HF REJ
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: + 3.00 div

7. Adjust the 9400 settings as listed first in (a) and then in (b) below. For each check the resulting sine wave.

   It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position - 3 div (i.e. the second line from the bottom) within ± 0.6 div.

   a) Trigger Coupling: DC
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: - 3.00 div

   b) Trigger Coupling: HF REJ
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: - 3.00 div

8. Disconnect the input from Channel 1 and connect it to input of Channel 2.

9. Turn off all traces, except Channel 2.

10. Set Input Channel 2: Coupling: 1 MΩ, DC
    Gain: 0.5 V/div
    Var. Gain: 1
    Offset: 0

11. Set Trigger Source to CHAN 2.

12. Repeat steps 4 through 7 for channel 2.

13. Leave the input connected to Channel 2 and leave Channel 2 on.

14. Set Trigger Source to EXT.

15. With the trigger level set first to + 1.5 V and then - 1.5 V, repeat steps 4 through 7 for the EXTERNAL trigger. Observe the effect on channel 2. Tolerance for the checkpoints: ± 0.8 div.

2.1.15 Trigger Level Test for AC and LF REJ

1. Set any sine wave generator capable of generating sine waves up to 2 MHz frequency, e.g. an Intron IFG-422 or TFG-8101 or Tektronix SG 503 LEVELED SINE WAVE GENERATOR, as follows:

   Frequency: approximately 2 MHz

2. Connect the output of the generator to the EXTERNAL input of the 9400 and to the Channel 1 input, using a coaxial T-connector. The cable length between EXTERNAL and CHAN 1 should be chosen so that the propagation delay is not greater than 2 nsec. If a Tektronix SG 503 is used, terminate at the Channel 1 input with a 50 Ω feed-through terminator.

3. Set the controls of the 9400 as follows:

   a) Turn off all traces except Channel 1.

   b) Time/div: 0.2 µsec/div.

   c) Interleaved sampling: OFF.

   d) Channel 1 input: Signal coupling: 1 MΩ, DC
      Gain: 0.5 V/div
      Var. Gain: 1
      Offset: 0

   e) Trigger: Source: CHAN 1
      Mode: NORM
      Delay: 50 % Pre-trigger (center of screen)
      Level: 0.00 V.

4. Adjust the output amplitude of the sine wave generator to get about an 8 division peak-to-peak sine wave, i.e. corresponding to a 2 V amplitude. It is important that the offset of the input be set to zero (use the Panel STATUS menu to verify this). Use the offset adjustment of the sine wave generator to center the signal with respect to the screen. Later, the test on the external trigger level requires that the signal have an absolute range of ± 2 V.

5. Check the sine wave. It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position zero (vertical center) within ± 0.6 division.

6. Adjust the 9400 settings as listed first in (a) and then in (b) below. For each, check the resulting sine wave:

   It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position + 3 div (i.e. the second line from the top) within ± 0.6 division.

   a) Trigger Coupling: AC
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: + 3.00 div

   b) Trigger Coupling: LF REJ
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: + 3.00 div

7. Adjust the 9400 settings as listed first in (a) and then in (b) below. For each check the resulting sine wave.

   It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position - 3 div (i.e. the second line from the bottom) within ± 0.6 div.

   a) Trigger Coupling: AC
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: - 3.00 div

   b) Trigger Coupling: LF REJ
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: - 3.00 div

8. Disconnect the input from Channel 1 and connect it to input of Channel 2.

9. Turn off all traces, except Channel 2.

10. Set Channel 2 input: Signal Coupling: 1 MΩ, DC
    Gain: 0.5 V/div
    Var. Gain: 1
    Offset: 0

11. Set Trigger Source to CHAN 2.

12. Repeat steps 4 though 7 for channel 2.

13. Leave the input connected to Channel 2 and leave the trace of Channel 2 on.

14. Set Trigger Source to EXT.

15. With the trigger level set to + 1.5 V and - 1.5 V, repeat steps 4 through 7 for the EXTERNAL trigger. Observe the effect on channel 2. Tolerance for the checkpoints: ± 0.8 div.

2.1.16 Bandwidth Test of the Trigger

This test checks the bandwidth of the trigger circuits.

1. Set up a Tektronix SG 503 LEVELED SINE WAVE GENERATOR as follows:

   a) Frequency: 200 MHz
   b) Amplitude Multiplier: X 1
   c) Output Amplitude: 5.5 (i.e. max.).

2. Connect the output of the SG 503 to the EXTERNAL input of the 9400 and also to the Channel 1 input using a coaxial T-connector. The cable length between EXTERNAL and CHAN 1 should be chosen so that the propagation delay is not greater than 2 nsec.

3. Set the controls of the 9400 as follows:

   a) Turn off all traces, except Channel 1.

   b) Time base: 5 nsec/div.

   c) Interleaved sampling: ON

   d) Channel 1: Coupling: 50 Ω, DC
      Gain: 0.5 V/div
      Var. Gain: 1
      Offset: 0

   e) Trigger: Source: EXT
      Mode: NORM
      Delay: 50% Pre-trigger (center of screen)
      Level: 0.00 V
      Coupling: DC, LF Rej and AC sequentially

4. The 9400 must keep triggering in a stable way (i.e. a strongly attenuated 200 MHz sine wave must be visible on the display) for all 3 couplings while the trigger level is at ± 0.20 V.

2.1.17 Manual time-base calibration with WWV standard signal (1 MHz)

Any 1 MHz sine wave generator with an accuracy better than 1 ppm can be used (for example a Marconi 2019A).

1. Press the following sequence of menu buttons:

   Main Menu
   Recall PANEL
   Default
   Menu Off.

2. Set the controls of the 9400 as follows:

   a) Channel 1: Signal coupling: 50 Ω DC
      Gain: 1 V

   b) Time base: 2 µsec/div

3. Select the main menu and press the button corresponding to the Panel Status Menu.

4. Adjust the **Vertical Offset** knob for channel 1 until 0.00 V is displayed.

5. Adjust the trigger settings as follows:

   Delay: 0% Pre- (Touch ZERO)
   Level: 00 Div
   Coupling: DC
   Source: CHAN 1
   Slope: +
   Mode: Normal

6. Ensure that the Panel Status Menu is as shown in Figure 6.

Modify
Segments

Set Ch 1
Attenuator

Set Ch 2
Attenuator

Return

PLOTTING

ACQUISITION PARAMETERS

VERTICAL	Chan 1	Chan 2
Fixed V/div	1 V	50 mV
Total V/div	1.56 V	50.0 mV
Offset	.00 V	2.0 mV
Coupling	DC 50 Ω	AC 1 MΩ

TRIGGER	
Delay	.0% Pre
Level	.00 div
Coupling	DC
Source	CHAN 1
Slope	+
Mode	NORMAL

Time/div	2 µs
Time/pnt	10 ns
Points/div	200
Interleaved Sampling	OFF
BW-Limit	OFF
# Segments for SEQNCE	15

Trigger Level has absolute meaning with DC-Coupling only

PANEL STATUS DISPLAY

Figure 6

7. Press the following sequence of buttons

   Return, Menu Off

8. Input the WWV signal to Channel 1.

9. Adjust the VERTICAL gain (Volt/div and VAR settings) to get a 6 division peak-to-peak signal.

10. Select the TRIGGER mode: SINGLE (HOLD).

11. Press DUAL GRID. A dual grid is displayed on the screen.

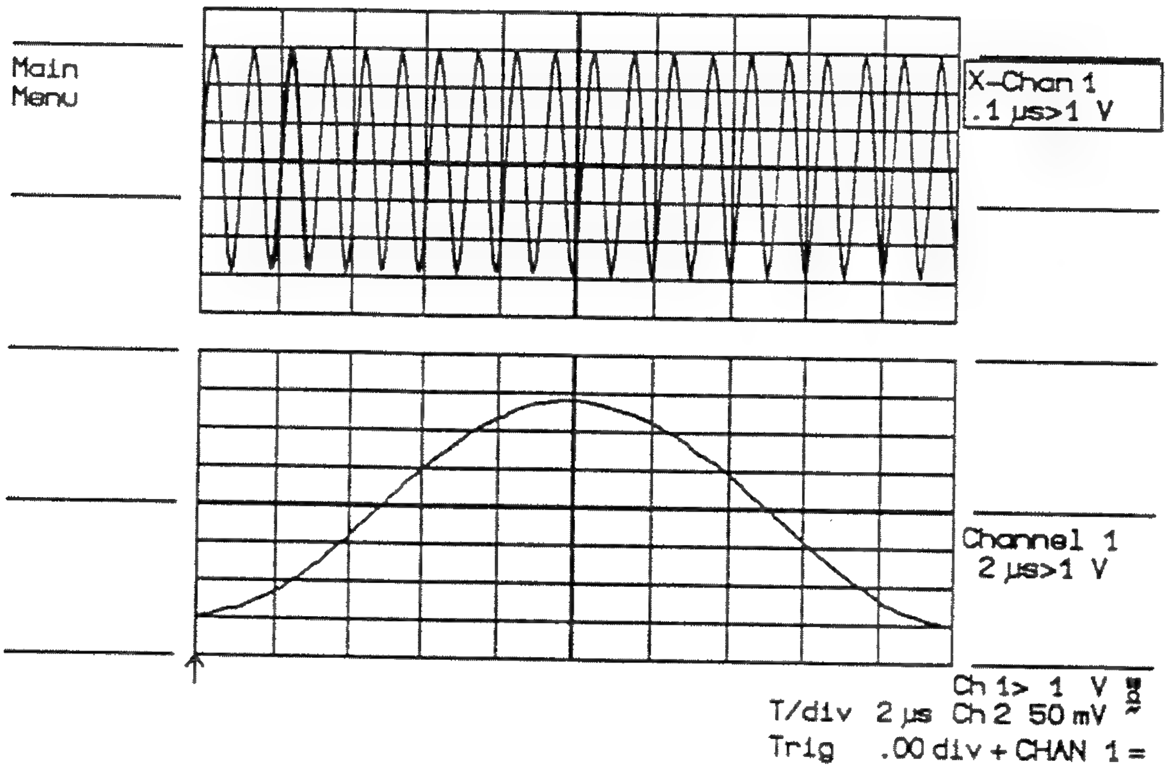
12. Press the following sequence of buttons:

    Press EXPAND A
    Press Display Control RESET
    REDEFINE Channel 1 (channel 1 is now the source trace).

13. Adjust the TIME MAGNIFIER to 0.1 μsec/div;

14. Turn the DISPLAY CONTROL Horizontal POSITION knob to select the 3rd period on the trace.

15. Using the Vertical POSITION knob put the expanded track on the second grid as shown in Figure 7.



WWV SIGNAL; FIRST EXPANSION

Figure 7

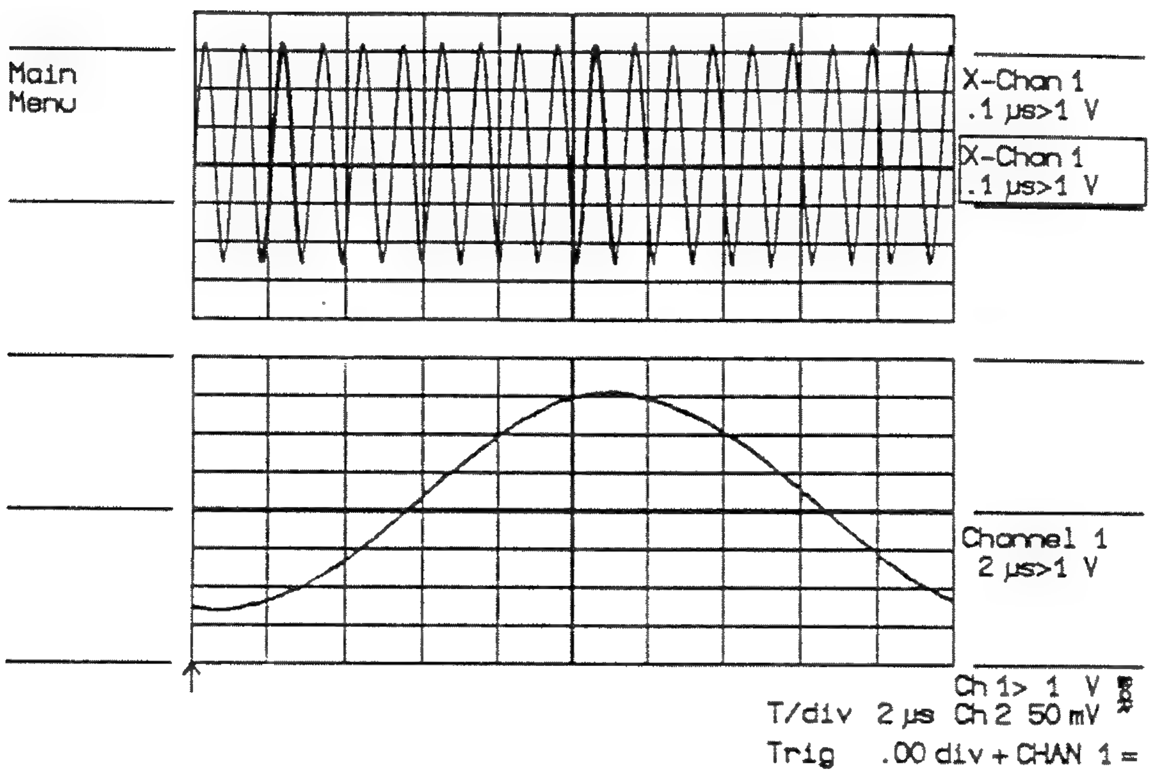
16. Press the following sequence of buttons:

    EXPAND B.
    DISPLAY CONTROL SELECT.
    REDEFINE Channel 1 (channel 1 is now the source trace).

17. Adjust the TIME MAGNIFIER to 0.1 μsec/div;

18. Turn the DISPLAY CONTROL Horizontal POSITION knob to select the 13th period.

19. Using the vertical and horizontal POSITION knobs, overlay the two expanded traces on the lower grid as shown in Figure 8.



WWV SIGNAL; SECOND EXPANSION

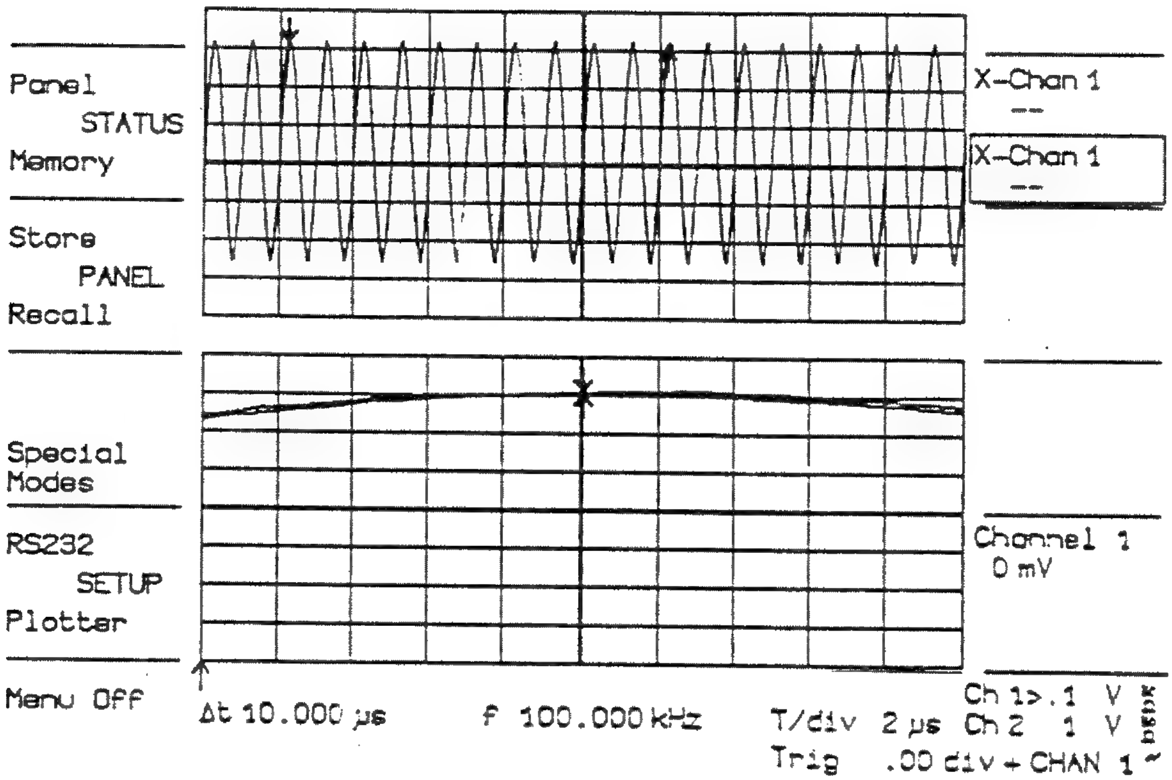
Figure 8

Measurement of the time difference (frequency)

20. Press the TIME cursor button.

21. Place the REFERENCE cursor on the 3rd period (control the cursor position on the upper grid).

22. Put the DIFFERENCE cursor (CURSOR POSITIONS) on the 13th period (control the cursor position on the upper grid) and adjust alignment of the two cursors with DIFFERENCE cursor (control the cursor position on the lower grid) as shown in Figure 9.



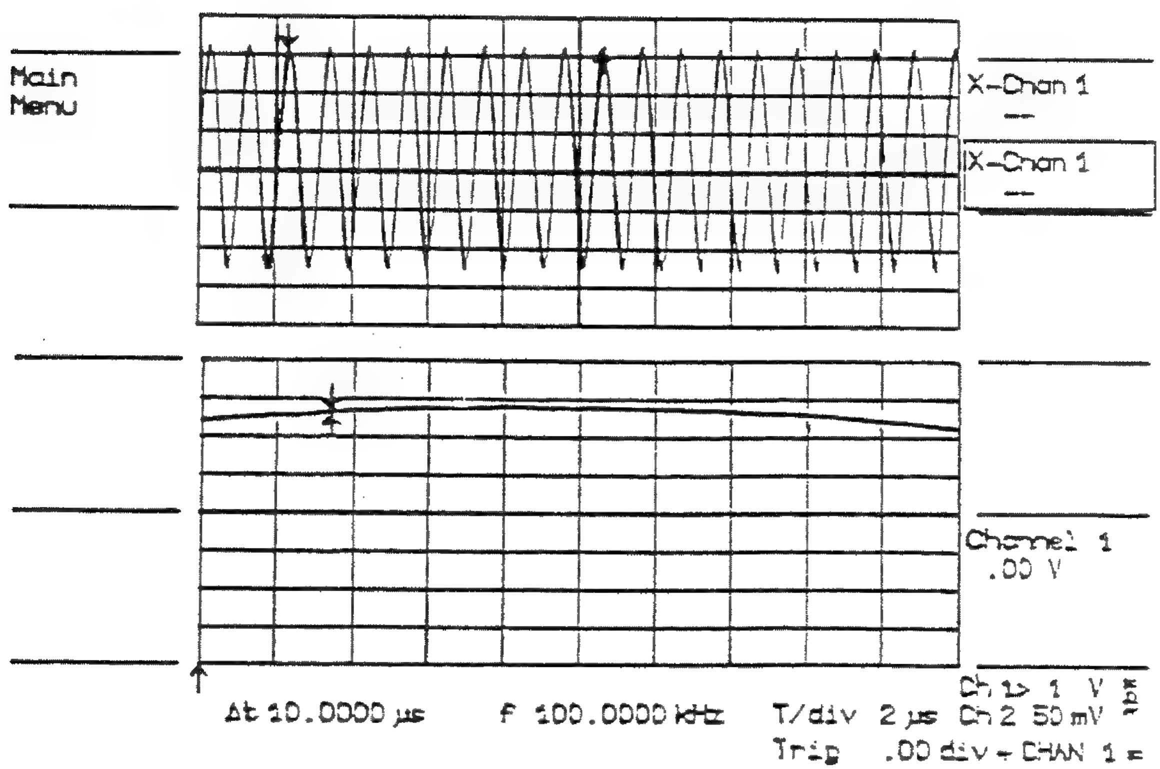
WWV SIGNAL: POSITION OF THE CURSORS

Figure 9

23. Press the following sequence of buttons:

    Main Menu
    Special Modes
    Mod. Common Expand (selects COMMON EXPANDED ON)
    Return
    Menu Off

24. Turn the TIME MAGNIFIER (DISPLAY CONTROL) to select the maximum expansion. Adjust the two cursors with the DIFFERENCE Cursor knob as shown in Figure 10.



WWV SIGNAL; MAXIMUM EXPANSION

Figure 10

25. The DIFFERENCE time reading must be in the interval 9.9996 µsec to 10.0004 µsec.

    Reading accuracy ± 400 psec (± 1 dot) on time reading.

2.2 Symptoms and Diagnosis

In this section some attempt is made to suggest possible problems which be the cause of observed symptoms in a defective 9400.

2.2.1 No Image on Screen

IF the **fan is still** AND **rear panel LEDs are off**

THEN check main power fuse on back panel, power plug, etc.,

ELSE IF the **fan runs** AND **rear panel LEDs are off**

THEN check low voltage supplies and their connections
check for ripple > 500 mV on any one of the low voltage DC power supplies

ELSE IF **rear LEDs are on** AND **front-panel LEDs are off**

THEN check power supplies to, and operation of, 9400-1 main board

ELSE IF **front-panel LEDs are on**

THEN check heater glow at rear of CRT
check 9400-7 correctly fitted at CRT base
check all cables 9400-2 and 9400-7 (4)

check fuses 9400-2
check that the thermo-switch is open on 9400-2 <1.2.5.1>
check RESET line high <1.2.5.1>
check signals on 9400-2 bus <1.2.2.1>
check amplifier inputs on 9400-2 <1.2.7.1>
check EHT generator on 9400-2 <1.1.9.1>
check sync signal from back panel
at J17 pin 13 9400-1 <1.1.8.1>

The fault is probably on the 9400-2 (1.2) or 9400-1 (1.1.16), but may be caused by no response from a peripheral of the 68000 - note that all boards are peripherals - which can be checked by looking at the re-boot circuit <1.1.2.1>.

2.2.2 Abnormal Image on Screen

IF the **display is slightly out of focus**, but otherwise normal

THEN	adjust focus control on 9400-7	(2.4.7)
OR	check function of 9400-7	(1.7)
	check HT supplies from 9400-2	(1.2.11)

ELSE IF **display** dim but otherwise normal

THEN	adjust brightness on 9400-7	(2.4.7)
OR	check function of 9400-7	(1.7)
	check HT supplies from 9400-2	(1.2.11)
	check luminance signal from 9400-2	(1.2.4)
	check potentiometers	(1.5.2)
	check potentiometer controls	(1.1.21.3)

ELSE IF the **display is badly out of focus** or just a patch of light

THEN	check function of 9400-7	(1.7)
	check HT supplies from 9400-2	(1.2.11)

ELSE IF entire image has the **wrong width**

THEN	adjust X amplifier gain	(2.4.2.3)
OR	check signal into X amp	(1.2.7+8)

ELSE IF entire image has the **wrong height**

THEN	adjust Y amplifier gain	(2.4.2.3)
OR	check signal into Y amp	(1.2.7+8)

ELSE IF the entire image is **distorted in X**

THEN	check X deflection processing	(1.2.6-8)

ELSE IF the entire image is **distorted in Y**

THEN	check Y deflection processing	(1.2.6-8)

ELSE IF the entire image is **shifted sideways**

THEN	adjust X offset	(2.4.2.2)
OR	check X circuits	(1.2.6-8)
OR	adjust centralizers	(2.4.7.4)

ELSE IF the entire image is **shifted vertically**

THEN	adjust Y offset	(2.4.2.2)
OR	check Y circuits	(1.2.6-8)
OR	adjust centralizers	(2.4.7.4)

ELSE IF the **lines do not join up** correctly

THEN adjust vector controls (2.4.2.5)
OR check circuits (1.2.4)
ELSE IF the grids/menus are good but the **waveforms bad**

THEN IF double arrows show **waveform 1 (2)**
is right off screen
THEN check the input offset at socket with
Hi-Z voltmeter (2.4.1.4)
AND check the input protection diodes (1.1.31.1)

ELSE IF **no waveforms** on Channel 1 (2)

THEN check the entire signal path from Channel 1 (2) input

ELSE IF **waveforms** on Channel 1 (2) **distorted**

THEN check 9400-3 Channel 1 (2) (1.3)

ELSE IF **bad waveforms** on both channels

THEN check 9400-8 is present <5.0.2>
check it has good signals CK, CKR,
SYNC (1.4)
check 9400-4 (1.4)
check 9400-1 (1.1)

ELSE IF **no waveforms** on either channel

THEN check 9400-8 is correctly inserted (5.0.3)
check 9400-8 carries correct signals (1.8)
check 9400-4 functions (1.4)

2.2.3 Abnormal Control Responses

2.2.3.1 Potentiometer Problem

IF **only one is faulty**

THEN IF accessible from rear

THEN probe with scope/meter for levels at ends and slider

ELSE remove front panel and test

IF potentiometer seems good, probe multiplexer output C pin 8 on 9400-5 (1.5.2) for level change with rotation

IF **no signal** change DG508 or test its control signals (1.5.2)

ELSE (several or all do not work)

probe multiplexer output, C pin 8 on 9400-5 (1.5.2) or front-panel connector pin 9 on 9400-1 (ANO) (1.1.21.3) <5.1.1> to see response to rotation

check DG508 control signals

IF **DG508 signal absent or wrong** remove bottom cover (5.0.1) and check signals on 9400-5 cable <5.1.1> (1.1.21.3) FA1-3, etc.

IF necessary investigate front-panel control circuit (1.1.21)

2.2.3.2 Switch Control

IF **only one is switch bad**

THEN check switch with meter
OR investigate signals (1.5.3) (1.1.21.4)

ELSE **(several or all do not work)**

IF all the switches execute the wrong function

THEN check that the cable is correctly inserted between 9400-1 and 9400-5 at both ends

ELSE check power on 9400-5 investigate signals (1.5.3) or remove bottom cover (5.0.1) and probe 9400-5 connector <5.1.1> (1.1.21) probe front-panel controller (1.1.21)

2.3 Fault Finding on Individual Boards

This section includes suggestions for locating faults on individual boards of the 9400, in a somewhat anecdotal manner, as a comprehensive list could not be made.

2.3.2 Display Board

2.3.2.1 No Image on Screen

IF there is **no image** on the screen

THEN check the thermo-switch, which is the round component at the center of the MOSFET heat sink; it should be open circuit in a working DSO. <1.2.5.1>

IF it is closed

THEN there is over heating; check the amplifiers <1.2.8.1>

ELSE (it is open) check one pin is at -15 V and the other is between -1 V and +1 V.

IF (lower than -1 V OR higher than +1 V)

THEN check the RESET line (1.2.5), which should be TTL high. <1.2.5.1>

IF the RESET line is TTL low

THEN check the source (9400-1 J17/2)(1.1.3).

ELSE

IF -1 V > thermo-switch > -5 V

THEN check Q67 and 1N748 zener <1.2.5.1>

ELSE

IF -5 V > thermo-switch > -15 V

THEN check Q52 and Q41 <1.2.5.1>

ELSE

IF +15 V > thermo-switch > +1 V

THEN check Q51 and Q42 <1.2.5.1>

2.3.7 CRT Services Board

2.3.7.1 IF No Image is Present

THEN check voltages on 9400-7:

600 V	580 V
60 V	75 V
Z	-2 V
ZC	0 V

IF 60 V -> 20 V AND 600 V -> about 10 V

THEN connecting ZC to ground will overcome the protection system to aid investigation

WARNING

IF there is a point of light at the center of the screen you must power down OR remove the ZC override. If you want to continue, power down and disconnect the EHT cable, placing in a dummy load or safe insulating receptacle.

2.3.9 Power Supplies

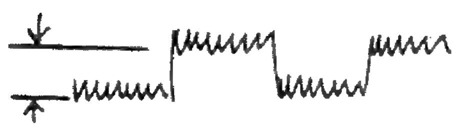
2.3.9.1 Power Supply Noise Problem

Some power supplies produce noise on the supply rail which can produce disturbance to the display of the 9400. The diagrams below show the maximum acceptable noise - any unit giving more than this should be replaced. The diagrams show what would be seen using a 9400 with a probe.

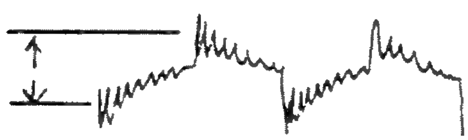
A Appearance. The noise looks like this:

|<- 10 or 20 msec->|

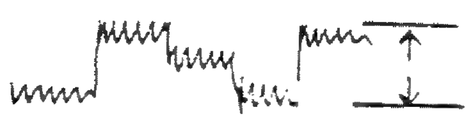
B Maximum low frequency ripple must be less than 30 mV p-p



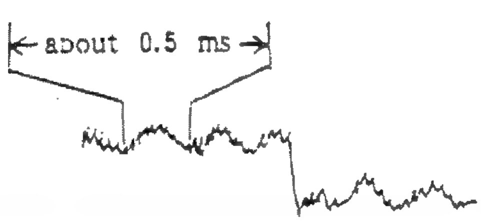
C Maximum high frequency ripple must be less than 30 mV p-p



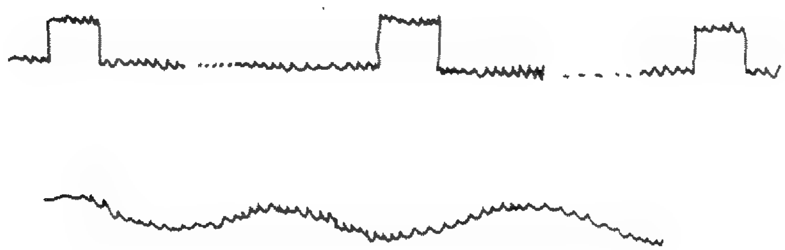
D Total ripple must be less than 50 mV p-p



E There must be no oscillations:



A similar problem is that some power supplies give sudden short changes in level. If this results in visible screen problems, reject the power supply. Any power supply which gives jumps of more than 50 mV should be rejected. The second, smooth variation is acceptable, because it causes no apparent trouble.



2.4 Adjustment Procedures for 9400

2.4.0 Introduction

This section describes all the adjustments which can be made in the field without the special LeCroy test gear which is only available at 9400 repair centers. Note that any adjustment which is omitted from this manual must not be touched, as maladjustment of certain presets can seriously degrade performance though this may not at first be apparent. Handling of boards should be done in such a way as to minimize the risk of moving a preset.

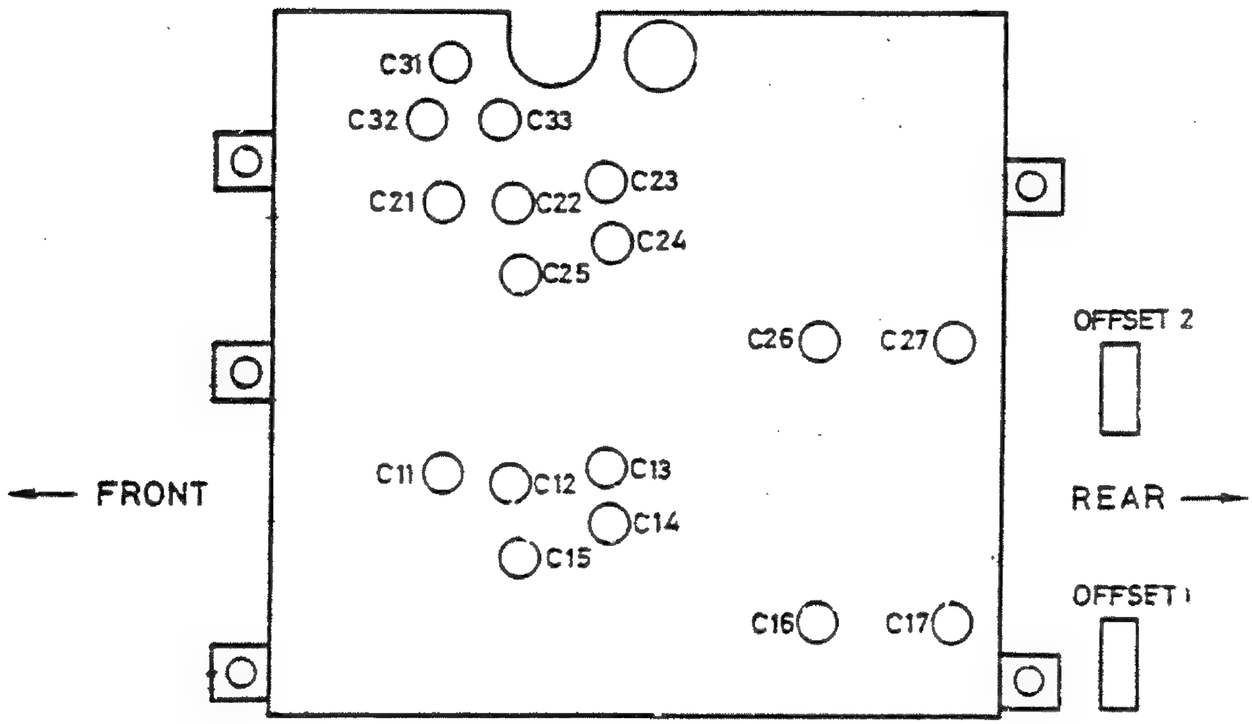
Some procedures require that the internal test software of the 9400 be set up; this is described in detail in paragraph 3.1.

The present adjustment procedures are contained in the computer assisted adjustment section of the 9400 calibration software package CALSOFT (CS01, CS02). It guides the service engineer through all the procedures and sets the 9400 up automatically as required for each individual adjustment. The present procedures are in compliance with the calibration limits applied in CALSOFT.

2.4.1 9400-1 Main Board

2.4.1.1 Introduction

The 9400-1 main board carries the front-end amplifiers, attenuators and trigger controls. There are numerous presets which can be adjusted in the field, for example after replacement of a HVV 200.



Presets on the 9400-1 front-ends

Figure 2.4.1.1

2.4.1.2 Power Supply

Check the supply voltages ± 15.01, ± 0.02 V, and ± 5.17 ± 0.01 V nominal on the 9400-9A board.

The ELBA supplies can be adjusted through the DSO rear panel.

2.4.1.3 Probe Calibrator

DSO probe calibrator set to 1 V.

Adjust potentiometer P0(F1) to 1 V at the probe calibrator output (within 0.5%) using a 4-digit voltmeter, and hit N to check again.

Probe calibrator set to 2 V. Check with a 4-digit voltmeter.

If not OK (within 0.5%), double error (e.g. 2.005 --> 2.010) by adjusting potentiometer P1(F1), and go back to check 1 V again.

2.4.1.4 Gain Curves and Offset

Gain curves

Put the DSO into the internal test menu with TRIG SOURCE LINE, MODE NORM.

Start the DSO internal test 'gain curves', BWL ON, 5 mV/div CH 1 and 2.

Check that the gain curves are at least 1/4 division above the gain = 1 line (left edge) on the left flat-top and that the curves decrease to at least 1/4 division below the gain = .4 line (center).

Check that the gain curve is smooth without steps or kinks.

If not OK, HVV200 of corresponding channel is probably bad!

Replace the 9400-1 board.

Repeat the test for BWL OFF and 10, 20 and 50 mV/div gain.

Offset

Put the DSO into the internal test menu with TRIG SOURCE LINE, MODE NORM.
Start the DSO internal test 'Offset vs Gain', BWL ON, 5 mV/div CH 1 and 2.

Check that the curves are rather horizontal (difference beginning-end of slope < 1 div) and that deviations from the center line stay within 1.5 divisions. If not OK, adjust potentiometers P3(D7)/P2(B7) to make the curves as flat as possible with deviations for BWL ON/OFF symmetric around the center line.

Repeat the test for 10, 20 and 50 mV/div gain.

2.4.1.5 Check Input Impedance

Channel 1 and 2

Check the input impedance for CH 1 and 2. The 1 MΩ DC and 50 Ω inputs for all gains should be 1 MΩ, and 51 Ω within 1%.

Trigger

Set the DSO to EXT TRIG SOURCE, COUPLING DC.
Check TRIG input impedance 1 MΩ (± 5%).

Set the DSO to TRIG SOURCE EXT/10, COUPLING DC.
Check TRIG input impedance 1 MΩ (± 5%).

2.4.1.6 Overload Protection

Set the DSO to CH 1 and 2 50 Ω.
Check that overload protection is activated within 15 to 25 seconds after applying > 7 V.

If not OK, adjust potentiometer slightly P4,P5 (G8).

Wait for at least 10 minutes between tests in order to allow settling to ambient temperature!

2.4.1.7 Trigger

Check Couplings

Set the DSO to TRIG SOURCE EXT, COUPLING DC.
Apply a 10 kHz square wave signal 4 V p-p to EXT.
Use the adjusted probe and look at pin 6 or 7 of MVL407 (B13).
You should see the same square wave.

Set the DSO to TRIG SOURCE EXT, COUPLING HFRej.
Apply a 10 kHz square wave signal 4 V p-p to EXT.
Use the adjusted probe and look at pin 6 or 7 of MVL407 (B13).
You should see slower fall/risetimes (integration).

Set the DSO to TRIG SOURCE EXT, COUPLING LFRej.
Apply a 10 kHz square wave signal 4 V p-p to EXT.
Use the adjusted probe and look at pin 6 or 7 of MVL407 (B13).
You should see spikes at the signal edges (differentiation).

Set the DSO to TRIG SOURCE EXT, COUPLING AC.
Apply a 15 Hz square wave signal 4 V p-p to EXT.
Use the adjusted probe and look at pin 6 or 7 of MVL407 (B13).
You should see spikes at the signal edges (differentiation).

Level DC

Check the ± 12 V regulators on 9400-1 (F10/11); they have to be matched within 50 mV for correct trigger level calibration.

Set the DSO to CH 1, 1 MΩ DC, 500 mV/div, TRIG: COUPLING DC, SLOPE POS, LEVEL 0 div.
Apply a 100 Hz sine waveform 4 V p-p to CH 1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.
If not OK, slightly adjust potentiometer P6(C/D12) and enforce AUTO-CALIBRATION and check again.

Set the DSO to CH 1, 1 MΩ DC, 500 mV/div, TRIG: COUPLING DC, SLOPE NEG, LEVEL 0 div.
Apply a 100 Hz sine signal 4 V p-p to CH 1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH 1, 1 MΩ DC, 500 mV/div, TRIG: COUPLING HFRej, SLOPE NEG, LEVEL 0 div.
Apply a 100 Hz sine signal 4 V p-p to CH 1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO set to CH 1, 1 MΩ DC 500 mV/div, TRIG: COUPLING HFRej, SLOPE POS, LEVEL 0 div.
Apply a 100 Hz sine signal 4 V p-p to CH 1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/DIV, TRIG: SOURCE CH2, SLOPE POS, LEVEL 0, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL +3 div, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2.
Check that crossing at trigger point is at +3 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL -3 div, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2.
Check that crossing at trigger point is at -3 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL 0, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 1 V/div, TRIG: SOURCE EXT/10, SLOPE POS, LEVEL 0, COUPLING DC.
Apply a 100 Hz sine signal 8 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at 0 divisions within 3 minor divisions.
If not OK, adjust by adding resistor 1/8 W 6.8K to 30K between base of Q5 to -5 or +5 V (depending on sign of deviation) on solder side; check again.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL 0, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL +1.5 V, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at +1.5 volt within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL -1.5 V, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at -1.5 volt within 1 minor division.

Bandwidth AC

Set the DSO to EXT DC.
Apply a 10 kHz square wave, about 20 V amplitude through 50 Ω 20 dB attenuator, 50 Ω feed through, to EXT.
Use the adjusted probe and connect to the base of Q5 below the input cover plate (the channel you are looking at should be adjusted first!)
Adjust C32 for no under-/overshoot.

Set the DSO to EXT/10 DC.
Apply a 10 kHz square wave, 0 dB, 50 Ω feed through, to EXT.
Use the adjusted probe and connect to the base of Q5 below the input cover plate.
Adjust C31/33 for no under-/overshoot,
C31: long time scale,
C33: short time scale.
If you had to adjust C31 or C33, go to previous adjustment C32.

Set the DSO to CH1 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH1, SLOPE POS, LEVEL 0, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH1 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH1, SLOPE NEG, LEVEL 0, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH1 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH1, SLOPE NEG, LEVEL 0, COUPLING LFRej.
Apply a 1 MHz sine signal 4 V p-p to CH1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH1 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH1, SLOPE POS, LEVEL 0, COUPLING LFRej.
Apply a 1 MHz sine signal 4 V p-p to CH1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL 0, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL +3 div, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2.
Check that crossing at trigger point is at 3 divisions within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL -3 div, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2.
Check that crossing at trigger point is at -3 divisions within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL +1.5 V, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2 through EXT.
Check that crossing at trigger point is at +1.5 V within 1 minor division.
If not OK, adjust level with C32 (if CH2 is not adjusted, go to CH2 50 Ω DC for the following checks, but make sure that the generator offset is 0!

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL -1.5 V, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2 through EXT.
Check that crossing at trigger point is at -1.5 V within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 1 V/div, TRIG: SOURCE EXT/10, SLOPE POS, LEVEL 0, COUPLING AC.
Apply a 1 MHz sine signal 8 V p-p to CH2 through EXT.
Check that crossing at trigger point is at 0 divisions within 3 minor divisions.

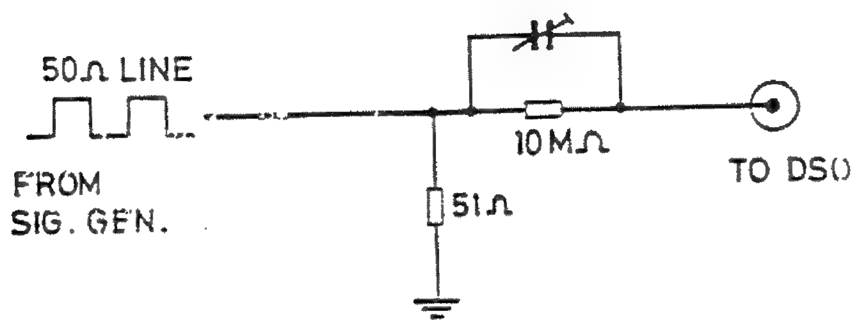
Set the DSO to CH2 AC 1 MΩ, 1 V/div, TRIG: SOURCE EXT/10, SLOPE POS, LEVEL +3 V, COUPLING AC.
Apply a 1 MHz sine signal 8 V p-p to CH2 through EXT.
Check that crossing at trigger point is at +3 V within 3 minor divisions.
If not OK, adjust level with C31/33 (if CH2 is not adjusted, go to CH2 50 Ω DC, but make sure that generator offset is 0!)
If you had to adjust, go back to previous C32 adjustment.

Set the DSO to CH2 AC 1 MΩ, 1 V/div, TRIG: SOURCE EXT/10, SLOPE POS, LEVEL -3 V, COUPLING AC.
Apply a 1 MHz sine signal 8 V p-p to CH2 through EXT.
Check that crossing at trigger point is at -3 V within 3 minor divisions.

2.4.1.8 Front-end

Channel 1

In the following adjustments the 4958 switch box is often used. It conveniently combines an adjusted /10 probe with attenuators. In the absence of a 4958, regular attenuators and a probe (like our Coline M12) which has been correctly compensated on an adjusted 9400 can be used. In the absence of a probe, an alternative test probe set up as shown in Figure 2.4.1.8 and properly adjusted on a good DSO, can be used.



Alternative Test Probe

Figure 2.4.1.8

Set the DSO to CH1, 1 V/div, 50 Ω, TRIG: SOURCE EXT, COUPLING DC, LEVEL 0.
Feed a 1 kHz square wave via switch box 4958 through EXT to CH 1.
Set BSD211/214 switch appropriately:
HVV200 no. XX XX 00 or 01 or 02 or 03: newer HVV with BSD214 transistor,
HVV200 no. XX XX /=00: older HVV with BSD211.
Set switch box 4958 to: 20 dB OFF, 20 dB OFF, 50 Ω OFF, Comp OFF.
Adjust signal amplitude to 6 divisions on screen.

Verify for the following settings that you always see the signal at 6 divisions:

CH 1			20 dB	20 dB	50 Ω	Comp	Reading
50 Ω,	1	V	OFF	OFF	OFF	OFF	6 div
50 Ω,	0.1	V	ON	OFF	OFF	OFF	6 div
50 Ω,	10	mV	ON	ON	OFF	OFF	6 div
1 MΩ,	10	mV	ON	ON	ON	OFF	6 div
1 MΩ,	0.1	V	ON	OFF	ON	OFF	6 div
1 MΩ,	1	V	OFF	OFF	ON	OFF	6 div
1 MΩ,	20	mV	ON	OFF	x	ON	6 div
1 MΩ,	200	mV	OFF	OFF	x	ON	6 div

Set the DSO to CH1 1 MΩ DC, 10 mV/div, TRIG: SOURCE CH1, COUPLING DC, LEVEL 0.
Apply a 10 kHz 6 V p-p square wave through 40 dB, 50 Ω feed through.
You should see 60 mV amplitude.

Set the DSO to CH1 1 MΩ DC, 100 mV/div, TRIG: SOURCE CH1, COUPLING DC, LEVEL 0.
Reduce attenuation to 20 dB.
Adjust C12 for no under/over-shoot.

Set the DSO to CH1 1 MΩ DC, 1 V/div, TRIG: SOURCE CH1, COUPLING DC, LEVEL 0.
Reduce attenuation to 0 dB.
Adjust C14/C13 for no under/over-shoot:
C14 long time-scale,
C13 short time-scale.

If you had to REadjust C14/C13, go back to adjustment C12.

Set the DSO to CH1 1 MΩ DC, 20 mV/div, TRIG: SOURCE CH1, COUPLING DC.
Apply a 1 kHz 6 V p-p square wave through switch box 4958 20 dB, Comp ON.

Adjust C11 for optimum risetime.

Set the DSO to CH1 200 mV/div, 1 MΩ DC, TRIG: SOURCE CH1, COUPLING DC, LEVEL 0.
Reduce attenuation to 0 dB.
Adjust C15 for optimum risetime.

Set the DSO to CH1 50 Ω DC, TRIG: SOURCE CH1, COUPLING DC.
Apply a 200 MHz sine signal with amplitude about 6 div to CH 1.
Adjust C17 for maximum amplitude.
Adjust C16 for maximum amplitude.
(Watch out for HVV oscillations at about 800 MHz!)

If you had to REadjust C16, go back to adjustment C17

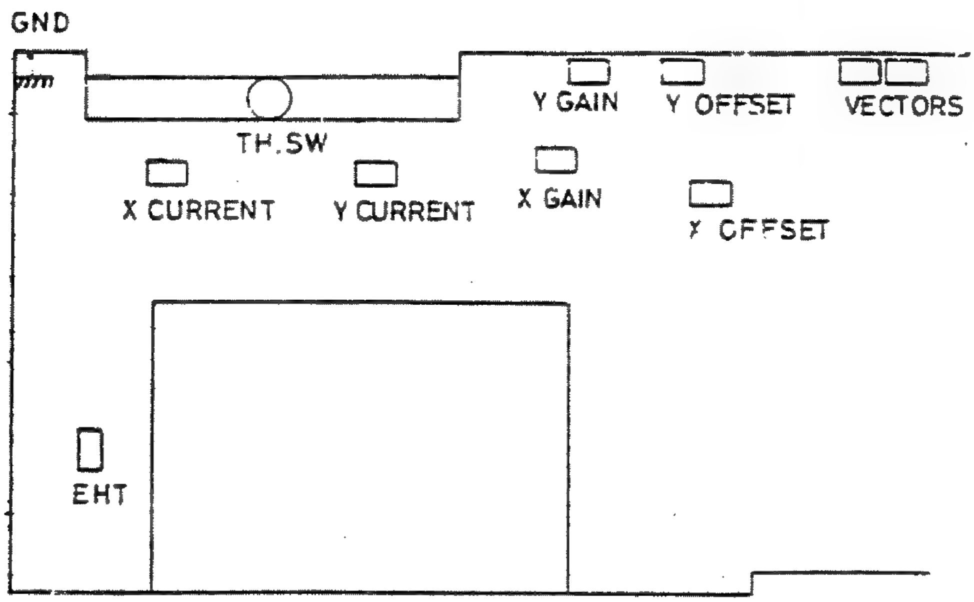
Channel 2

Repeat the above adjustment for channel 2. Add 10 to all capacitor labels, for example C11 becomes C21.

2.4.2 9400-2 and 9400-7 Display

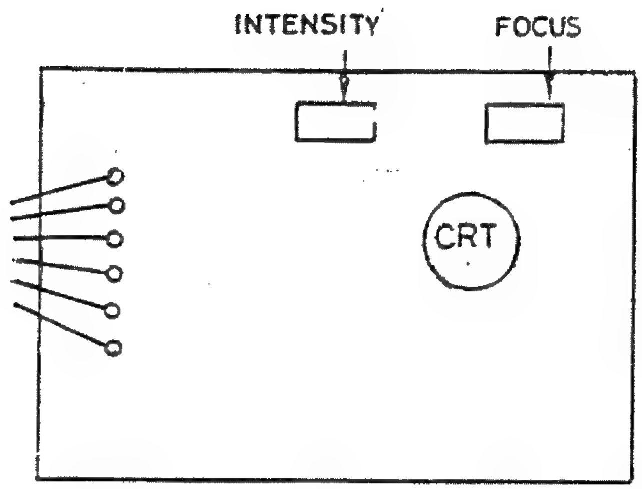
2.4.2.1 Introduction

The 9400-2 board carries a number of adjustments for the CRT image, many of which are field adjustable using procedures given below. The 9400-7 board carries much of the phosphor protection circuitry, and also the intensity and focus presets, which may be adjusted if there are no other contributory problems.



9400-2 Preset Controls

Figure 2.4.2.1



Intensity and Focus Controls

Figure 2.4.2.2

EHT

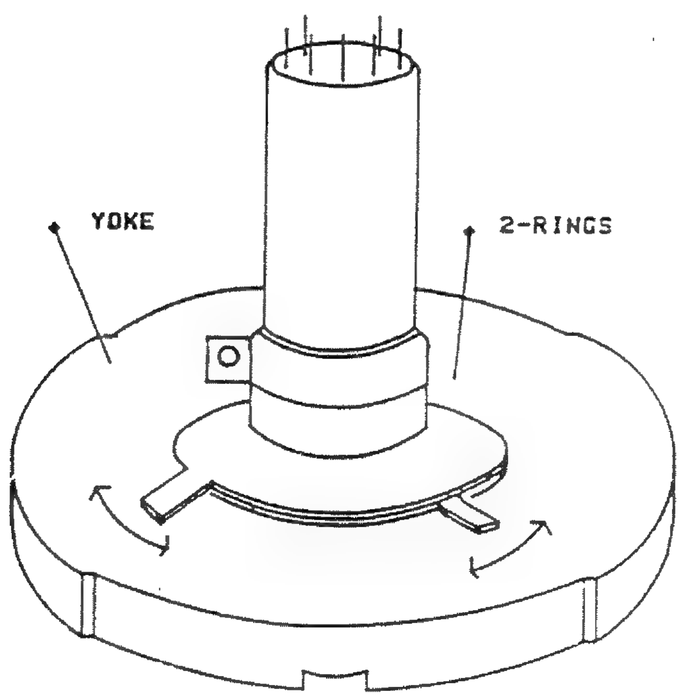
The 9400 should be set up to display a fairly complex image, and the two intensity controls on the front panel should be turned up; the EHT generator will then experience a substantial load. The EHT adjustment should be set to give an EHT potential of 11 kV. The 60 V and 600 V lines on the 9400-7 should also be checked.

Vector Joining

Adjust vectors with the help of the pair of vector potentiometers on the 9400-2 board right upper corner, above the connector.
Check that there are neither gaps nor overlaps in the letters T and S.

Centralizing Adjustment

If the X and Y amplifiers are correctly adjusted, and the image is poorly centered on the screen, it may be desirable to adjust the two magnetic rings on the yoke. This should not be done unless all other sources of image offset have been eliminated, and the amplifier offsets on the 9400-2 have been found to be correct.



Centralizing Rings

Figure 2.4.2.3

2.4.2.2 Adjustments

Image Position Adjustment

The offset controls may, in principle, be adjusted to obtain a centered image, provided that there are no other problems, see Centralizing Adjustment. Before making adjustments make sure that offsets at TP15 and TP21 are less than 10 mV for parts of the waveform after PGDIS and before SYDIS (1.1.16) (1.2.2), and other flat parts of the waveform between sections of vector drawing.

Intensity

Turn the DSO grid intensity off and the intensity to maximum.
Adjust the intensity potentiometer on the CRT board such that the center spot is just invisible.
If the intensity cannot be suitably controlled, then 9400-2 (1.2.4) (1.2.9) or 9400-7 (1.7) or 9400-1 (1.1.21.3) or the 9400-5 (1.5.2) must be checked.
This is the maximum allowed setting of the 9400-7 intensity control. It can be reduced if desired. Note that the yellow phosphor of the CRT in the 9400 is much more susceptible to damage by high beam currents than the usual blue/green phosphors.

Focus

Turn the grid intensity to maximum.
Adjust the focus control on the CRT board to optimize the image, taking into account all parts of the screen. If an expanded trace is selected, the selection box should be clearly separable from the menu separators.
If an adequate focus cannot be obtained, then the 9400-7 (1.7) or its power supplies on the 9400-2 (1.2.9) must be checked.

Image Size

Press the internal test button 'Calibration Constants' with border lines displayed.
Adjust the image size with the help of potentiometers GY/GX gain controls to the left of the two large yellow capacitors.

Yoke Rotation

Ensure that DSO power is OFF.
Rotate the image upright by turning the mechanical yoke position. For this loosen the screw on the yoke ring holder.

2.4.3 9400-3 ADC Board

2.4.3.1 Introduction

There are numerous preset controls on the 9400-3 ADC boards, which are set during manufacture. Only two of these are field-adjustable without the support of special LeCroy test gear. Every effort should be made to avoid disturbing these controls while handling the boards as they control the accuracy of waveform digitization. Note that the ADC boards may be interchanged for testing and fault finding, but they should always be replaced in their original position.

2.4.3.2 Gain Curves and Offsets

Gain curves

Put the DSO into the internal test menu with TRIG: source LINE, MODE NORM.
Start the DSO internal test 'Gain Curves', BWL ON, 5 mV/div CH 1 and 2.
Check that gain curves are at least 1/4 division above the gain = 1 line (left edge) on the left flat-top and that curves decrease to at least 1/4 division below the gain = 0.4 line (center).
Check that the gain curve is smooth without steps or kinks.
If not OK, the HVV200 of corresponding channel is probably bad!
Replace the 9400-1 board.

Repeat test for BWL OFF and 10, 20 and 50 mV/div gain.

Offset

Put the DSO into the internal test menu with TRIG: SOURCE LINE, MODE NORM.
Start the DSO internal test Offset vs Gain, BWL ON, 5 mV/div CH 1 and 2.
Check that the curves are rather horizontal (difference beginning-end of slope < 1 div) and deviations from the center line stay within 1.5 divisions.
If not OK, adjust potentiometers P3(D7)/P2(B7) to make the curves as flat as possible with deviations for BWL ON/OFF symmetric around the center line.

Repeat the test for 10, 20 and 50 mV/div gain.

2.4.3.3 Precision Adjustment for 1% Scopes

Adjust the DAC 800 (on the main 9400-1 board) offset to zero.
Measure voltage (mV) CAL1/CAL2 after LM324 (G6), in field G7 on one of the points where the two diodes are connected.
If larger than 1 mV, adjust potentiometer ZR (P8(J20) solder side) next to DAC 800, just behind -15 V power supply. It is difficult to access and a long slim screwdriver is needed.

Adjust the CH 1 and 2 HSH202 offset to zero.
Set the DSO to CH 1,2 50 Ω DC OFFSET 0, AUTO-CALIBRATE.
Measure voltage at CH 1,2 ADC SMB socket.
If larger than 3 mV, slightly adjust potentiometer P6 on the ADC board then enforce AUTO-CALIBRATION and check again (to do this, leave the ADC board in the DSO, put the GPIB board on the extender and reach in from the rear of the CRT!)

Put the DSO into the internal test menu with TRIG: SOURCE LINE, MODE NORM.
Start the DSO internal test Offset vs Gain, BWL ON, 5 mV/div CH 1 and 2.
Check that the curves are rather horizontal (difference beginning-end of slope < 1 div) and deviations from the center line stay within 1.5 divisions.
If not OK, adjust potentiometers P3(D7)/P2(B7) to make curves as flat as possible with deviations for BWL ON/OFF symmetric around the center line.

Repeat the test for 10, 20 and 50 mV/div gain.

2.4.3.4 Over-shoot

Channel 1

Set the DSO to CH 1, 50 Ω DC, 200 mV/div, TRIG: SOURCE: CH 1, COUPLING DC, Level 0.
Make sure that the CH 1 front-end is properly adjusted!
Apply a square wave with a risetime faster than 1 nsec (for example TEK PG502) through a 20 dB attenuator.
Adjust the step amplitude to 5 divisions.
Use the attenuator at input to attenuate possible reflections.
Adjust the capacitor between pins 8-10 of HSH202 such that signal overshoot is 1 minor division.
The signal should settle within 40 nsec.

Channel 2

Set the DSO to CH 2, 50 Ω DC, 200 mV/div, TRIG: SOURCE: CH 2, COUPLING: DC, LEVEL 0.
Make sure that the CH 2 front-end is properly adjusted!
Apply a square wave with a risetime faster than 1 nsec (for example TEK PG502) through 20 dB attenuator.
Adjust the step amplitude to 5 divisions.
Use the attenuator at input to attenuate possible reflections.
Adjust the capacitor between pins 8-10 of HSH202 such that signal overshoot is 1 minor division.
The signal should settle within 40 nsec.

2.4.4 9400-4 TDC Board

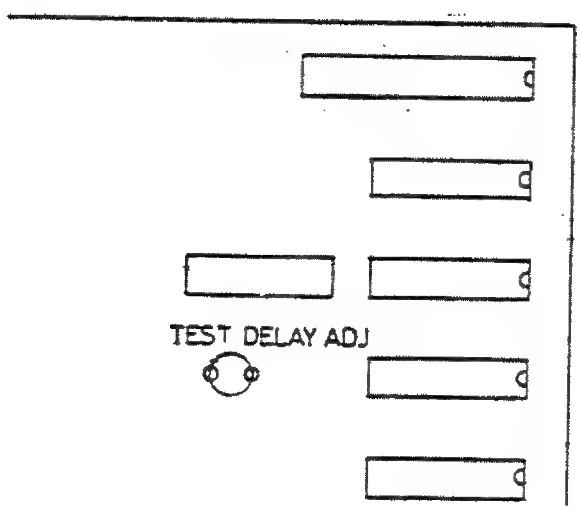
2.4.4.1 Frequency

Check the frequency (100 or 50 MHz) on the 2nd or 3rd line (from front) of the clock bus board.
If not OK, something basic is wrong with the TDC board.

Set the DSO to CH 1, 100 mV/div, 50 Ω DC, TRIG: SOURCE CH1, COUPLING AC, LEVEL 0, DELAY 19.99 msec post-trigger.
Apply to CH1 a sine wave of 100 kHz from a precision (better than 1 ppm) generator.
Adjust the 100 MHz ADJ such that the signal crosses the center point.
Turn the power off/on several times and check that the frequency is still OK. (This is to check that not too much adjustment was applied which may leave the oscillator locked out of the characteristic 100 MHz. If this happens, replace the crystal.)

2.4.4.2 Internal Trigger Delay

Set the DSO internal test 'TDC Calibration'.
Check (after a warm-up of at least 20 minutes) that there are two peaks of about the same width.
If not, adjust at TST DLY and check again.
It is very hard to reach this preset with a tool, but some help may be given using a probe adjustment screwdriver bent by 90 degrees. Also note that on ADC boards manufactured since February 1988 this varicap points upwards and is therefore easy to reach.



TDC Preset Control

Figure 2.4.4.1

2.4.5 Front-panel Board

2.4.5.1 LED Matching

All front-panel LEDs should be matched for color, in one of three grades (1.5.5). If urgent replacement of an LED is required, and the correct color match is not available, it is permissible to mismatch by one grade only in the case of a single LED, far from the others. For example, if one of a group fails, it can be replaced by one taken from a distant place on the panel, and the distant one can be replaced by the poorly matching one. Although the colors are fairly close, they look very bad when mixed.

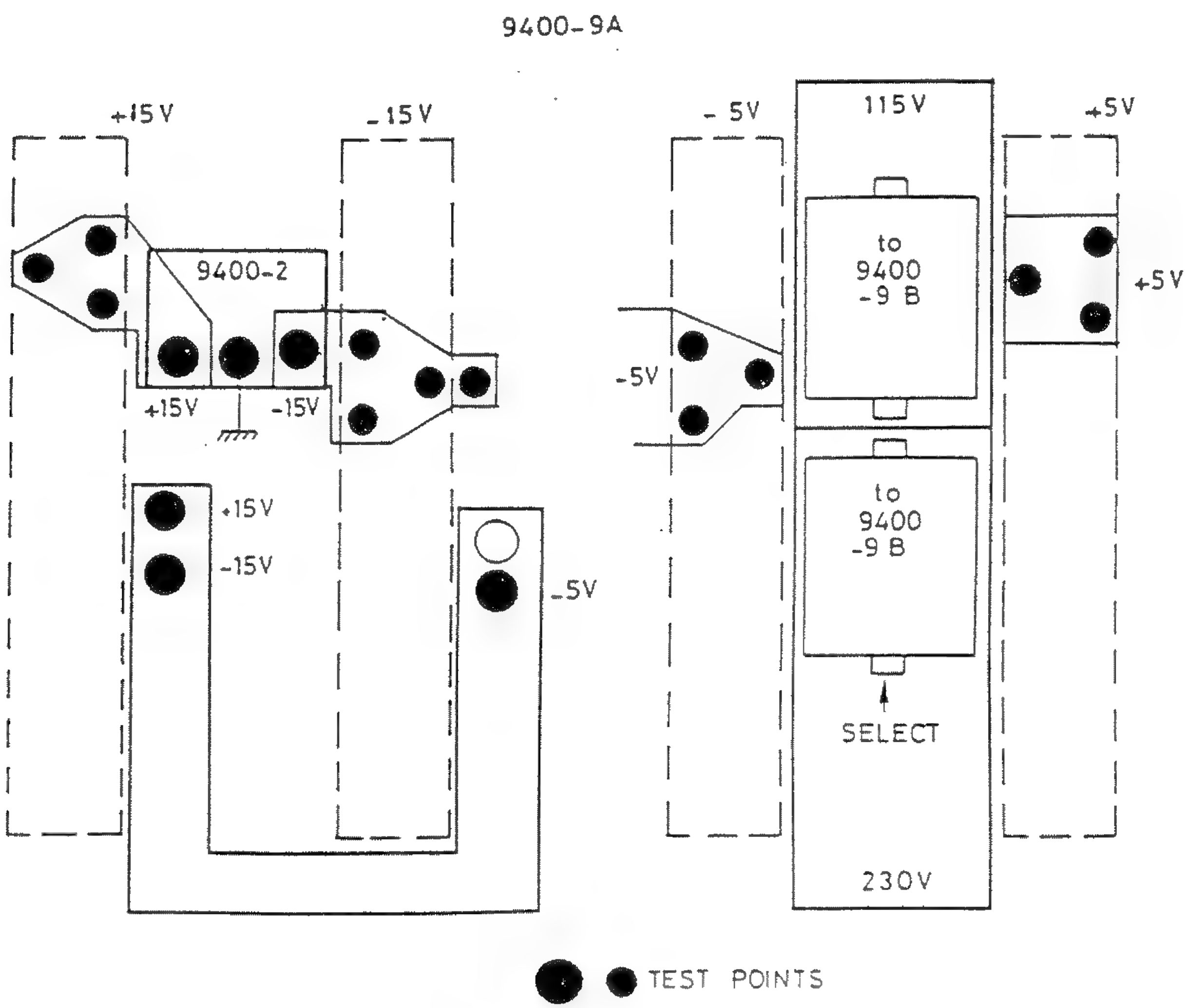
2.4.6 Changing the Input Line Voltage (Board 9400-9)

This will only be necessary when a 9400 has been transported, involving a change of local voltage.

Note that there are two operations, which must BOTH be done.

1. Ease out the little cover over the voltage adjuster <1.9.2> and take out the rotor. Rotate until the new voltage faces forward. Replace the rotor and the cover.

2. Remove the top cover (5.0.1) and move the large brown 12 pin plug on the 9400-9A <5.0.3> <2.4.9.1> to the 115 V or the 230 V position as appropriate. Check both settings carefully before powering up the DSO.



SETTING THE 115 V/220 V CONNECTION

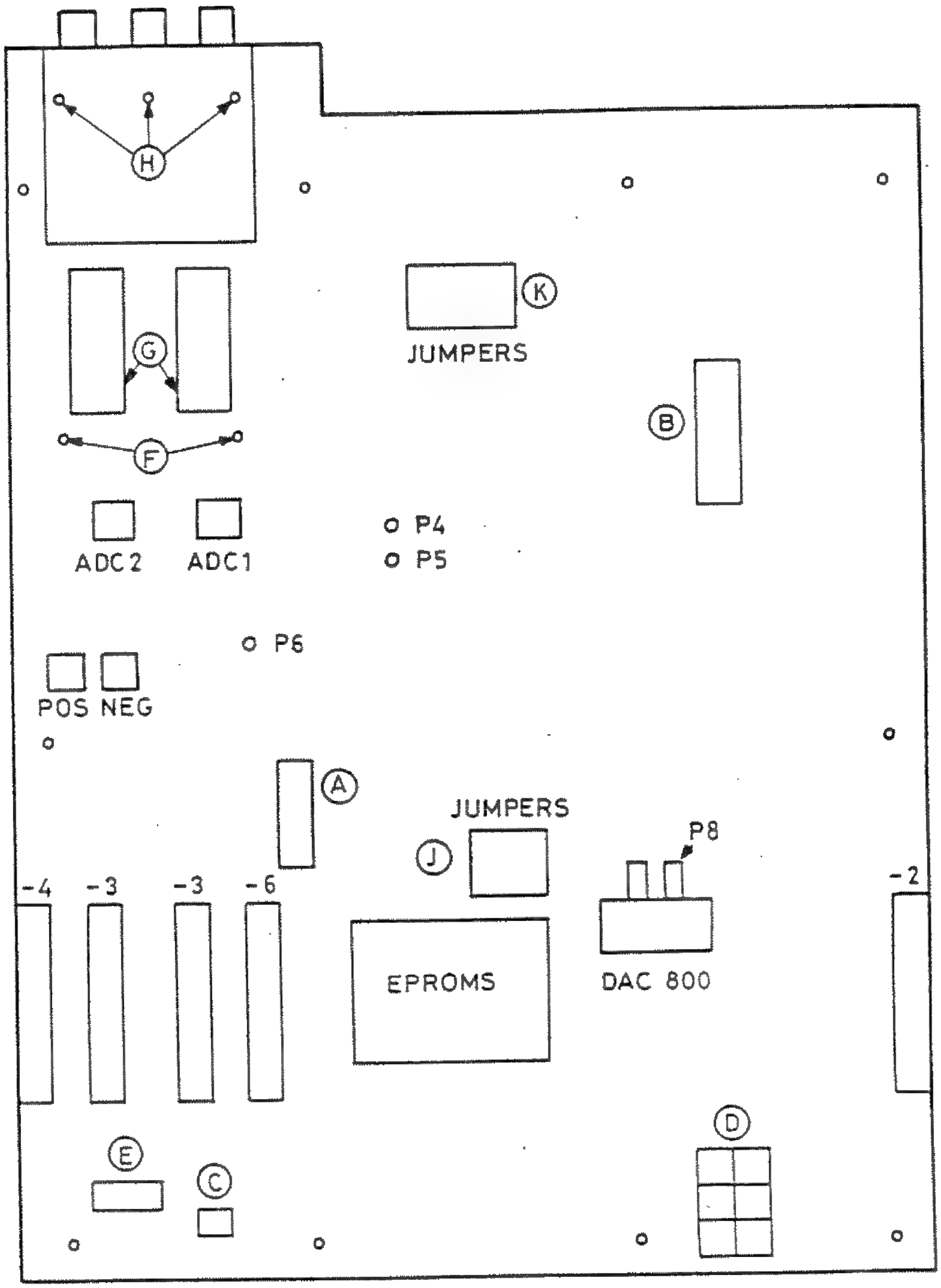
Figure 2.4.6

2.4.7 Potentiometers Cross Reference for the 9400-1 Board

Potentiometer	Used for	Name on Schematics	Location on board (Rev. F and up)
P0	Probe Calibrator	P0	F1 solder
P1	"	P1	F1 solder
P2	HVV200 Offset	no name	B7 solder
P3	"	no name	D7 solder
P4	Overload Protection	no name	G8 component
P5	"	no name	G8 component
P6	Trigger Level	P4	C/D12 comp
P8	Offset DAC 800	P6	J20 component

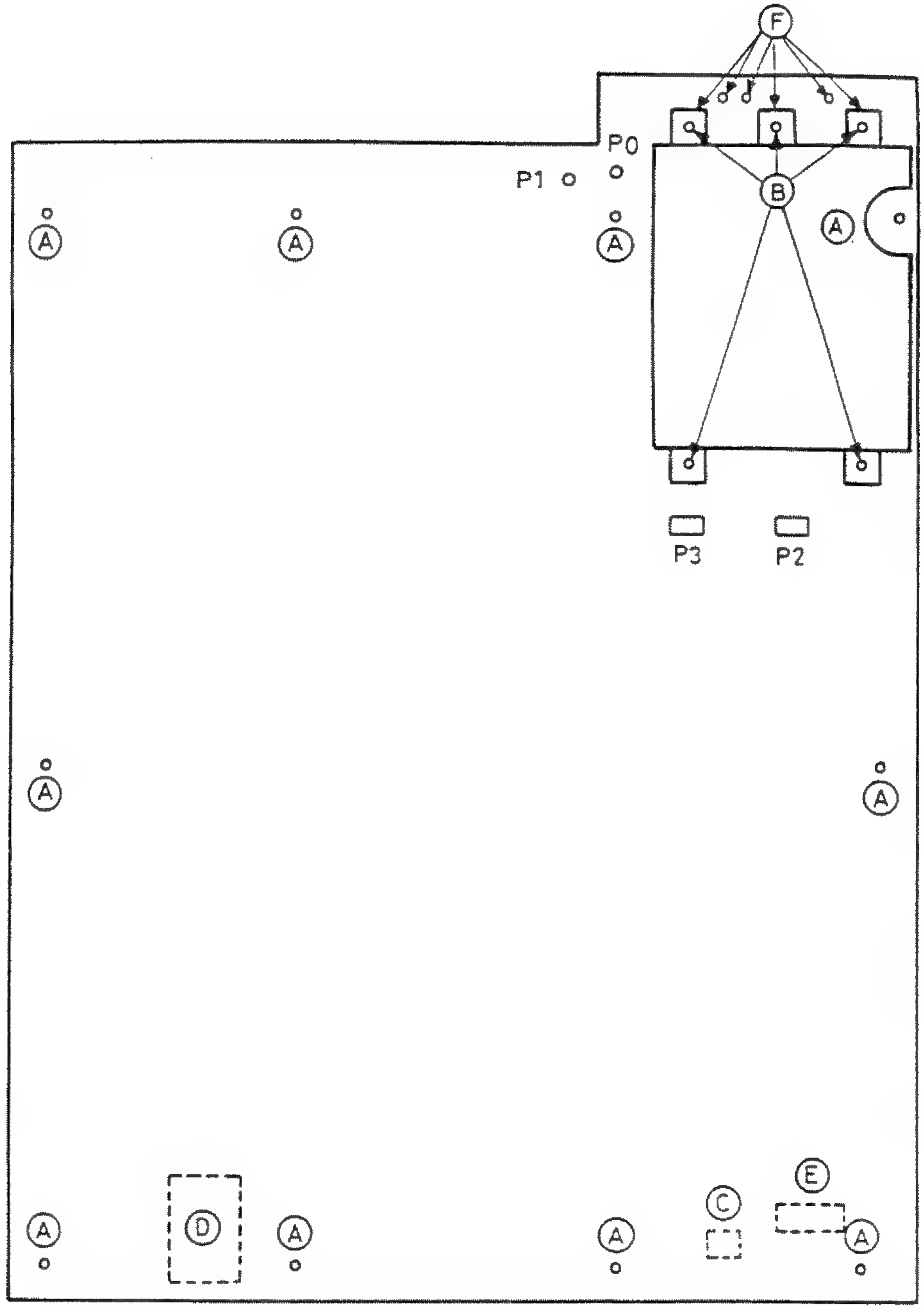
For Earlier Revisions

Revisions BC	remove resistor and place potentiometer P1 (2.2 MΩ)
All revisions	P0 on solder side
F and above	P2/P3 solder side
up to rev D	P0 component side between probe connectors



Top view of 9400-1 Main Board

Figure 2.4.7.1



Underside of the 9400-1 Main Board

Figure 2.4.7.2

CHAPTER 3

TEST SOFTWARE FOR THE 9400

Table of Contents

3.0 Introduction

This chapter describes 9400 tests which require the use of LeCroy software. The 9400 software includes a small number of test routines which can be controlled from the front panel - these are described in (3.1). The other software system described here is a series of routines operating under CP/M on the LeCroy 3500. For these a 4928 tester board is also required. In (3.2) a brief outline of the system is given, together with a copy of each menu. Because the system is easy to use, only a few of the operations are described in detail in this section.

Note

The following sections apply only to versions V2.0 and higher. If your Model 9400 has an earlier software version (check on the upper right hand corner of the "Memory STATUS" display page), please ask your LeCroy contact person for an update of your scope's software.

For further information on the comprehensive software package CALSOFT (order code CS01, CS02) for 9400 adjustment and calibration, refer to the CALSOFT operator's manual.

3.1 Internal Test Software of the 9400

3.1.2 Turn On

1. Check that the correct line voltage is set on the rear-panel power connector. 9400s which have ELBA power supplies (this can be recognized by the 4 adjustment potentiometers below the 4 green LEDs on the right upper side of the rear panel) must be modified both externally on the power connector and internally on the power supply board (by changing the position of the power-connector).

2. Check the following:

   a) that the display turns on after about 10 sec.

   b) that the display is stable (if traces are displayed, turn them all off).

   c) that the range of INTENSITY and GRID INTENSITY is reasonable.

3. Wait about 10 minutes for the 9400 to reach a stable temperature.

3.1.3 Test for Low Frequency Noise on the Input

This test verifies that the front-end components, ADC and power supplies operate correctly. Low frequency noise may be observed if any of the power supplies oscillate.

1. Turn on the Channel 1 and 2 traces, turn the others off.

2. Set the 9400 so that a single grid is displayed on the screen.

3. Set the controls of the 9400 as follows:

   a) Input coupling: 1 MΩ, DC (Channels 1 and 2)
   b) Fixed gain: 5 mV/div (Channels 1 and 2)
   c) variable gain: 1 (Channels 1 and 2)

   d) Trigger - Slope: pos. or neg.
   Source: LINE
   Coupling: DC
   Mode: NORM
   Delay: zero

4. Setting the time base to 10, 5, 2, 1, and 0.5 msec/div in turn, check:

   a) that the displayed waveforms are constant bands with amplitudes less than 1/5 vertical division.
   b) that there is no discernible periodic structure.

5. Using the offset control, move the channel 1 and channel 2 traces slowly through the entire range and check that there is no change in the displayed trace. This is best seen by displaying only one trace at a time.

Solution to Problems

If there is a low frequency structure of the order of 1 kHz, check the following:

a) Is the lower RF-shield of the front-end correctly installed?
In some of the older versions, the screw head which holds the right-hand front foot of the lower 9400 cover may push the RF-shield towards the 9400-1 main board, creating shorts. Verify that the absence of the lower 9400 cover has no effect on the noise problem.

b) Have any of the 4 supply voltages oscillations of more than 50 mV (peak-to-peak) amplitude in the frequency range of 50 Hz to 200 kHz (check for time-base settings 10 msec/div through 10 µsec/div). If this is the case, the power supply must be repaired. Note that power supply oscillations may occur particularly at high temperatures (use a heat gun to verify a repair).

3.1.4 Preparation for Internal Tests

The 9400 is capable of executing a number of autonomous tests, the results of which are stored in reference memory C, and normally accessed through the (expanded) display controls. Whenever the test menu is entered (see Section 5), the entire memory C buffer is cleared and the 9400 is set up to display the expansion of memory C under trace "EXPAND A". When each individual test is performed, the 9400 automatically expands the display and centers it on the newly acquired histogram. You may nevertheless use the manual controls of "EXPAND A" to further modify the display, if so desired.

Note: When **Return** is pressed in the Test Modes menu the 9400 returns to the Main menu. During the internal tests the data in the memory locations of the 9400 are overwritten.

3.1.5 Entering the Internal Test Menu

1. Ensure that the 9400 is in the "root" menu, i.e. only "Main Menu" should appear on the left of the grid. Otherwise push the "Return" soft key until this is the case.

2. While keeping the lowest soft key (the one above SCREEN DUMP) pressed, push the top soft key "Main Menu". The "Test Modes" menu should appear.

3. To make sure that the 9400 triggers, set the trigger controls as follows:

    Trigger source: LINE
    Trigger mode: NORM

This ensures that the front-end is recalibrated whenever the input conditions are modified during the following test procedures.

3.1.6 Internal TDC Calibration

The 9400 calibrates the 10 psec time interpolator on the 100 MHz time base when the time base is modified. If this calibration fails (i.e. one of the peaks described below is missing), this may give rise to "jumps" in the display of INTERLEAVED waveforms at intervals of 10 nsec.

1. Push the fourth soft key "TDC-Cal, int. trig.". Within less than a second, the distribution displayed in the upper screen picture in Figure 3.1.6.1 should appear.

2. Check that the distribution contains 2 peaks, each at least 2 vertical divisions high.

3. Use the Position knob to center the left-hand peak on the display.

4. Turn the Time Magnifier knob clockwise to expand to 5 µsec/div.

5. Check that the width of the distribution is more than 1 horizontal division.

6. Repeat steps 3, 4 and 5 for the right-hand peak.

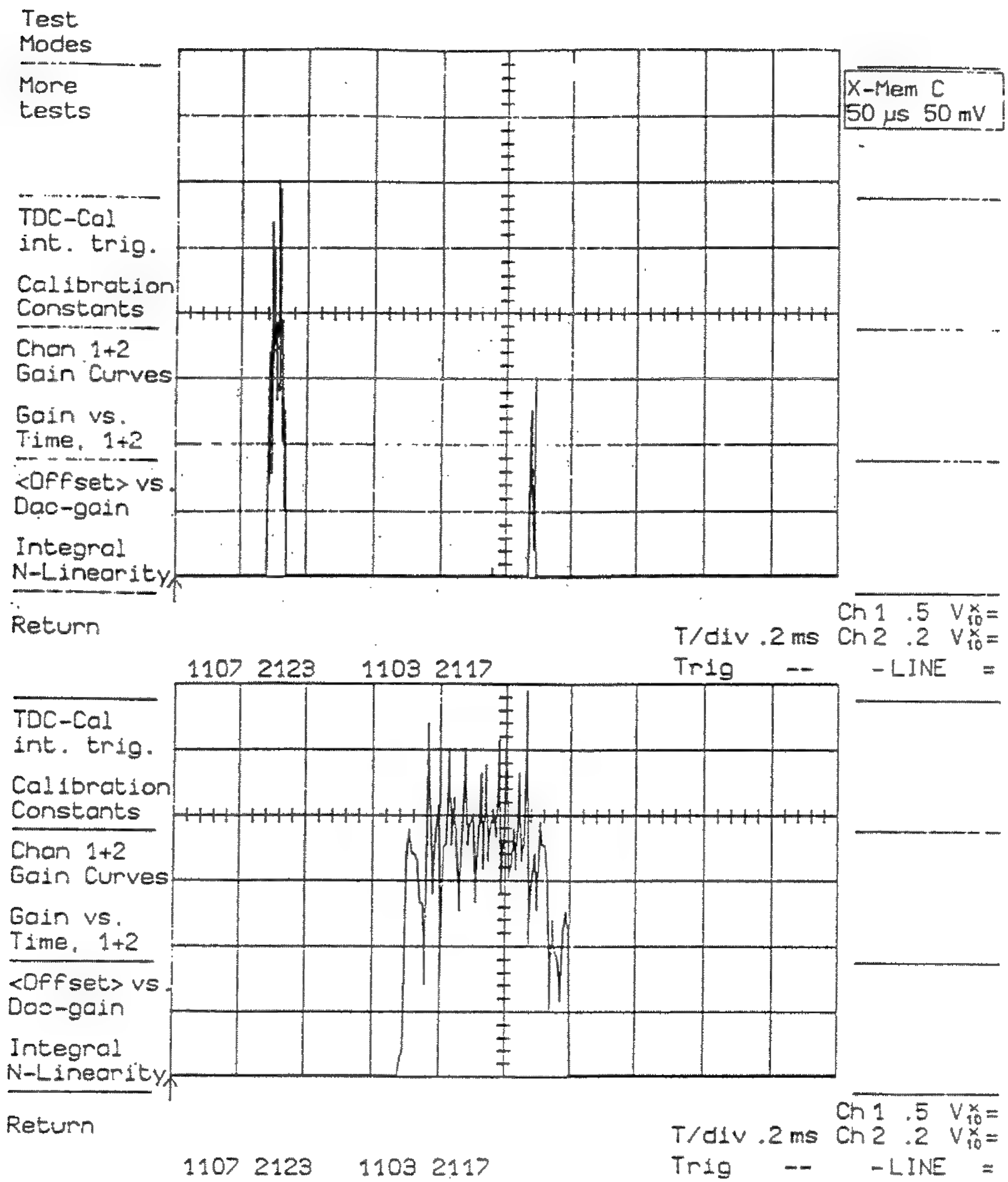
Solution to Problems

If either peak is missing or is too narrow, adjust the timing capacitor on the 9400-04 time-base card as follows:

1. Remove the top cover.

2. Locate the capacitor which is about 2 inches below the rear edge of the 9400-8 timing bus card.

3. Turn the capacitor 1/8 of a turn either way and check its effect by redoing the measurement, i.e. by pushing "TDC-Cal, int. trig."



INITIAL AND EXPANDED TDC TEST WAVEFORM

Figure 3.1.6.1

3.1.7 Gain Curves

This test allows the user to check whether the dynamic range of the programmable input amplifiers is sufficient. If it is not, the 9400 cannot calibrate itself correctly, giving rise to jumps of the ground line when turning the bandwidth limit on and off.

1. Set the bandwidth limit OFF.

2. Set the Channels 1 and 2 VOLTS/DIV controls to 5 mV/div.

3. Push the soft key "Chan 1 and 2 Gain Curves". The gain curves should appear within 5 seconds.

4. Check that the 2 gain curves (shown in Figure 3.1.7.1):

   a) are at least 1/4 division above the gain = 1 line on the left flat-top.

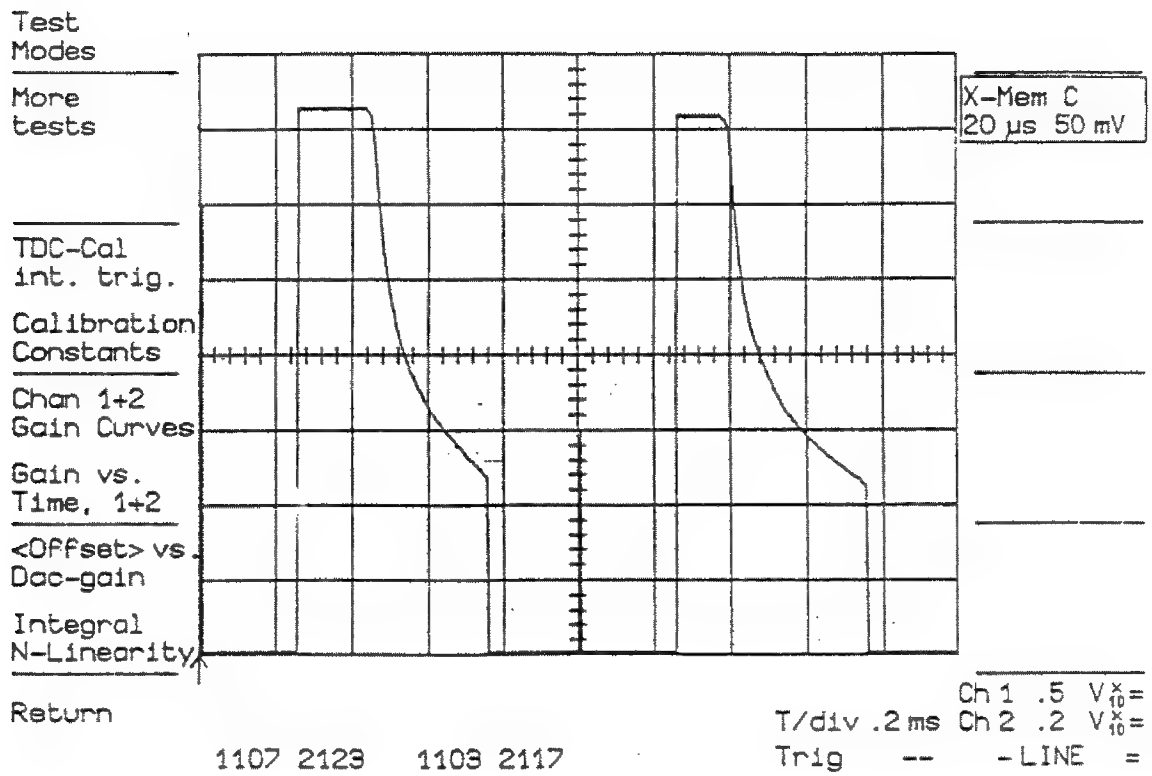
   b) decrease to at least 1/4 division below the gain = 0.4 line.

5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:

   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF

Solution to Problems

If the results of any of the tests (step 4) are not satisfactory, the HVV200 front-end hybrid of the corresponding channel must be changed.



GAIN CURVES

Figure 3.1.7.1

3.1.8 Gain vs. Time

This test permits the user to verify that the 9400 reliably measures the gain of the front-end amplifiers. It may not do so if there is noise present which influences the gain measurement. In this case, the calibration of the front-end may not work.

Note: this test is performed with the calibrated gain set to 1.00. The vertical scale is changed to 1 percent per division for easier observation. The absolute position of the measured gain is a measure of the precision of the gain calibration.

1. Set the Bandwidth Limit OFF.

2. Set the VOLTS/DIV control of channels 1 and 2 to 5 mV/div

3. Press the soft key "Gain vs. Time, 1 + 2". The new distributions should appear within 15 seconds.

4. Check the two curves (which should resemble those shown in Figure 3.1.8.1) as follows:

   The deviation from the center (1.0 gain) line should be within the following limits.

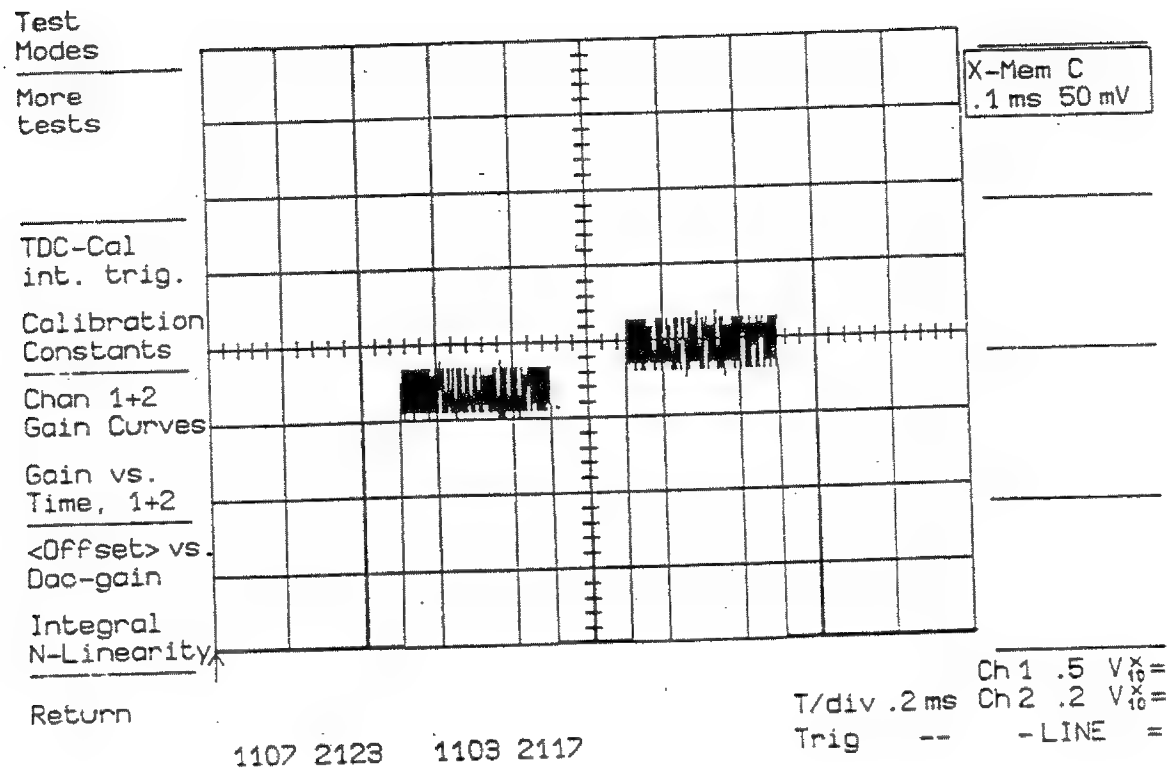
Gain	1% DSO	2% DSO
5 mV/div	± 1.5%	± 2%
other	± 0.8%	± 1.5%

5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:

   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF.
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF.

Solution to Problems

If the width of the band is too large, check for low frequency noise, (see Section 3.1.3).



GAIN VS. TIME CURVES

Figure 3.1.8.1

3.1.9 <Offset> vs. Gain-DAC

This test permits the user to check if the offset of the second front-end amplifier has been correctly adjusted.

1. Set the Bandwidth Limit OFF.

2. Set the VOLTS/DIV control of channels 1 and 2 to 5 mV/div.

3. Press the soft key "<Offset> vs. Dac-gain". The new curves should appear within 20 seconds.

4. Check the two offset curves (as shown in Figure 3.1.9.1)

   a) the curves should be rather horizontal, i.e. the difference between the left edge and the right edge should be less than 1 vertical division.

   b) the vertical position of the curve should lie in the 4 major central divisions.

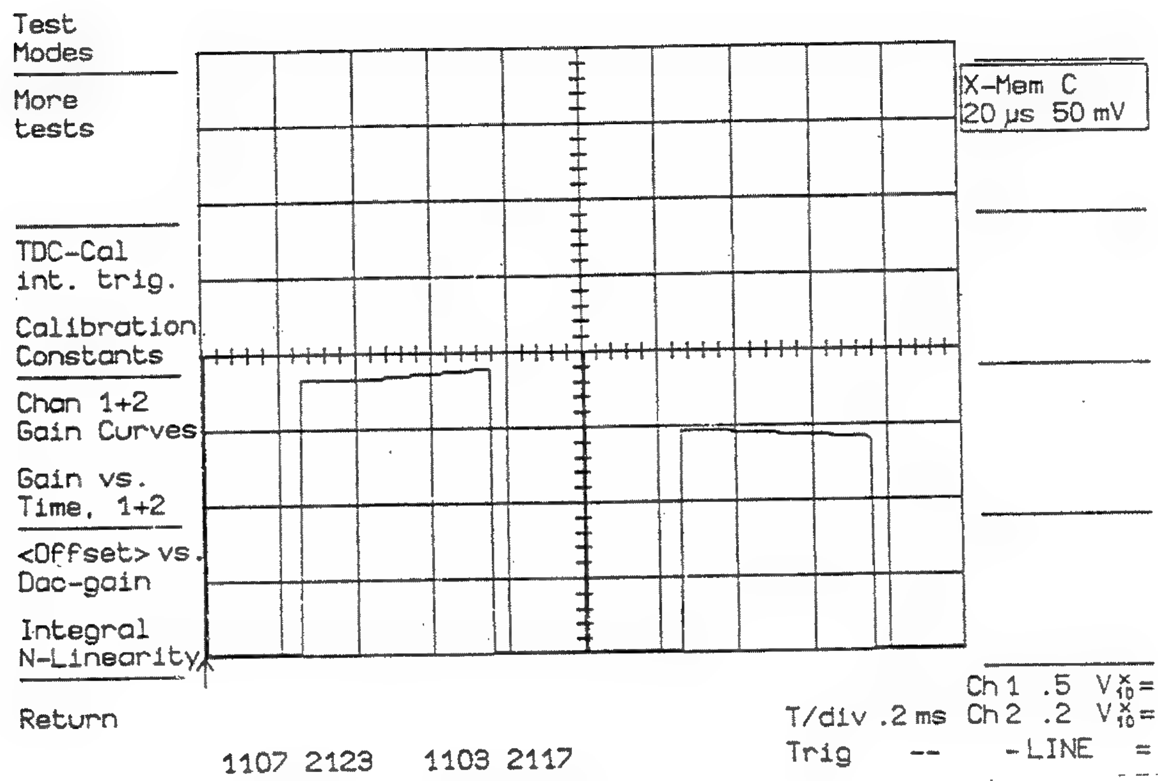
5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:

   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF.
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF.

NOTE: Since the adjustment of the output offset of the HVV200 is common to bandwidth limit ON and OFF, check that the deviations from a horizontal curve are as symmetrical as possible, i.e. by equal amounts above and below the center.

Solution to Problems

If an offset curve is not horizontal enough, the offset of the second amplifier (within the HVV200) must be readjusted. This requires a repetition of the calibration of the output offset of the corresponding HVV200.



OFFSET VS. GAIN DAC

Figure 3.1.9.1

3.1.10 Integral Non-Linearity

This test allows the user to check the DC integral non-linearity and the offset-calibration of the front-end amplifiers.

1. Set the Bandwidth Limit OFF.
2. Set the VOLTS/DIV control of channels 1 and 2 to 5 mV/div.
3. Press the soft key "Integral N-Linearity". The new curves should appear within about 10 seconds.
4. Check the integral non-linearity curves. (Figure 3.1.10.1 shows an example where the results for channel 1 are not satisfactory.)

   The curves must be within the following deviation from the center (0%) line. (1 division = 1%.)

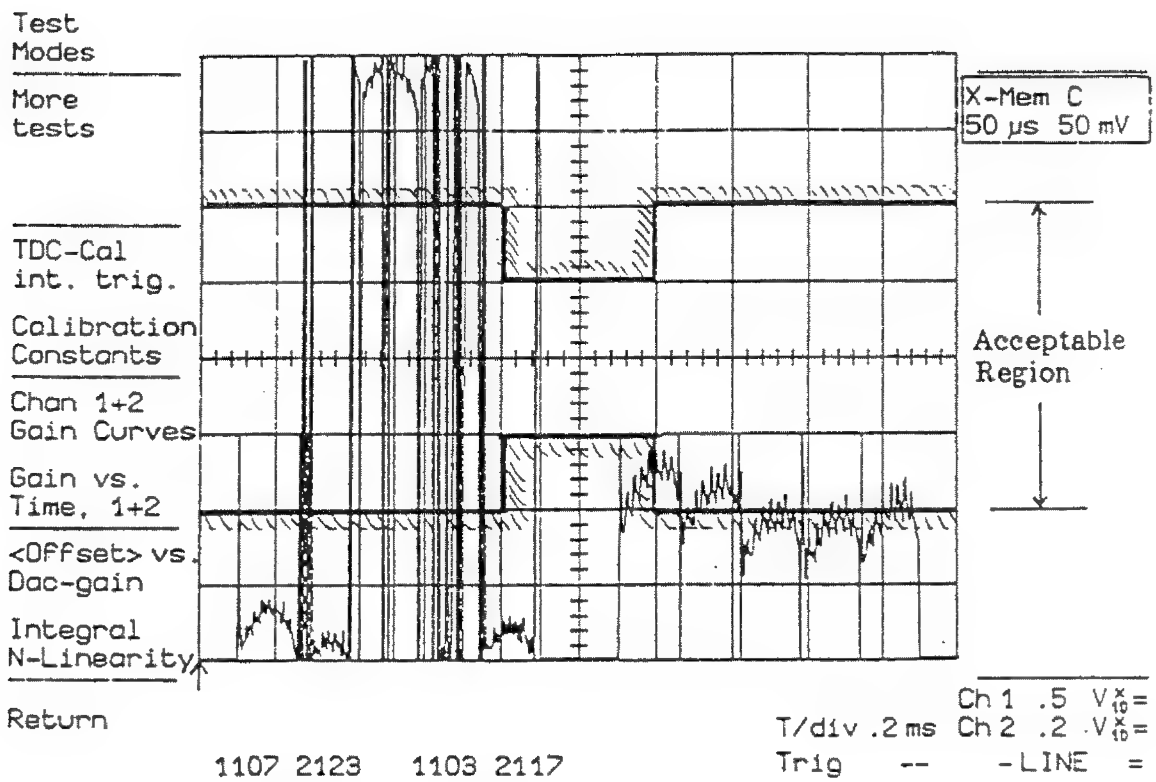
Curve	0 (leftmost)	1	2	3	4 (rightmost)
Gain					
5 mV/div	2.5%	2%	2%	2%	2.5%
other	2%	2%	1.5%	2%	2%

5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:

   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF.
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF.

Solution to Problems

If any of the curves is outside the limits, the HVV200 of the corresponding channel has an integral non-linearity of more than 1% and should be exchanged. However, a bad offset calibration may give rise to deviations outside this tolerance. This would show up as a systematic vertical offset of the outermost curves (of the 5 sub-curves) with respect to the other curves.



INTEGRAL NON-LINEARITY CURVES

Figure 3.1.10.1

3.2 Software for Use with the 4928 Tester

3.2.1 Introduction

The 4928 tester is a board with a connector at the top and bottom, in the standard DSO slot position, which enables it to be placed in communication with a 9400. It is used with software in the LeCroy 3500 to emulate the 68000 processor in a way which enables the 3500 to control each function of the DSO in turn, with the 68000 disabled. In addition, the 4928 has logic to process data at high-speed, to make the performance of the tests possible in a reasonable time (about 15 minutes for a complete set). This section of Chapter 3 includes a listing of all the menus available with this software.

3.2.2 Operation of the 4928 Tester

Note that the 4928 is normally placed above the 9401-2, but to use the 4928 with older 9400s containing the 9400-6 GPIB board, the 9400-6 is removed, the 4928 is put in the DMA slot, and the 9400-6 is placed on top of the 4928.

The 4928 can be put in any slot of the 3500, as the software will find it.

The software is "DSO" under CPM, i.e. it is called by -

A>DSO

The software is menu driven and interrupt driven, making it very easy to use. Help functions are available at all times.

A consistent pattern of control codes is used. The tests in any section are labeled A1, A2, A3.... where A is a letter.

Press An	for test n of group A
Press AH	for help for group A
Press A-	for complete set of tests A - except
C-	gives C0 and C1 only, because C2 is a short test
Press Z	for repeat of a test
Press J-	for loop on J1, non-interactive tests

The tests will not be described in great detail, because the screen listings are fairly clear, and the program is quite easy to use.

3.2.C Front Panel Test

This test enables all the front-panel controls to be tested individually in any order. The program presents an image on the display of the LeCroy 3500 which represents the display of the 9400 <3.2.C.1>.

The 3500's display symbols allow simple, quick tests of the controls.

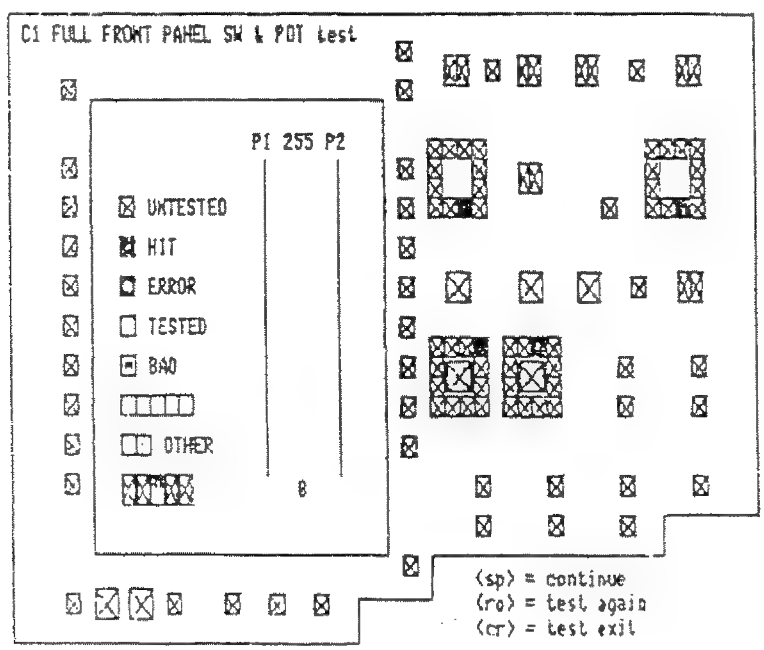
Push-buttons: push each button once. If it works, the symbol changes to an open rectangle. At the end of the sequence the unsatisfactory push-buttons can be tried again. If they still fail, a repair is needed.

Rotary switches: this test is the same as the push-button test.

Potentiometers: this test is slightly different. In order to test each potentiometer it is necessary to turn it all the way in each direction. The two vertical bars, P1 and P2, acquire little ticks which show where the ADC has measured the positions of the potentiometers. Two bars are needed for those controls which have no end stop, because these employ pairs of potentiometers joined in opposing orientation. When ticks have been made from one end to the other, the symbols will go clear.

LEDs test - CO: this test cycles through the LEDs at a speed determined by the operator.

Completion: when all the controls have been tested and found to be working, the program will flash all the LEDs in sequence.



DISPLAY ON 3500 FOR TEST C OF 9400 CONTROLS

Figure 3.2.C.1

3.2.P Tests of the CRT Image

These tests use section P of the "DSO" software.

3.3.P.1 Size, Position and Brightness

These basic attributes are tested with <3.3.1>, which is generated by test P1 of the "DSO" program (3.2). The four short lines should just touch the edge of the bezel. Any fault can be corrected by reference to (2.4.2.3) for size, (2.4.2.2) and (2.4.7.4) for position, and (2.4.7.2) for brightness.

The line "C" should be subjectively about half as bright as "A" below it. The region "B" should show a gradation from dark-to-light, left-to-right.

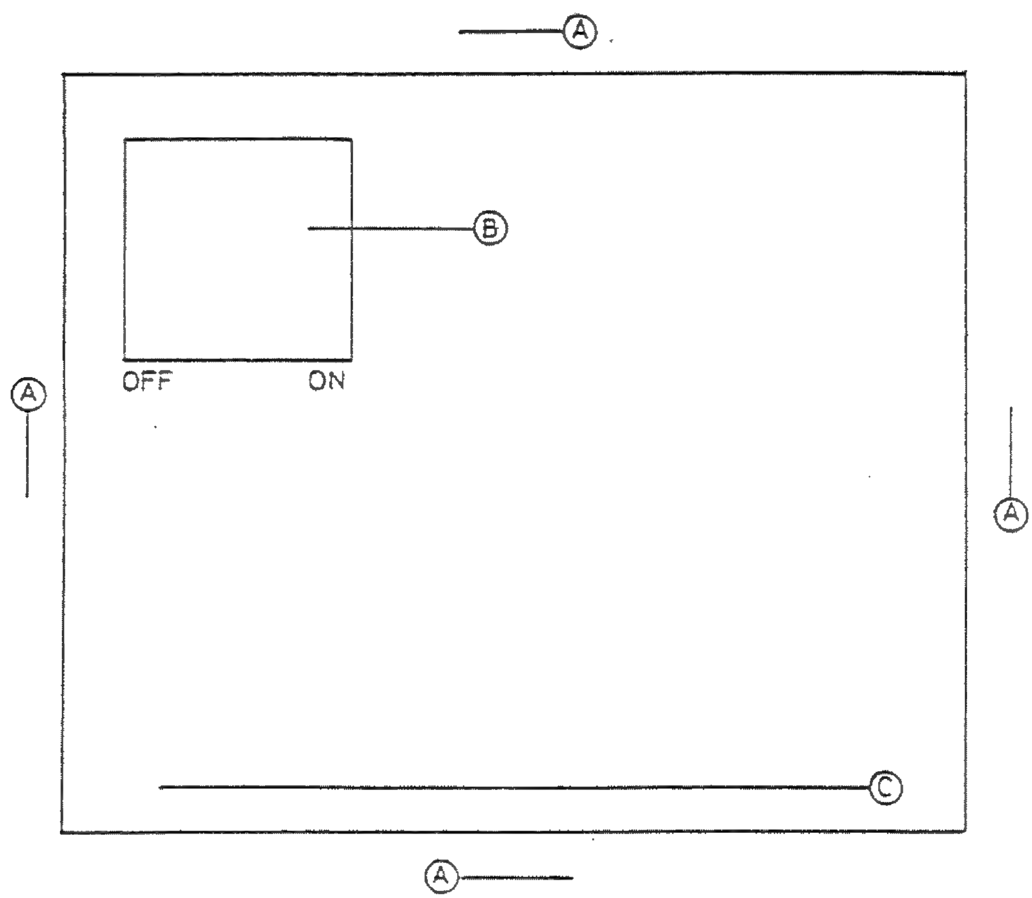


Figure 3.3.1

3.3.P.2 Tests of Vector Joining

These basic attributes are tested with <3.3.2>, which is generated by test P2 of the "DSO" program (3.2). The characters should be neatly drawn, and all the little vectors which add to make the lenticular shapes should neither overlap nor show gaps. Adjustment is possible (2.4.2.5).

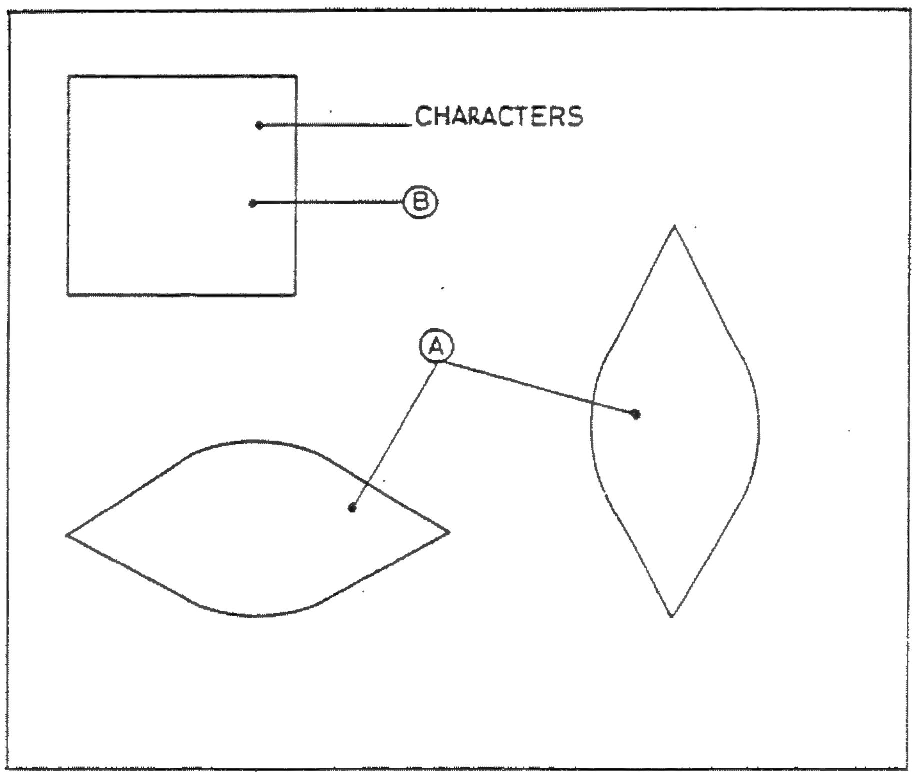


Figure 3.3.2

3.3.P.3 Tests of Amplifiers

See <3.3.3> for the images, which are generated by test P4 of the "DSO" program. The diagonals should be made of double bars no more than 5 mm apart. The triangles should be uniformly bright. If they are not, check the amplifier quiescent currents (2.4.2.6).

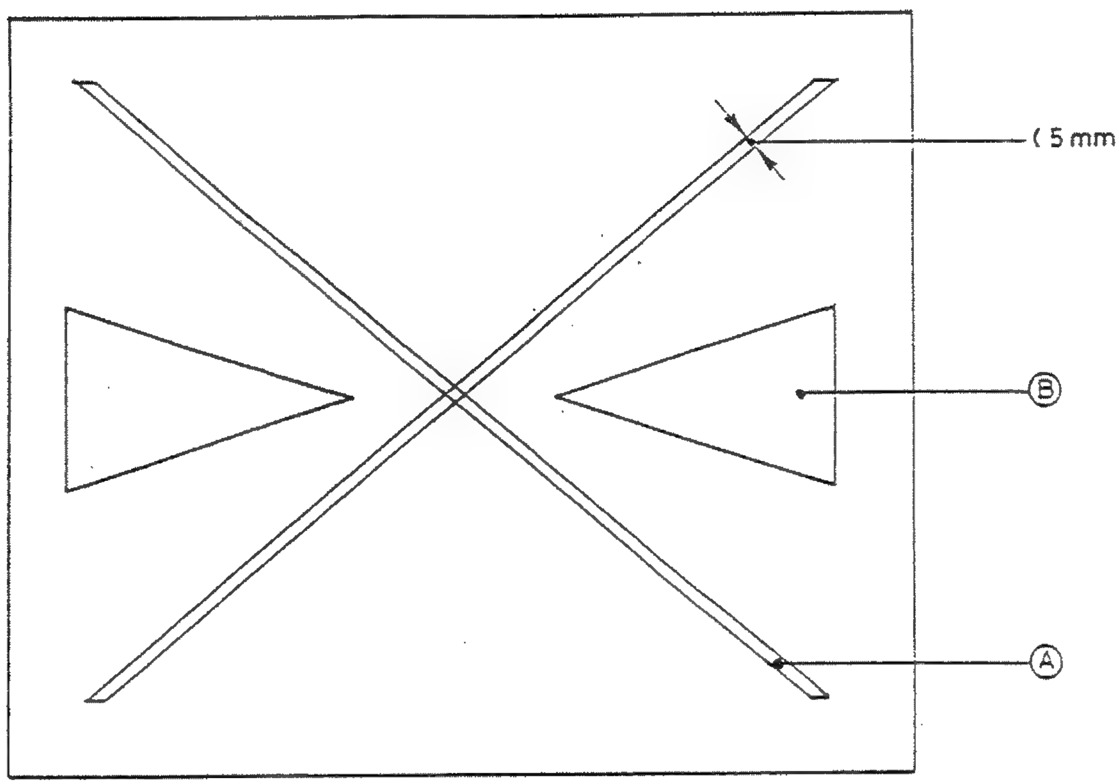
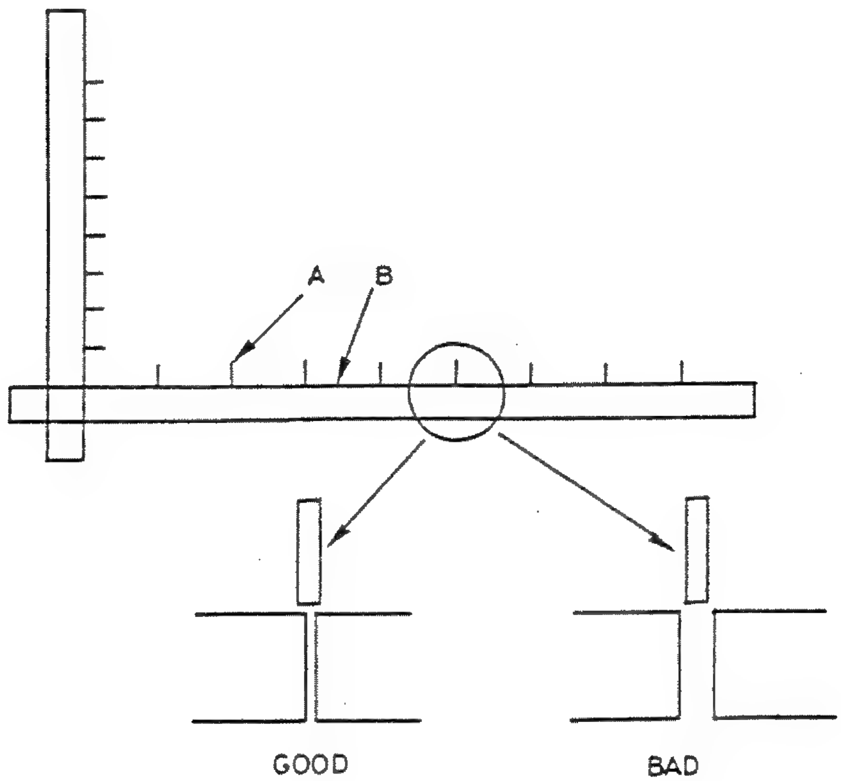


Figure 3.3.3

3.3.P.4 Tests of X and Y DACs

See <3.3.4> for the images, which are generated by test P3 of the "DSO" software. The "ticks" correspond to the places where errors are most likely, i.e. at large bit changes. Any dark bands on the wide bright stripes should be narrower than the tick. If not, the DAC may be at fault (1.2.3).



SIZE, POSITION AND BRIGHTNESS

Figure 3.3.4

```
==== Updated version 11 march 1986 BM LeCroy SA Geneva Switzerland ====


++++++ 9400 DSO MAIN TEST PROGRAM (overlayed program) ++++++


----- CRATE 0 --- SLOT  1 -----

    hit 'H' for HELP option

? H
 An = ADC test           B  = BOOT CPU / RUN
 Cn = FRONT PAN test     Dn = DYN RAM test
 En = EPROM test         Fn = FPY DISK test
 Gn = GPIB test          H  = HELP
 In = RT CLOCK test      Jn = ALL POSS TEST
 Kn = TIMER test         Ln = MULTIPL test
 Mn = MINMAX test        Nn = CALIB DAC test
 On = ADD RAM test       Pn = DISPLAY test
 Qn = BUS test           Rn = RS-232 test
 Sn = STAT RAM test      Tn = TIMEBASE test
 Un = CPU test           V  = DSO ADDR TABLES
 W  = MISCELL TABLES     X  = SWITCHES STATUS
 Y  = DEBUGGER           Z  = SAME TEST

  n = 0 to 9 : specific test
  n = - : all test        n = H : option help

<lf>= TEST EXIT        <esc>= RESTART PROGR
  : = STOP ERR on/off     ; = RUN ERR on/off
  . = TEST LOOP on/off    . = CPU RUN on/off
  / = PRINTER on/off      \ = PRINT ERROR on/off
<cr>= CONTINUE          <sp>= DATA SEPARATOR
<ro>= RUBOUT             ^C = PROGRAM EXIT

? AH

----ADC test----
A- = ADC RESPONSE test
? B
BOOT CPU
        0 LOC errors
```

```
?
?
? CH

----FRONT PANEL test----
C0 = LED test
C1 = POT & SWITCHES full test
C- = FULL TEST
C2 = POT & SWITCHES short test
? D\C0

----FRONT PANEL test----
C0 = LED test
 H => command HELP

  s7  seq  -LED RUN-


     1-6 => sample CYCLE select   or  7-0 => SPEED select
  or  <sp> => return to CYCLES SEQUENCE (1-6)
  or  A1 to D8 => select LED on  (with 0 cleen)

c ! CH1  ! CH2  ! TR CPL ! TR SCE ! TR MODE ! T SL ! MISCEL !
1 !------!------!--------!--------!---------!------!--------!
2 ! AC   ! AC   ! AC     ! CH1    ! READY   !      ! REMOTE !
3 ! GND  ! GND  ! LFREJ  ! CH2    ! SEQNCE  ! POS  !        !
4 ! DC   ! DC   ! HFREJ  ! LINE   ! AUTO    ! NEG  ! BDWTHL !
5 ! GND  ! GND  ! DC     ! EXT    ! NORM    !      ! OVERLD !
6 ! DC50 ! DC50 ! TRIG'D ! EXT/10 ! SINGLE  !      ! INTSPL !


Xo !  1   !  2   !  3   !  4   !  5   !  6   !  7   !  8   !
---!------!------!------!------!------!------!------!------!
 A ! REMOT! BDWHL! OVLD1! AC1  ! GND1 ! DC1  ! GND1 ! DC501!
 B ! READY! TR'D ! OVLD2! AC2  ! GND2 ! DC2  ! GND2 ! DC502!
 C ! SEQU ! AUTO ! NORM ! SINGL! AC   ! LFREJ! HFREJ! DC   !
 D ! ITSPL! +SLP ! -SLP ! CHAN1! CHAN2! LINE ! EXT  ! E/10 !

  s7  seq  -LED RUN-
? DH

----DYNAMIC RAM test----
D0 = 0000 and ffff test
D1 = ADDRESS test (address to address)
D2 = 55,aa,99 and 66 shifted test (4 pass)
D3 = 0001 and fffe shifted test (32 pass)
D4 = BYTE test (00ff and ff00)
D- = FULL TEST
? EH

----EPROM test----
E0 = PATTERN test
E1 = CPU BUS ADDR partial test
E2 = EPROM FULL VERIFY
E- = FULL TEST
E3 = EPROM SAVE TO DISK
E4 = E2 if disk file not found
?
?
?
```

```
?
?
? FH
F #### not implemented function ####
?
?
? GH

----GPIB PORT test----
G0 = SWITCHES read test
G1 = SER POLL & ADDR REG W/R test
G2 = INTERR (both sources) test
G3 = not implemented
G4 = not implemented (use IBM-PC-AT)
G- = FULL TEST
?
? H
 An = ADC test             B  = BOOT CPU / RUN
 Cn = FRONT PAN test       Dn = DYN RAM test
 En = EPROM test           Fn = FPY DISK test
 Gn = GPIB test            H  = HELP
 In = RT CLOCK test        Jn = ALL POSS TEST
 Kn = TIMER test           Ln = MULTIPL test
 Mn = MINMAX test          Nn = CALIB DAC test
 On = ADD RAM test         Pn = DISPLAY test
 Qn = BUS test             Rn = RS-232 test
 Sn = STAT RAM test        Tn = TIMEBASE test
 Un = CPU test             V  = DSO ADDR TABLES
 W  = MISCELL TABLES       X  = SWITCHES STATUS
 Y  = DEBUGGER             Z  = SAME TEST

  n = 0 to 9 : specific test
  n = - : all test         n = H : option help

<lf>= TEST EXIT         <esc>= RESTART PROGR
  : = STOP ERR on/off      ; = RUN ERR on/off
  . = TEST LOOP on/off     , = CPU RUN on/off
  / = PRINTER on/off       \ = PRINT ERROR on/off
<cr>= CONTINUE          <sp>= DATA SEPARATOR
<ro>= RUBOUT               ^C = PROGRAM EXIT

?
? IH

----RTC test----
I0 = RTC SCALERS test
I1 = RTC set
I2 = RTC read
I- = FULL TEST
?
?
?
?
?
?
?
?
?
?
?
?
```

```
J1 = ALL NO INTERACT. tests
     CBQ-E-K-D-S-O-M-L-P-N-C-R-G-A-T-I-U-

J2 = ALL 9400-1 INTERACT. tests ONLY
     CBS4C2E4NON1N2BB

J3 = ALL FULL 9400 INTERACT. tests
     CBS4C1P1P2P3P4R3R4GOE4I1N1N2BB

J4 = J1 & J2 FULL SAMPLE MOTHER CARD test
     CBQ-E-K-D-S-O-M-L-P-N-C-R-G-A-T-I-U-
     CBS4C2E4NON1N2BB

J5 = J1 & J3 FULL DSO tests (CS)
     CBQ-E-K-D-S-O-M-L-P-N-C-R-G-A-T-I-U-
     CBS4C1P1P2P3P4R3R4GOE4I1N1N2BB

J6 = 9401-2 CARD tests
     Q-O-I-G-
?
? KH

----TIMER test----
K0 = FULL TEST (80 sec test)
K- = SHORT TEST (6 sec test for 1/16)
?
? LH

----MULTIPLIER test----
L0 = SIGNED DIRECT access test (380)
L1 = SIGNED INDIR write access test (380)
L2 = SIGNED SQUARE test (36)
L3 = UNSIGN DIRECT access test (342)
L4 = UNSIGN INDIR write access test (342)
L5 = UNSIGN SQUARE test (36)
L6 = SIGNED SPEC PATTERN test (direct addr)
L7 = UNSIGN SPEC PATTERN test (direct addr)
L- = FULL TEST
L8 = SIGNED LONG test (65536) take 49 min
L9 = UNSIGN LONG test (65536) take 43 min
?
? MH

----MIN/MAX test----
M0 = BYTES DIRECT addr access (34)
M1 = BYTES INDIR write addr access (4)
M2 = WORD DIRECT addr access (74)
M3 = WORD INDIR write addr access (4)
M4 = RE-READ MIN/MAX (INDIR WORD format)
M- = FULL TEST
?
?
?
? NH

----CALIB DAC test----
N0 = DAC calibration
N1 = PROBE CAL DC calibration
N2 = PROBE CAL AC test
N3 = DAC/ADC test
N4 = S&H crosstalk test
N- = FULL TEST
```

```
J- = J1 LOOP for long test (stop loop with ".")
J0 = ALL tests
J1 = ALL NO INTERACT. tests
     CBQ-E-K-D-S-O-M-L-P-N-C-R-G-A-T-I-U-

J2 = ALL 9400-1 INTERACT. tests ONLY
     CBS4C2E4NON1N2BB

J3 = ALL FULL 9400 INTERACT. tests
     CBS4C1P1P2P3P4R3R4G0E4I1N1N2BB

J4 = J1 & J2 FULL SAMPLE MOTHER CARD test
     CBQ-E-K-D-S-O-M-L-P-N-C-R-G-A-T-I-U-
     CBS4C2E4NON1N2BB

J5 = J1 & J3 FULL DSO tests (CS)
     CBQ-E-K-D-S-O-M-L-P-N-C-R-G-A-T-I-U-
     CBS4C1P1P2P3P4R3R4G0E4I1N1N2BB

J6 = 9401-2 CARD tests
     Q-O-I-G-
?
? KH

----TIMER test----
K0 = FULL TEST (80 sec test)
K- = SHORT TEST (6 sec test for 1/16)
?
? LH

----MULTIPLIER test----
L0 = SIGNED DIRECT access test (380)
L1 = SIGNED INDIR write access test (380)
L2 = SIGNED SQUARE test (36)
L3 = UNSIGN DIRECT access test (342)
L4 = UNSIGN INDIR write access test (342)
L5 = UNSIGN SQUARE test (36)
L6 = SIGNED SPEC PATTERN test (direct addr)
L7 = UNSIGN SPEC PATTERN test (direct addr)
L- = FULL TEST
L8 = SIGNED LONG test (65536) take 49 min
L9 = UNSIGN LONG test (65536) take 43 min
?
? MH

----MIN/MAX test----
M0 = BYTES DIRECT addr access (34)
M1 = BYTES INDIR write addr access (4)
M2 = WORD DIRECT addr access (74)
M3 = WORD INDIR write addr access (4)
M4 = RE-READ MIN/MAX (INDIR WORD format)
M- = FULL TEST
?
?
?
? NH

----CALIB DAC test----
N0 = DAC calibration
N1 = PROBE CAL DC calibration
N2 = PROBE CAL AC test
N3 = DAC/ADC test
N4 = [illegible]
```

```
00 = 0000 and ffff test
01 = ADDRESS test (address to address)
02 = 55,aa,99 and 66 shifted test (4 pass)
03 = 0001 and fffe shifted test (32 pass)
04 = BYTE test (00ff and ff00)
0- = FULL TEST
?
? PH

----DISPLAY test----
P0 = DISPLAY PAGES test
P1 = DISPLAY SCREEN SIZE and INTENSITY calibr
P2 = DISPLAY VECTORS LENGTH calibr
P3 = DISPLAY VECTORS SPEED test
P4 = DISPLAY LINAERITY test
P- = FULL TEST
?
? QH

----BUS test----
Q0 = HALT RESET INTER & STATIC BUS test (6 cycles)
Q1 = SAMPLE CYCLES test (8 in DMA mode with 4928)
Q2 = ADDRESS BUS test (65 in DMA mode)
Q3 = DATA BUS test (38 in DMA mode)
Q- = FULL TEST
?
? RH

----RS232 PORT test----
R0 = PORT-1/2 reg test
R1 = PORT-1 LOOP BACK test (internal conn)
R2 = PORT-2 LOOP BACK test (internal conn)
R3 = PORT-1 -> PORT-1/2 test (external conn)
R4 = PORT-2 -> PORT-2/1 test (external conn)
R- = FULL TEST
R5 = RS232 FULL DUPLEX test
?
? SH

----STATIC RAM test----
S0 = 0000 and ffff test
S1 = ADDRESS test (address to address)
S2 = 55,aa,99 and 66 shifted test (4 pass)
S3 = 0001 and fffe shifted test (32 pass)
S4 = NON-VOLATILE test
S- = FULL TEST
?
?
?
?
?
?
?
?
?
?
?
?
?
?
?
?
?
```

```
?
?
? TH

----TDC test----
T- = TDC RESPONSE test
?
? UH

----CPU test----
U0 = SAMPLE CPU CYCLES test (7 first)
U1 = BOOT CPU AND RUN test
U2 = AUTO-REBOOT test
U3 = BOOT CPU
U- = FULL TEST
?
? V
 W  h000000-h07ffff = EPROM
 -  h080000-h17ffff = reserved
U&L h180000-h18ffff = GPIB,RTC (& FLPY DISK)
 W  h190000-h19ffff = TIMEBASE
W/L h1a0000-h1affff = FRONT PANEL & INPUT COUPL
 U  h1b0000-h1bffff = RS-232C 1 & 2
W B h1c0000-h1cffff = MULTIPLIER & MIN/MAX
w L h1d0000-h1dffff = NON VOLATILE RAM
w L h1e0000-h1effff = DISLAY PAGE (& START ACCES RAM)
 W  h1f0000-h1fffff = TIMER
W B h200000-h27ffff = DYNAMIC RAM
(W) h280000-h2fffff = reserved (h2a8xxx = 4928)
U&L h300000-h37ffff = ADC1 & ADC2
W B h380000-h3fffff = ADD RAM (on cust connect)
W B+h400000+h800000 = dir acc MULT & MIN/MAX
 W  h200000-h2027fe = 1rst DISPLAY PAGE
 W  h202800-h204ffe = 2nd  DISPLAY PAGE
 W  h205000-h20500e = S&H INPUT CNTR

int 1 = FRT PAN       int 2 = (FLPY DISK)
int 3 = RS-232-1      int 4 = RS-232-2
int 5 = TRIGGER       int 6 = GPIB
int 7 = TESTER (4928) 1 -> 7 incr priority

?
? OH

----ADD DYNAMIC RAM test----
00 = 0000 and ffff test
01 = ADDRESS test (address to address)
02 = 55,aa,99 and 66 shifted test (4 pass)
03 = 0001 and fffe shifted test (32 pass)
04 = BYTE test (00ff and ff00)
0- = FULL TEST
?
?
?
?
?
?
?
?
```

```
?
?
?
?
? W
 A--SAMPLE&HOLD RAM ADDR
h205000 = GAIN CH1    h205002 = GAIN CH2
h205004 = OFFS CH1    h205006 = OFFS CH2
h205008 = TRIG HI LEV h20500a = TRIG LO LEV
h20500c = CAL CH(1&2) h20500e = PROBE CAL ->ADC last

 B--FRONT PANEL LEDS AND FRONT END COMMANDS (shift reg)
1: REM   BDWH [OVLD  AC    GND   DC    GND   DC50] LCH1
2:[READY TRID][OVLD  AC    GND   DC    GND   DC50] LCH2
3:[SEQU  AUTO  NORM  SINGL AC    LFREJ HFREJ DC   ] LTRG
4  ISPL [+SLP  -SLP][CHAN1 CHAN2 LINE  EXT   E/10] LTRG
5:[TCH1\ TCH2\ TEXT\ TLIN\ TDC\  THFR\ TAC\  TLF\] CTRG
6:[PRCAC ---   BWL1  BWL2][EXT/1 +EDGE -EDGE --- ] CTRG
7;[HI\50 AC\DC /1    /10   /120  G*8\  G*4\  G*2\] CCH2
8;[HI\50 AC\DC /1    /10   /120  G*8\  G*4\  G*2\] CCH1


**** hit <cr> to continue ****

 C--FRONT PANEL (POT&SW) and FRONT END READ (#=interr)
h1a0000 # P1            h1a0002 # P2 DIFF CURS
h1a0004 # P1            h1a0006 # P2 REF CURS
h1a0008 # P1            h1a000a # P2 TR DELAY
h1a000c # P1            h1a000e # P2 HOR POS
h1a0010 # P1            h1a0012 # P2 VERT POS
h1a0014 # P1            h1a0016 # P2 VERT GAIN
h1a0018 # P TRIG LEV    h1a001a # P VAR GAIN 2
h1a001c # P OFFSET 2    h1a001e # P VAR GAIN 1
h1a0020 # P OFFSET 1    h1a0022 # P INTENSITY
h1a0024 # P GRID INT    h1a0026 # OVLD 2
h1a0028 # OVLD 1        h1a002a # TRIG LEV
h1a002c # TEMP          h1a002e # PRCAL/DAC(last)
h1a0030 = TIME/DIV      h1a0032 = TIME MAG
h1a0034 = VOLT/DIV 2    h1a0032 = VOLT/DIV 1
h1a0038 < ZERO  SLOPE C1CP- C1CP+ C2CP- C2CP+
          TRSC- TRSC+ TRCP- TRCP+ TRMD- TRMD+ >
h1a003a < spare ---   ---   ---   INSPL RESET
          BDWH  2GRID CUMKR CUTME CUVLT CUTRK >
h1a003c < ---   ---   SELCT REDEF CHAN2 CHAN1
          F-FCT E-FCT D-MEM C-MEM B-EXP A-EXP >
h1a003e < SCDMP spare STORE SK-9  SK-8  SK-7
          SK-6  SK-5  SK-4  SK-3  SK-2  SK-1  >

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----DSO DEBUGGER--

Y?
Y?
 (,) cpu halt          (\) no print error   (/) no print all
 (:) no stop error     (;) no run error     (.) no test loop
Y?
Y?
B                 =BOOT CPU
C                 =CLEAR (reset)
G haaa            =GO CPU
D haaa            =DISPLAY  (a)->v
S haaa hvv        =SET       (a) v->v (verify)
R haaa hnn        =READ      (a)++->v (n time)
W haaa hvv hnn =WRITE     v->(a)++ (n time)
P haaa            =PUT       a->(a)-- (to ha00)
I haaa hvv        =INSERT  sv->(a)-- (to haoo)
V                 =VERIFY  (after P or I option)
E                 =EXECUTE CPU SINGLE CYCLE
T                 =TRACE CPU (list)
A hvv haaa        =AT VALUE / addr STOP CPU
L                 =LINES STATUS
F hn              =FORMAT BYTE / WORD / DMA hold
X                 =FLAG status

haaa =ADDRESS (6dig hex)    hvv =DATA (4dig hex)
hnn  =NB CYCLE (4dig hex)  =0 LOOP  <0 SPEC option

Y?
? Y

----DSO DEBUGGER----

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 (,) cpu halt          (\) no print error   (/) no print all
 (:) no stop error     (;) no run error     (.) no test loop
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Y?
Y?
TRACE RUNNING CPU (<sp> or new option)
(h000000) h0022 RsW Prom
(h000002) h0000 RsW Prom
(h000004) h0000 RsW Prom
(h000006) h0150 RsW Prom
(h000150) h4e71 RsW Prom
(h000152) h207c RsW Prom
(h000154) h0000 RsW Prom
(h000156) h0172 RsW Prom
(h000158) h227c RsW Prom
(h00015a) h0020 RsW Prom
(h00015c) h5010 RsW Prom
(h00015e) h203c RsW Prom
(h000160) h0000 RsW Prom
(h000162) h0004 RsW Prom
(h000164) h5380 RsW Prom
(h000166) h32d8 RsW Prom
(h000168) h51c8 RsW Prom
(h000172) h4ef9 RsW Prom
(h205010) h4ef9 W W DRam
(h00016a) hfffc RsW Prom
(h000166) h32d8 RsW Prom
(h000168) h51c8 RsW Prom
(h000174) h0000 RsW Prom
(h205012) h0000 W W DRam
(h00016a) hfffc RsW Prom
(h000166) h32d8 RsW Prom
(h000168) h51c8 RsW Prom
(h000176) h01e0 RsW Prom
(h205014) h01e0 W W DRam
(h00016a) hfffc RsW Prom
(h000166) h32d8 RsW Prom
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J- = J1 LOOP for long test (stop loop with '.')
J0 = ALL tests
J1 = ALL NO INTERACT. tests
     CBQ-E-K-D-S-O-M-L-P-N-C-R-G-A-T-I-U-

J2 = ALL 9400-1 INTERACT. tests ONLY
     CBS4C2E4NON1N2BB

J3 = ALL FULL 9400 INTERACT. tests
     CBS4C1P1P2P3P4R3R4GOE4I1N1N2BB

J4 = J1 & J2 FULL SAMPLE MOTHER CARD test
     CBQ-E-K-D-S-O-M-L-P-N-C-R-G-A-T-I-U-
     CBS4C2E4NON1N2BB

J5 = J1 & J3 FULL DSO tests (CS)
     CBQ-E-K-D-S-O-M-L-P-N-C-R-G-A-T-I-U-
     CBS4C1P1P2P3P4R3R4GOE4I1N1N2BB

J6 = 9401-2 CARD tests
     Q-O-I-G-
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Y?
Y?
Y?
Y?
 (,) cpu halt          (\) no print error    (/) no print all
 (:) no stop error     (;) no run error      (.) no test loop
Y?
Y?
Y?
TRACE RUNNING CPU (<sp> or new option)
(h000000) h0022 RsW Prom
(h000002) h0000 RsW Prom
(h000004) h0000 RsW Prom
(h000006) h0150 RsW Prom
(h000150) h4e71 RsW Prom
(h000152) h207c RsW Prom
(h000154) h0000 RsW Prom
(h000156) h0172 RsW Prom
(h000158) h227c RsW Prom
(h00015a) h0020 RsW Prom
(h00015c) h5010 RsW Prom
(h00015e) h203c RsW Prom
(h000160) h0000 RsW Prom
(h000162) h0004 RsW Prom
(h000164) h5380 RsW Prom
(h000166) h32d8 RsW Prom
(h000168) h51c8 RsW Prom
(h000172) h4ef9 RsW Prom
(h205010) h4ef9 W W DRam
(h00016a) hfffc RsW Prom
(h000166) h32d8 RsW Prom
(h000168) h51c8 RsW Prom
(h000174) h0000 RsW Prom
(h205012) h0000 W W DRam
(h00016a) hfffc RsW Prom
(h000166) h32d8 RsW Prom
(h000168) h51c8 RsW Prom
(h000176) h01e0 RsW Prom
(h205014) h01e0 W W DRam
(h00016a) hfffc RsW Prom
(h000166) h32d8 RsW Prom
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CHAPTER 4

CABLES AND CONNECTORS IN THE 9400

Table of Contents

4.1 This section is a compilation of data for the cables and connectors used in the 9400 DSO. For information on the part numbers and further information use Chapter 6. The positions of the cables are shown in the diagrams accompanying Chapter 4.

4.2 **Warning**

- Do not remove any connector while the scope is under power, unless you are sure that this action will not cause damage.

- Do not insert any connector while the scope is under power, unless you are sure that this action will not cause damage.

- Some cables carry high voltages when the DSO is under power. These voltages may persist after the DSO has been switched off, and therefore great care is needed when handling these cables. (5.3)

- Some connectors are very firmly seated, for example the small coaxial SMB connectors linking the ADC and TDC boards to the 9400-1. These should never be removed by pulling the cables.

- Removal of certain cables when the scope is running will cause damage, for example the cables from the 9400-2 to the deflection yoke. If the deflection current is lost in one direction, the trace becomes a brilliant line; if both deflections are lost, the resulting brilliant point will probably damage the phosphor irretrievably.

4.3 List of Cables Used in the LeCroy 9400 DSO

The following list is of cables with a connector at each end.

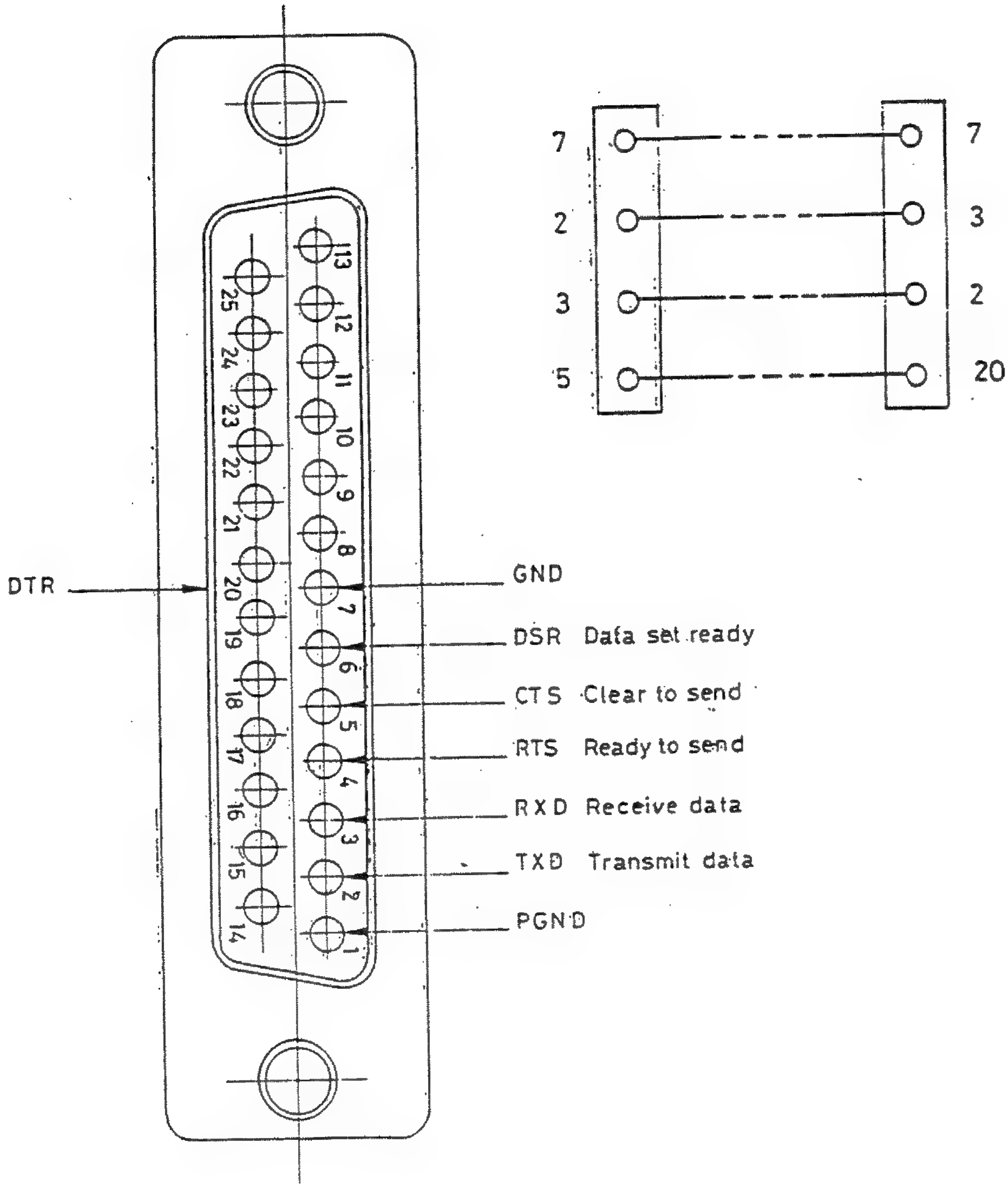
Title	Function	From	To	Cable	Connector
H6	Panel control	9400-1	9400-5	34 ribbon	34 IDC 2-row

The following list is of cables which are anchored at one end.

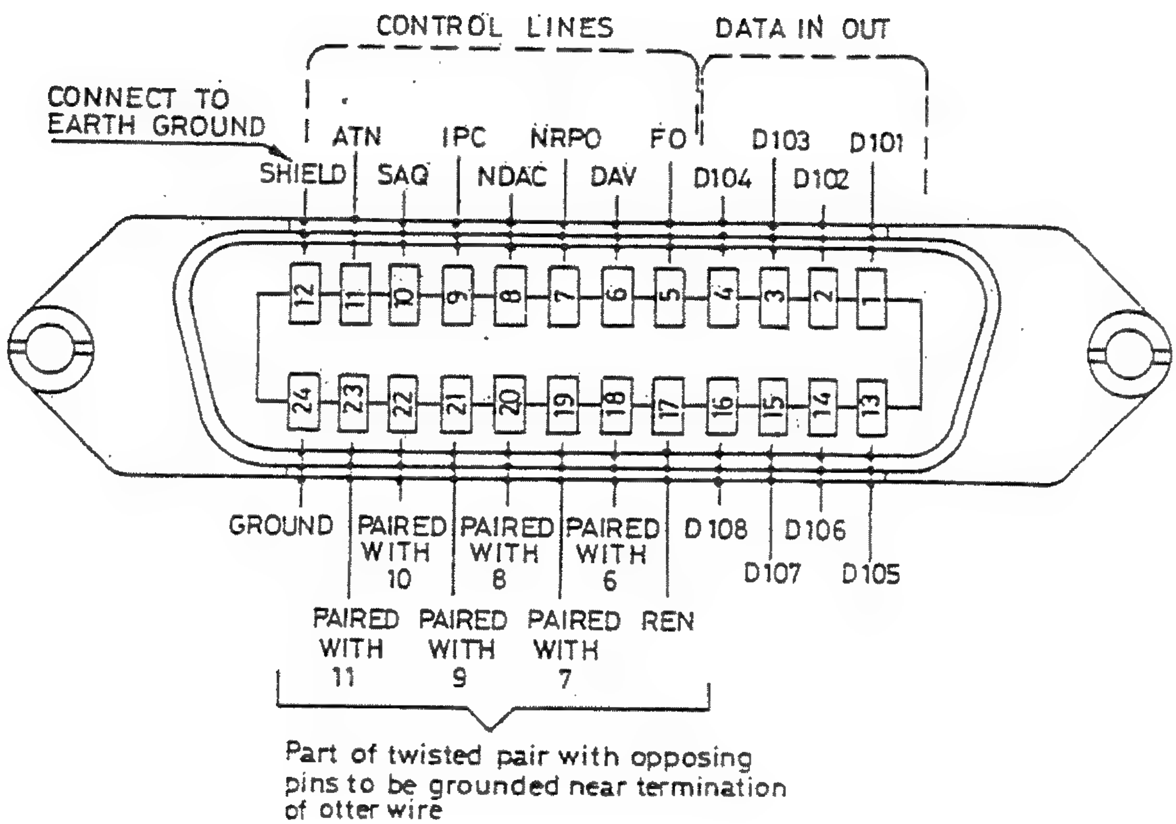
Title	Function	Fixed	Free	Cable	Connector
	Line power	9400-9B	9400-9A	4	12 brown
	Line power	9400-9B	F.P. Sw	4	4 spade
	DC power	9400-9A	9400-2	3	3 brown
	DC power	9400-9A	9400-1	6	6 brown
	Ground link	9400-9B	9400-1	1 black	1 spade
	50 Hz+battery	9400-9B	9400-1	7 black	12 2-row
	CRT services	9400-7	9400-2	7	8 1-row
H3	X deflection	Yoke	9400-2	2 rd/blu	3 1-row
H3	Y deflection	Yoke	9400-2	2 yl/grn	3 1-row
H4	GPIB data	Back	9400-1	ribbon	26 2-row
H5	GPIB data	Back	9400-1	ribbon	16 2-row
	RS232 comms	Back	9400-1	8 color	8 2-row
	RS232 plotter	Back	9400-1	8 color	8 2-row

The following list is of cables which are anchored at both ends.

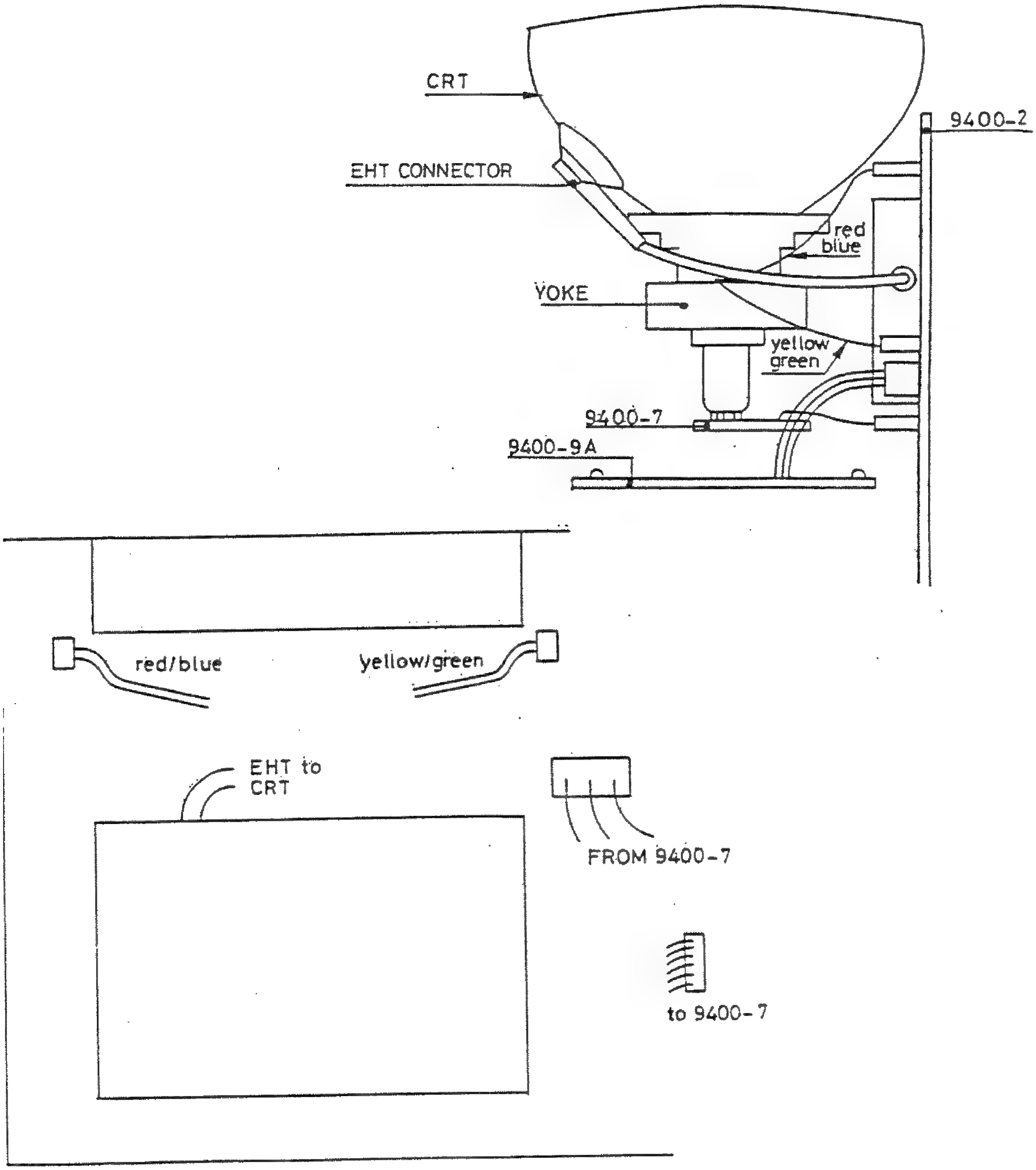
Title	Function	From	To	Cable
	Battery current	Battery	9400-9B	4 wires



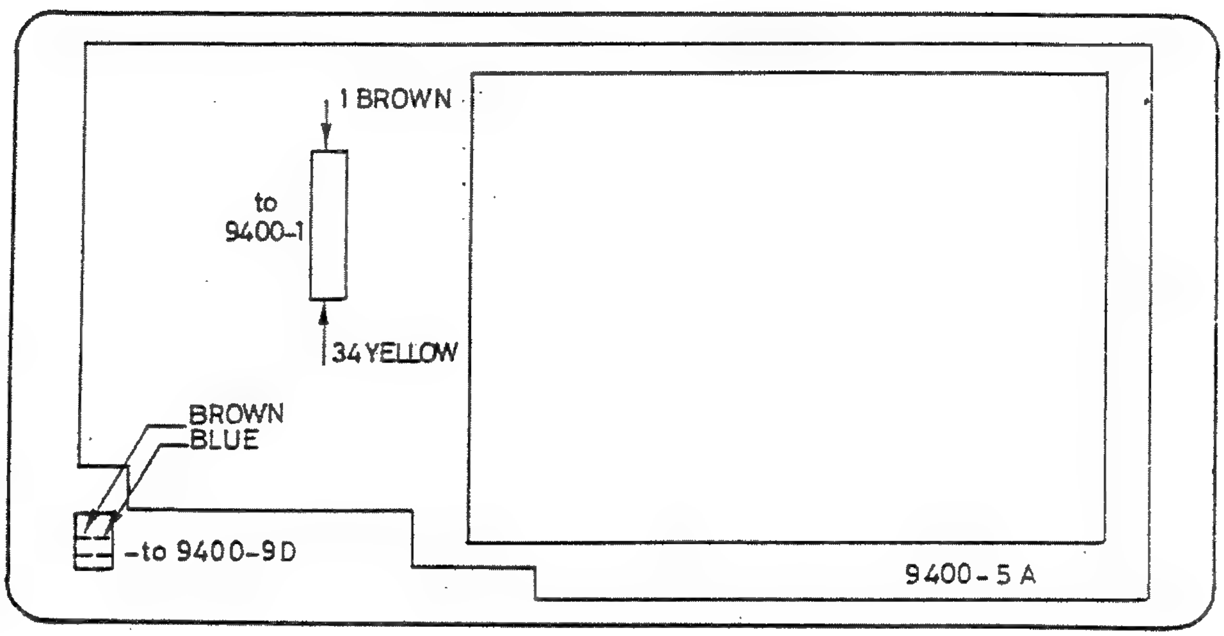
RS232-C INTERFACE



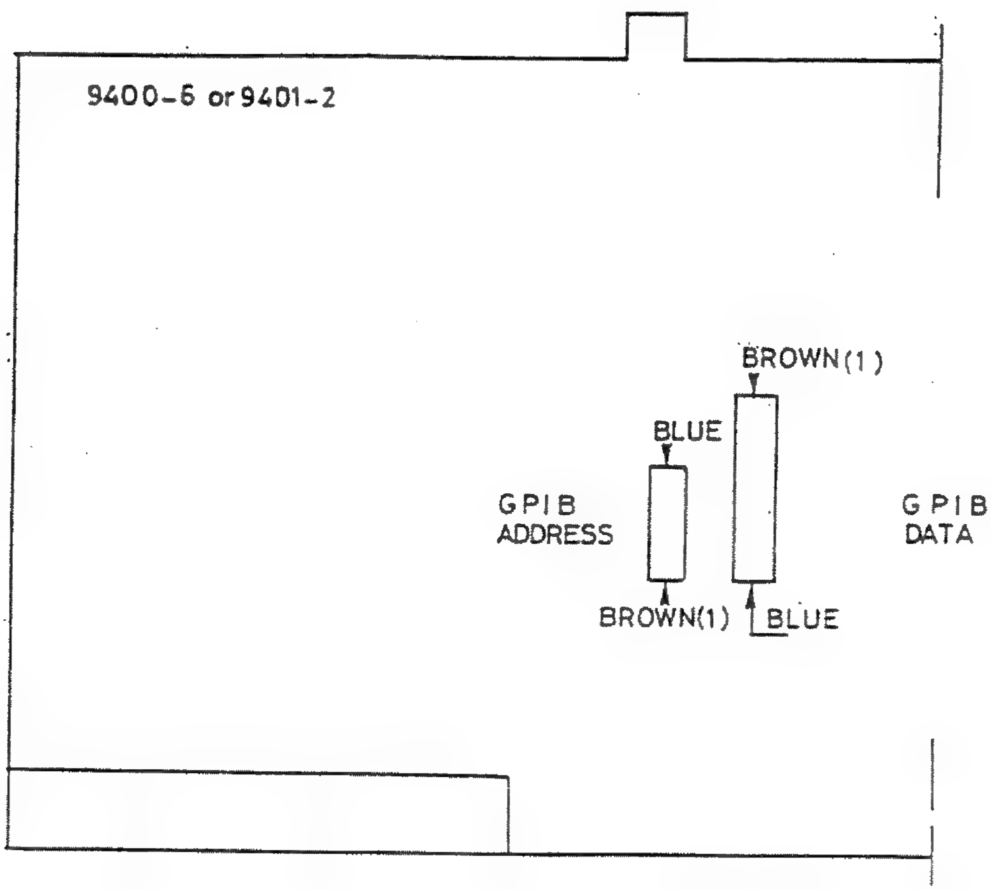
GPIB / IEEE-488 INTERFACE



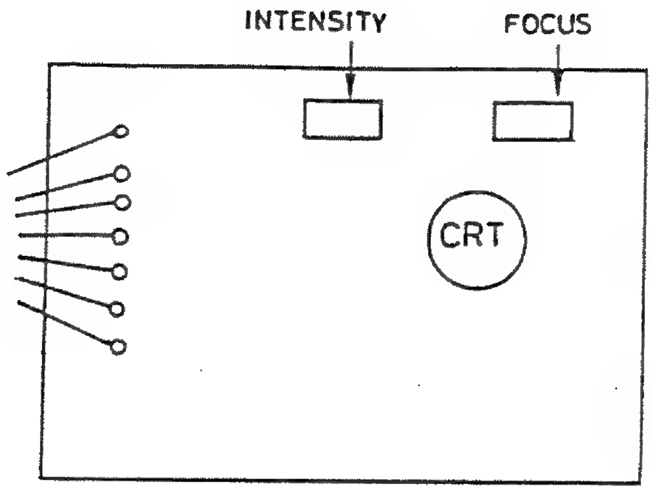
9400-2 DISPLAY BOARD



9400-5 FRONT PANEL BOARD



9400-6 AND 9401-2 GPIB BOARD



9400-7 CRT BOARD

Connections in order:

600 V
60 V
+15 V
-15 V
Z
ZC

CHAPTER 5

ASSEMBLY AND DISASSEMBLY

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CHAPTER 5

ASSEMBLY AND DISASSEMBLY

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WARNING

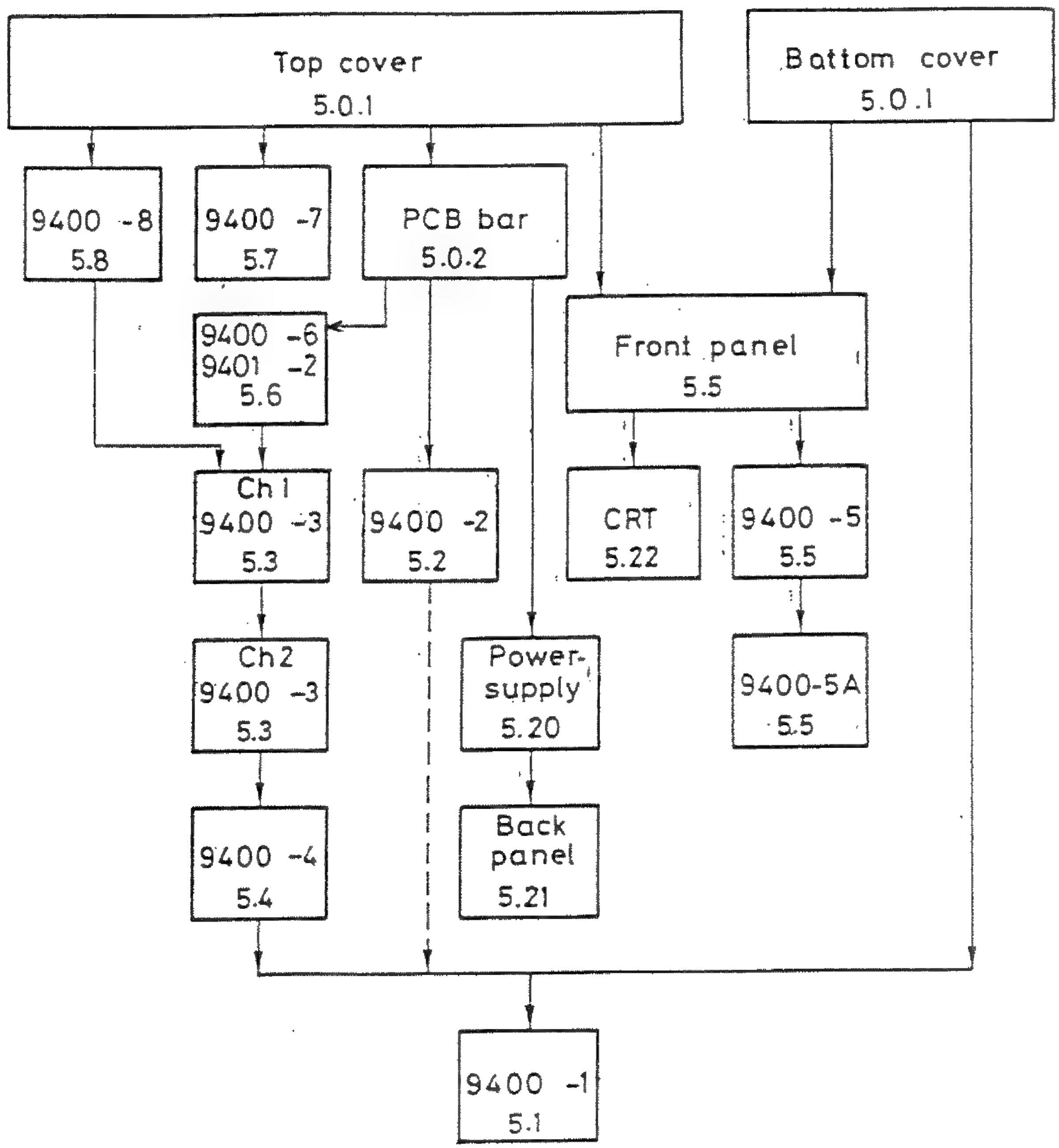
Before removing any parts from the LeCroy 9400 DSO be sure to read carefully the instructions referring to those parts, noting any precautions needed to avoid problems caused by mechanical behavior, static electricity, high voltage supplies, etc.

The 9400 DSO is built in a proprietary case which provides a sturdy mechanical support and electromagnetic screening, as well as providing good access to the boards.

Some parts are fitted with springs, while others, such as the PCB retaining bar, <5.0.2> may be slightly stressed. In either case, care is needed while disassembling, because screws, nuts, washers or springs which get lost in the DSO can be hard to retrieve.

ASSEMBLY and DISASSEMBLY

Disassembly procedure. Any board can be removed only if any items higher in the diagram, and connected by a solid line, are already out. The reassembly procedure is the inverse of the disassembly procedure.



5.0.1 Removal of Covers

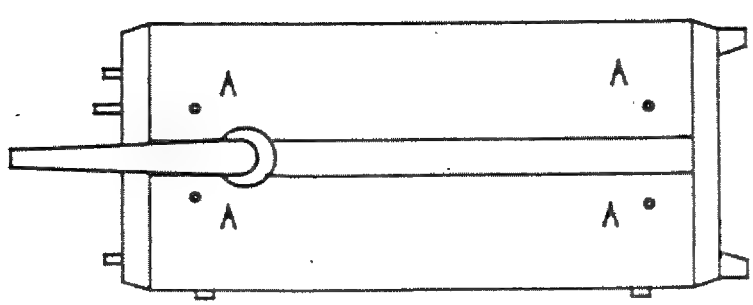
The top and bottom covers are each secured by four plated screws, <5.0.1.A> for which a suitable large driver is needed. To remove the bottom cover turn the handle to the forward position <5.0.1>. In removing and storing the covers and when working on the DSO care should be taken to avoid any chance of chipping the external paintwork. Removal of the bottom cover gives access to the 9400-1 mother board, while removal of the top cover gives access to most of the other boards, except the 9400-9B, which is attached near the bottom of the back panel.

5.0.2 Removal of the PCB Retaining Bar

This bar <5.0.2> holds the 9400-2, 9400-3, 9400-4 and 9400-6 or 9401-2 in place against the lower restraints, and it must be removed if any of these boards is to be removed. In some older DSOs the lugs on the PCBs did not penetrate far enough into the slots in the bar, resulting in a board occasionally slipping out of place. More recent bars have an extra piece rivetted on the underside. In case of trouble a new bar can be ordered, or a local modification could be done. Note that elasticity of the bar can make screws jump into the DSO when loosened. The bar is fixed with four screws and lockwashers. <5.0.2.B> <5.1.3.B>.

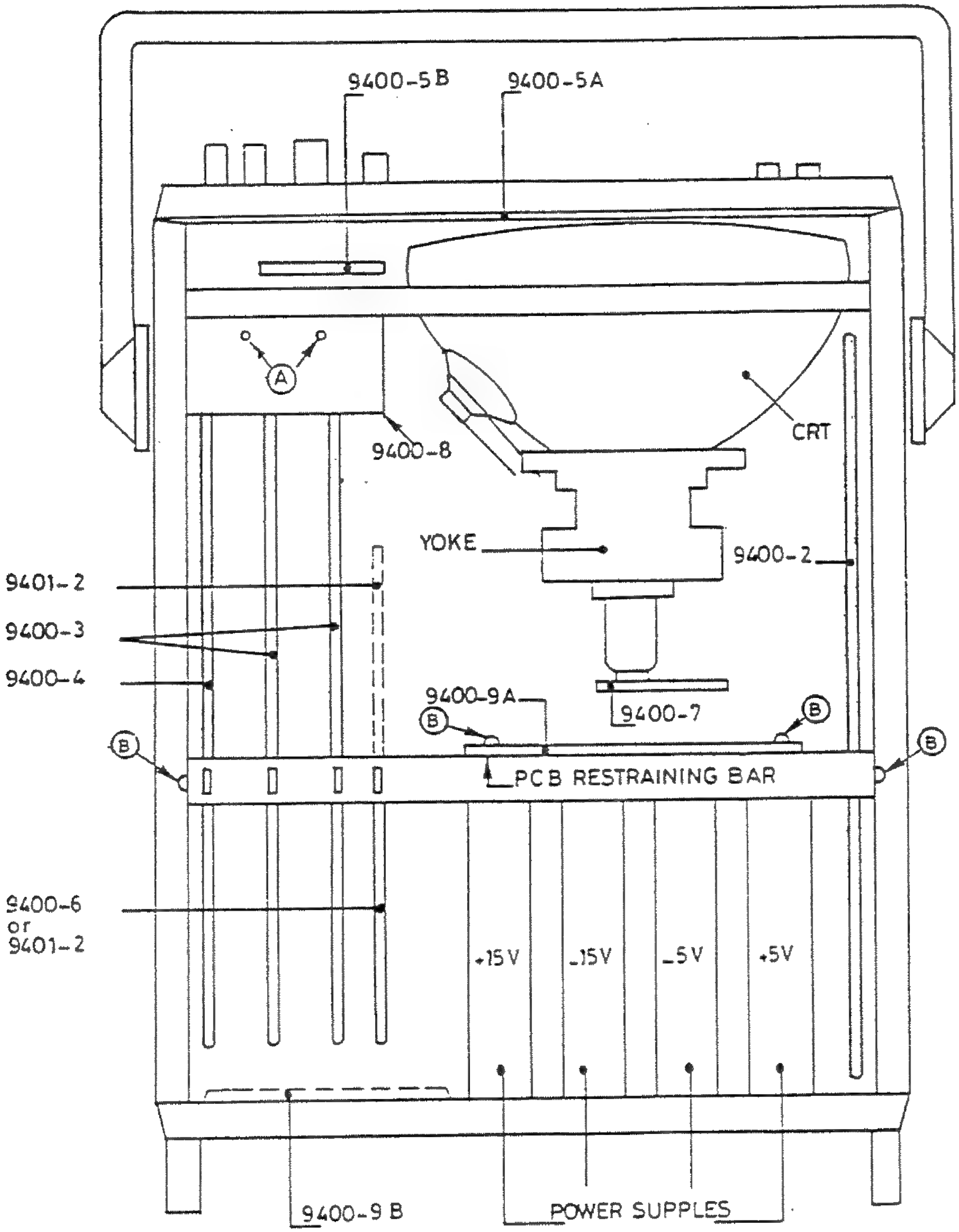
5.0.3 Removal of the Clock Bus Board 9400-8

This is the little board at the front right of the DSO, <5.0.2> across the top of the two ADC boards and the TDC board. It is attached to the top bracket with two screws and lockwashers. <5.0.2.A> Be careful to replace it after any work on the boards, and make sure that the connectors are well aligned before pushing it home.



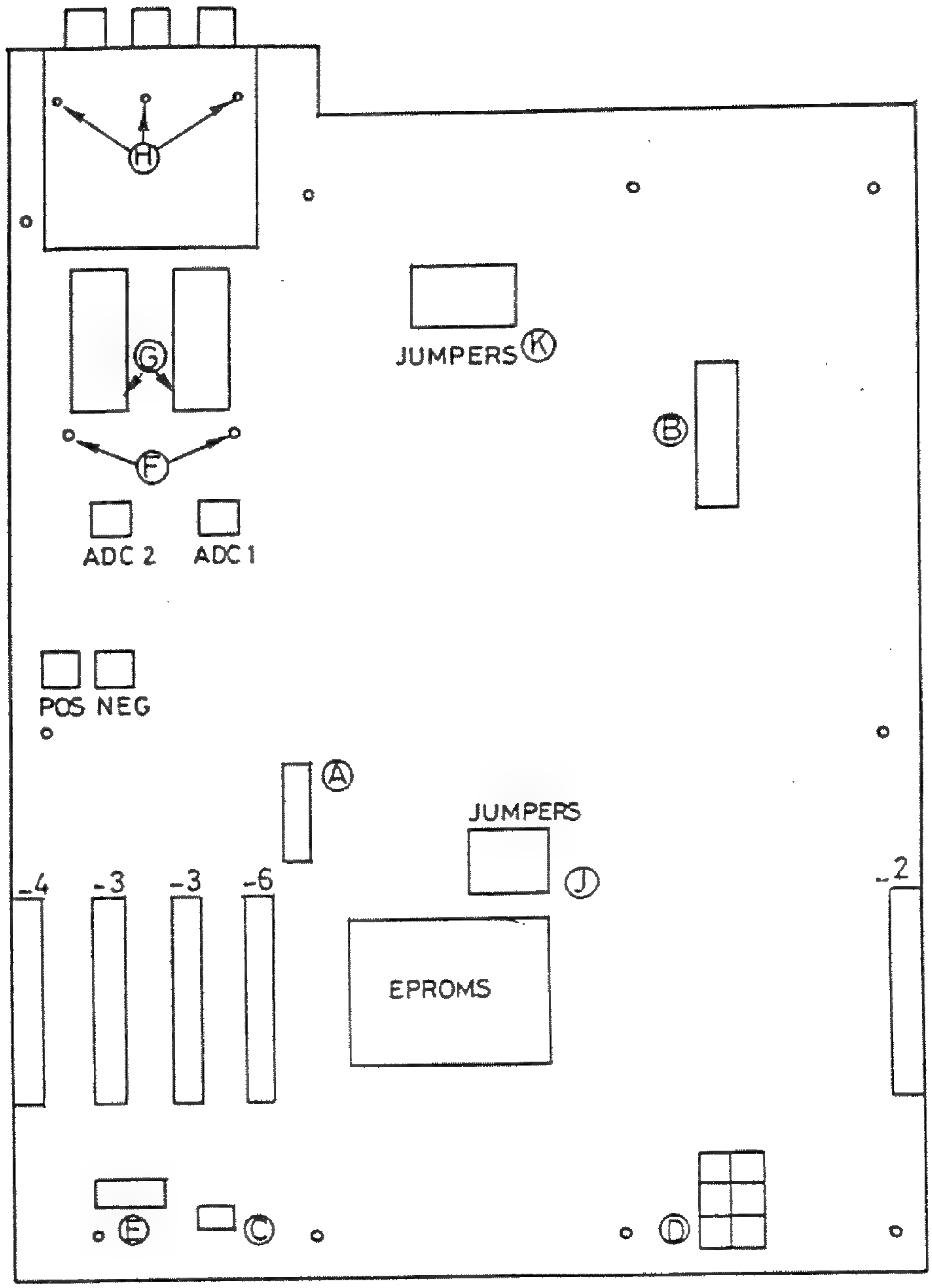
REMOVING THE COVERS FROM THE 9400

Figure 5.0.1



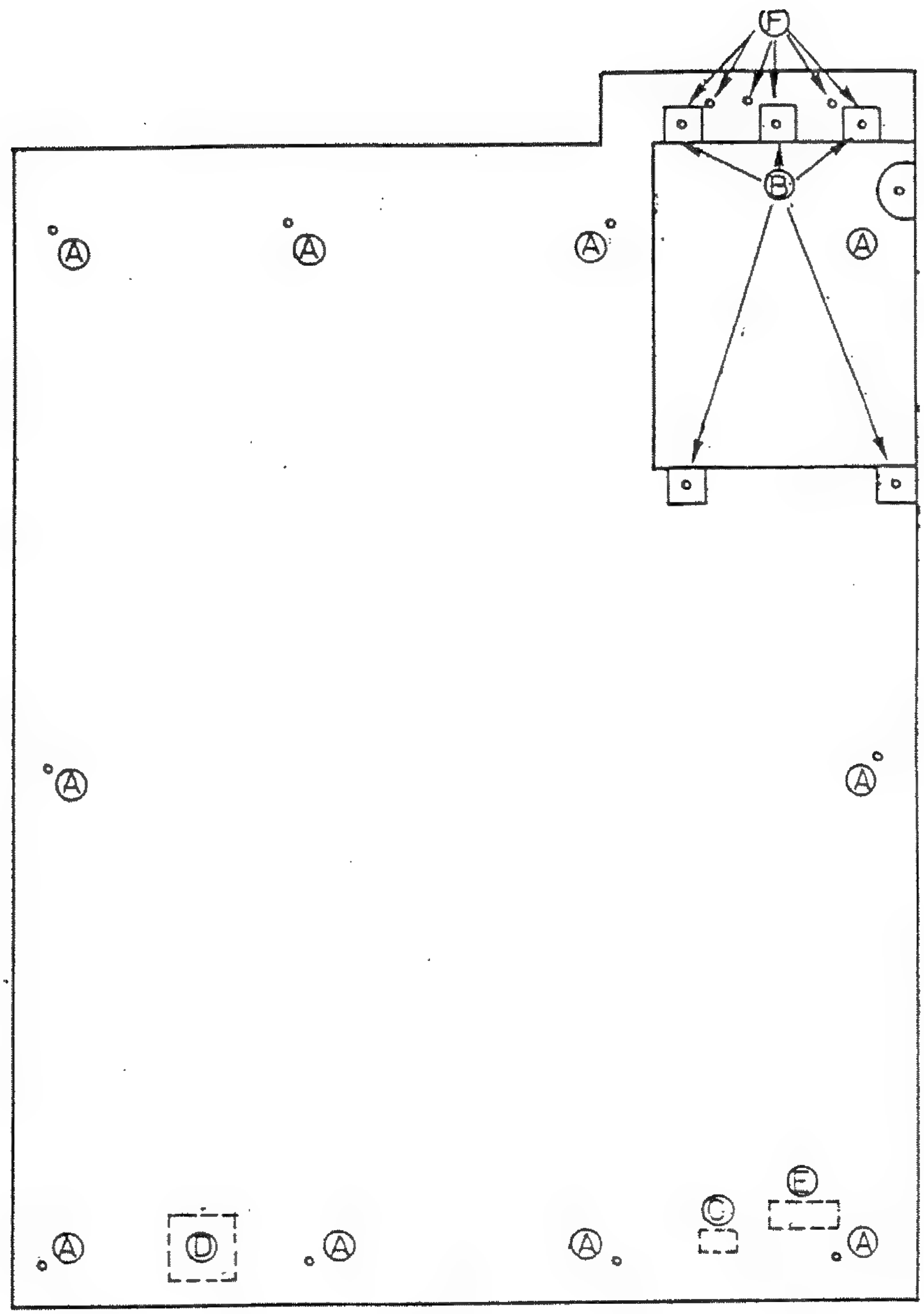
PLAN VIEW OF 9400 INTERIOR SHOWING BOARDS

Figure 5.0.2



TOP VIEW OF 9400-1 MAIN BOARD

Figure 5.1.1

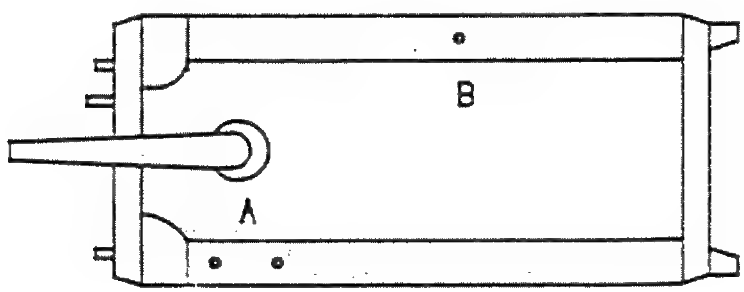


UNDERSIDE VIEW OF 9400-1 MAIN BOARD

Figure 5.1.2

5.1.1 Removal of the 9400-1 Mother Board

In order to remove this board it will be necessary to remove the two covers (5.0.1) and the five boards coupled to the 9400-1, the 9400-2, two 9400-3, 9400-4, and 9400-6 or 9401-2. (5.2, 5.3, 5.4, 5.6 or 5.12) The DSO should be stood on its back panel with the screen at the top. Once the four boards are out, the ten screws, <5.1.2.A> can be removed, followed by the two at the right side of the DSO which hold the frontend heat sink to the case. <5.1.3.A> Next, the heat sink must be removed from the frontend, by removing two screws <5.1.1.F> taking care to retain the two springs and the washers. The springs are needed to maintain good contact between the heat sink and the hybrids. The heat sink can then be removed. Disconnect the RS232 cable <5.1.1.B> and the front panel cable <5.1.1.A> from the top of the 9400-1. Later DSOs do not have springs.



RIGHT SIDE VIEW OF 9400, COVERS OFF

Figure 5.1.3

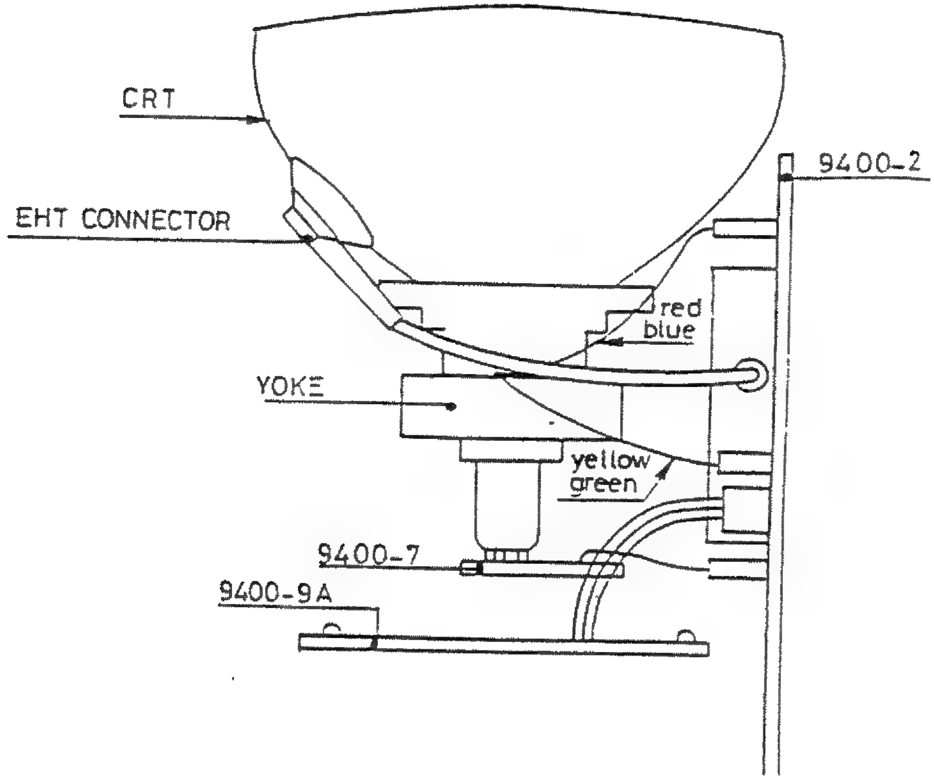
The 9400-1 is now free from the case, but is trapped by the three BNC connectors and the two probe calibrator terminals at the front, and by the power connector at the back. With care, the back of the board can be eased toward the front of the DSO until the power connector just clears the lip of the case, enabling the back edge of the board to be pulled out sufficiently to enable the three cables <5.1.1.C+D+E> at the rear of the board to be disconnected. The board can now be lowered, freeing the three BNC connectors and the calibration terminals from the front panel. With great care, the 9400-1 can be removed without disturbing the 9400-2, but this should be done only by LeCroy personnel who are familiar with the DSO. In such a case replacement needs to be done with care also, to ensure correct alignment of the long connector between the 9400-1 and -2 boards.

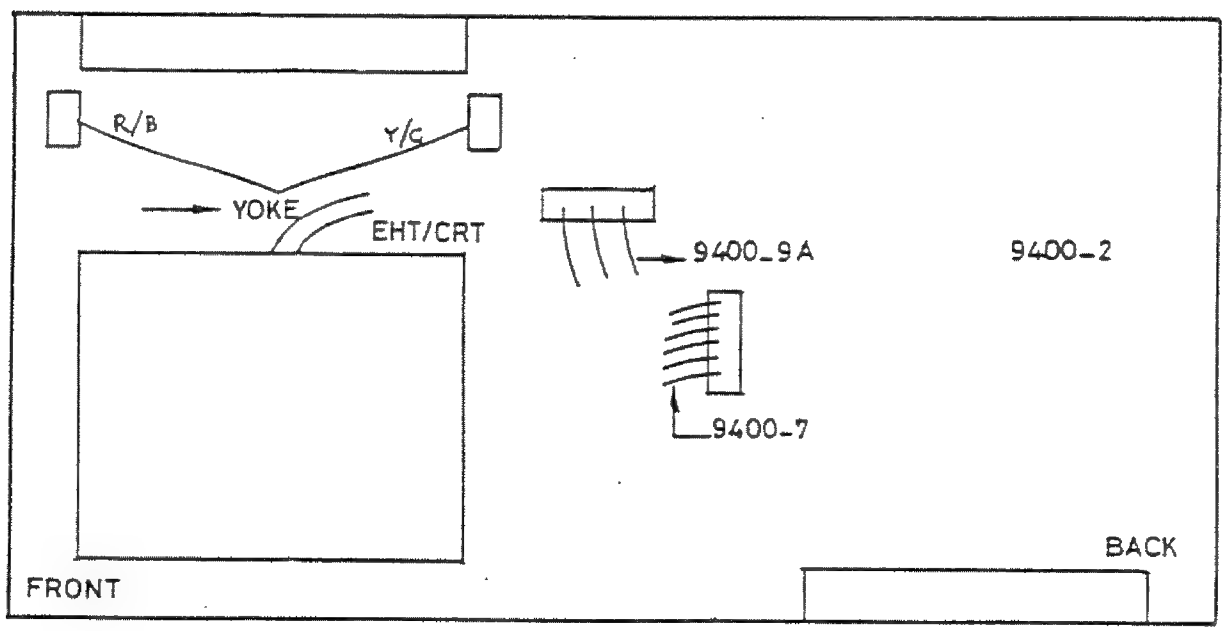
5.1.2 Replacement of the 9400-1 Main Board

The replacement procedure is the reverse of the removal procedure. Stand the DSO on its back. Care should be taken to use a suitable quantity of heat sink compound between the hybrid and sink, and between sink and case. It is very important when installing the heat sink to lift the two frontend hybrids (HVV), almost out of the Berg connectors, so that the heat sink can exert pressure on them when it is replaced.

Replace the RS232-C connector. Offer up the board to the case, and poke the three BNC sockets and the probe calibrator terminals through the holes on the front panel. Then attach the three cables at the back of the board. Next, carefully flex the board enough to lift the large brown connector over the lip of the case. If you left the 9400-2 in place, very carefully push home the 9400-1 so that the connectors mate correctly, remembering that the pins are easy to bend. At this stage you should be able to push the board into its final position and to insert the 10 retaining screws.

At this point the frontend heat sink should be attached. Push it into place and press it down until you can just attach the nuts or screws (depending on the ECO), which hold it to the board. Do not push too far, let the tightening of the nuts do it for you. Finally, screw the heat to the case.





CABLES CONNECTED TO THE 9400-2 BOARD

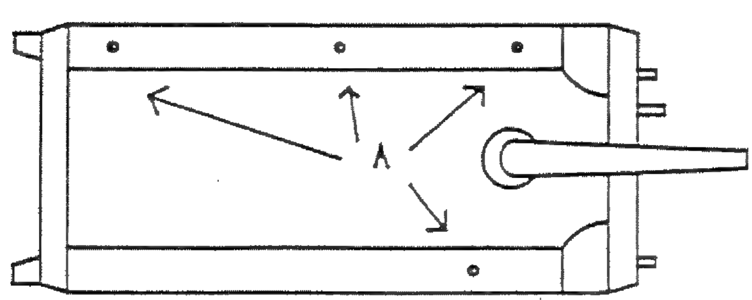
Figure 5.2.1

5.2.1 Removal of the 9400-2 Display Board

The 9400-2 display board is situated along the left side of the DSO. <5.0.2> To remove it, first remove the top cover (5.0.1) and the PCB retaining bar (5.0.2). There are several cables connected to the 9400-2; their positions can be seen in <5.2.1>.

- Remove the two cables which lead to the deflection yoke.
- Remove the cable which leads to the 9400-7 board on the end of the CRT. Take care; this power cable carries 600 volts, with an impedance low enough to cause a very unpleasant electric shock, the effect of which may make you hit some part of the DSO.
- Remove the power cable with the brown connector.
- Remove the EHT plug from the receptacle at the right side of the CRT, taking great care not to touch the metal. On no account allow the free end of the cable to get near any circuits. Touch the free end of the cable to an unpainted part of the case, for at least one second, and repeat until no spark is seen or heard. This ensures that even if the discharge is oscillatory, no significant charge remains. The CRT must be discharged similarly, using a wire or a tool which is first placed on the case, and only then placed on the CRT receptacle. Note that the EHT voltage is 11 kV; a shock at this level can be serious, especially if you have one hand on the chassis and one on the EHT. The usual rule holds good - use one hand only.

The four screws <5.2.2.A> which secure the 9400-2 to the case can now be removed, and the board can now be removed vertically from the DSO, making sure that the EHT cable is kept away from PCBs, as some charge may remain.



LEFT SIDE VIEW OF 9400, COVERS OFF

Figure 5.2.2

5.2.2 Replacement of the 9400-2 Display Board

The procedure is the reverse of the removal procedure. The same precautions against high voltage are needed. It is a good idea again to ensure that both CRT and board are discharged. A convenient ground point on the 9400-2 is the top of the large resistor at the top left of the board, seen from the component side. Before fitting the top two screws, make sure that a suitable amount of heat sink compound is present. It is easier to install the CRT focus/brightness cable if the 9400-7 is first removed from the base of the CRT, and is put back on the CRT after the black plug has been installed on the 9400-7.

5.3.1 Removal of the 9400-3 ADC Boards

The 9400-3 ADC boards are situated parallel to the right side of the DSO. <5.0.2> The left one is for Channel 1; the right for Channel 2. To remove either board requires removal of the PCB retaining bar. (5.0.2) In order to remove ADC board 2 it is necessary to remove ADC board 1 first. The clock bus board, 9400-8, must also be removed. (5.0.3)

Before an ADC board can be taken out, its signal input cable must be removed from the 9400-1, which needs care, as the SMB connector is seated firmly. On no account must the cable itself be pulled. On the back of each ADC board is a rather bulky delay line. Make sure that in lifting out the board that this coil does not foul any parts on the next board to the right, especially the small coaxial cables.

5.3.2 Replacement of the 9400-3 ADC Boards

This is a straightforward reversal of the removal procedure, requiring care in placement of cables and insertion of the card into the large socket at the back of the 9400-1; it is rather easy to bend pins if there is a misalignment. Do not forget to replace the clock bus; without it there will be no results.

5.4.1 Removal of the 9400-4 TDC Board

Removal of this board must be preceded by removal of the PCB restraining bar (5.0.2), 9400-8, (5.8) and both 9400-3 (5.3). The next step is the careful removal of both SMB plugs from the 9400-1, not by pulling the cables, but by pulling the plugs, which can be quite firmly seated. The board can be lifted out vertically. Make sure that while a board is being examined, repaired or stored, the two coaxial cables do not get damaged.

5.4.2 Replacement of 9400-4 TDC Board

The replacement is straight forward, the only requirements being careful alignment of the main connector, and correct connection of the two SMA plugs into the correct sockets. Place the two coaxial cables in a way which will cause the least disturbance when the neighboring ADC board is inserted. The two cables on the 9400-4 board are labeled POS and NEG, and they should be plugged into POS and NEG respectively on the 9400-1. Do not forget the 9400-8 board. If you do not put it back you get no waveforms on the screen.

5.5.1 Removal of the 9400-5 Front Panel Board

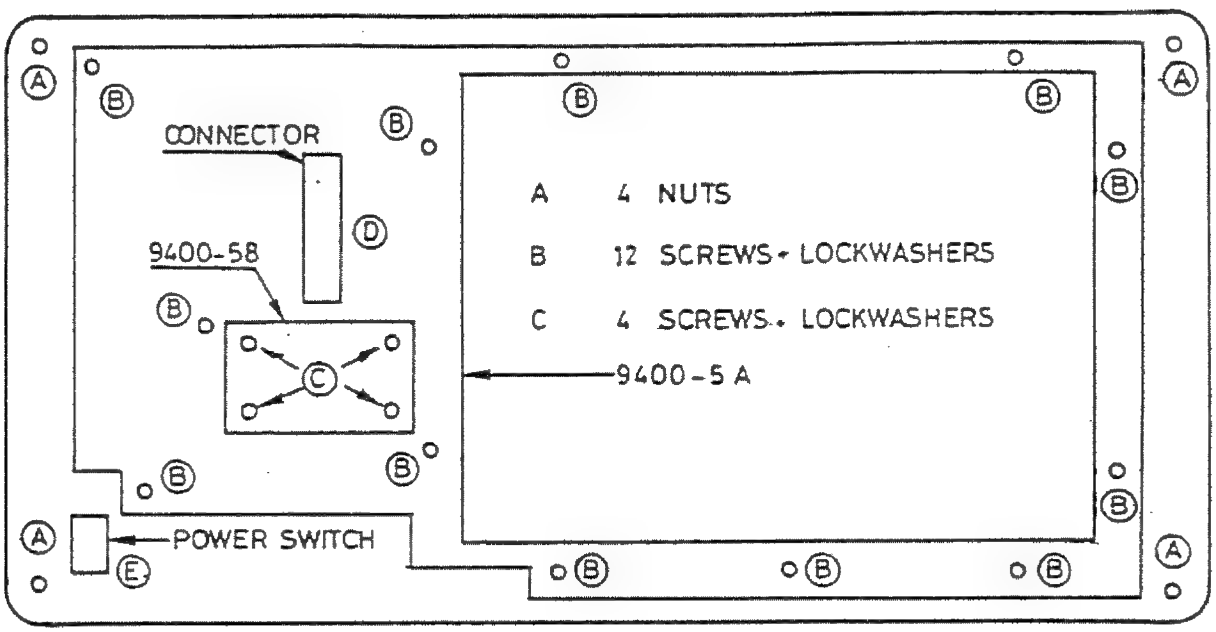
In order to remove this board first remove both covers. (5.0.1) Next remove the ribbon cable from the 9400-5 board. <5.5.1.D> Now remove the four nuts at the corners of the front panel. <5.5.1.A> Remove four spade terminals <5.5.1.E> from the power switch, making sure that they can be put back in the correct positions. The front panel assembly can now be removed from the DSO. If any parts need to be changed on the main front panel board, 9400-5A, they must be separated from the panel. All the rotary knobs must be removed, which means taking off all the caps (careful, soft plastic) and loosening the nuts. Then the twelve screws with lock washers can be removed, <5.5.1.B> which frees the board. Rotary controls are fixed with a nut and washers: push buttons are fixed by soldering the terminals. The plastic parts are easily damaged by heat. When replacing a push button, take great care to achieve good alignment, to avoid sticking when the button is used.

Note that the LEDs are graded before assembly into three colors, to achieve a uniform appearance. The LEDs are yellow, and they are graded into greenish yellow, yellow, and orange-yellow. These are referred to as "green", "yellow" and "orange" for convenience. The replacement should match the rest. If the available replacement does not match, take a single LED from as far from the others as possible, e.g., "REMOTE" or "INTERLEAVED SAMPLING ON", and use it as the replacement. The poorly matching one then becomes the singleton. Never put a poorly matched LED in a group - it will look obviously wrong.

To change the fine gain potentiometers, remove the 9400-5B by undoing the four screws. <5.5.1.C>

5.5.2 Replacement of the 9400-5 Board

The replacement procedure is the reverse of the removal procedure. Take great care when fitting the 9400-5A to the panel that each push button is free to move in and out to the full extent of its travel.



REAR VIEW OF 9400-5 FRONT PANEL BOARD

Figure 5.5.1

5.6.1 Removal of the 9400-6 GPIB board

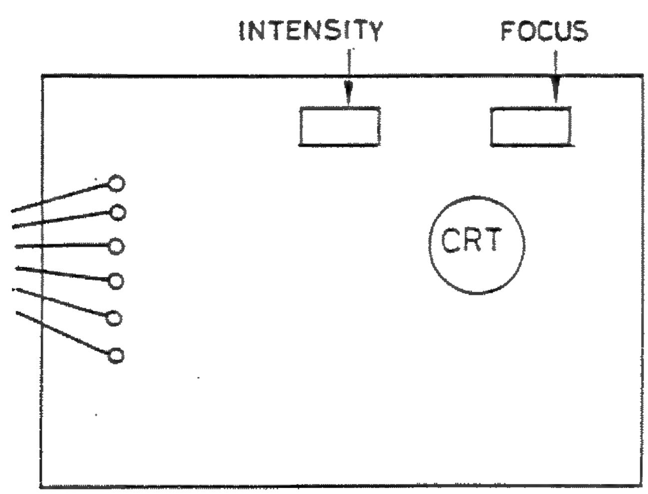
Remove the PCB retaining bar (5.0.2) and then detach the two ribbon cables from the 9400-6 board. They are of different sizes. Note the orientation - they are both color coded. The larger cable has line 1 at the top, while the smaller has line 1 at the bottom. The GPIB board can now be removed. Note that on a few 9400 DSOs the units were supplied with wrongly color coded or wrongly polarized cables. The best procedure is write down the orientation of each cable and to put it back in the original position.

5.6.2 Replacement of the 9400-6 Board

Simply reverse the procedure of 5.6.1.

5.7 Removal and Replacement of the 9400-7 CRT Board

Ease the board carefully towards the back of the DSO, until it is free. Detach its cable from the 9400-2 board. In some cases it may be easier if the power cable from the 9400-9A to the 9400-2 is previously detached.



FRONT VIEW OF 9400-7 CRT BOARD

Figure 5.7.1

5.8 Removal and Replacement of the 9400-8 Clock Bus

This is very simple, requiring only that care be taken in alignment of the connector pins when reassembling the board.

5.9 9400-9A and 9400-9B Power Supply Boards

These two boards cannot be simply removed. For information on the 9400-9A see (5.21) and for 9400-9B see (5.20).

5.12 Removal and Replacement of 9401-2 GPIB and Memory Board

This board is fitted in later 9400 DSOs in the position previously occupied by the 9400-6 GPIB board. The procedures for the 9401-6 are the same as for the 9400-B. (5.6)

5.20 Removal of the Low Voltage Power Supplies

5.20.1 Removal of the Block of Four

The four main DC power supplies of the 9400 DSO are situated on the left side of the back panel, and behind the 9400-9A board. <5.0.2> They should be removed only as a block of four, after which they can be dealt with individually as required.

Remove the line power cable from the 9400-9A, noting its position. Remove the power cable from the 9400-2, <5.2.1> so that it is connected only to the 9400-9A. There is still one cable connected to the 9400-9A on the other side, but it cannot yet be moved.

Remove the lower set of four countersunk screws <5.21.1.A> from the back panel, and the outer two upper screws <5.21.1.B>. Now, holding the front of the 9400-9A and the block of power supplies very carefully, so that they do not hit the CRT or the 9400-1 board, remove the last two screws <5.21.1.C> from the back panel. It should now be possible to lift the power supplies up enough to reach underneath and pull out the power connector from the 9400-1. <5.1.1.D> The power supply block is now completely free from the 9400 DSO.

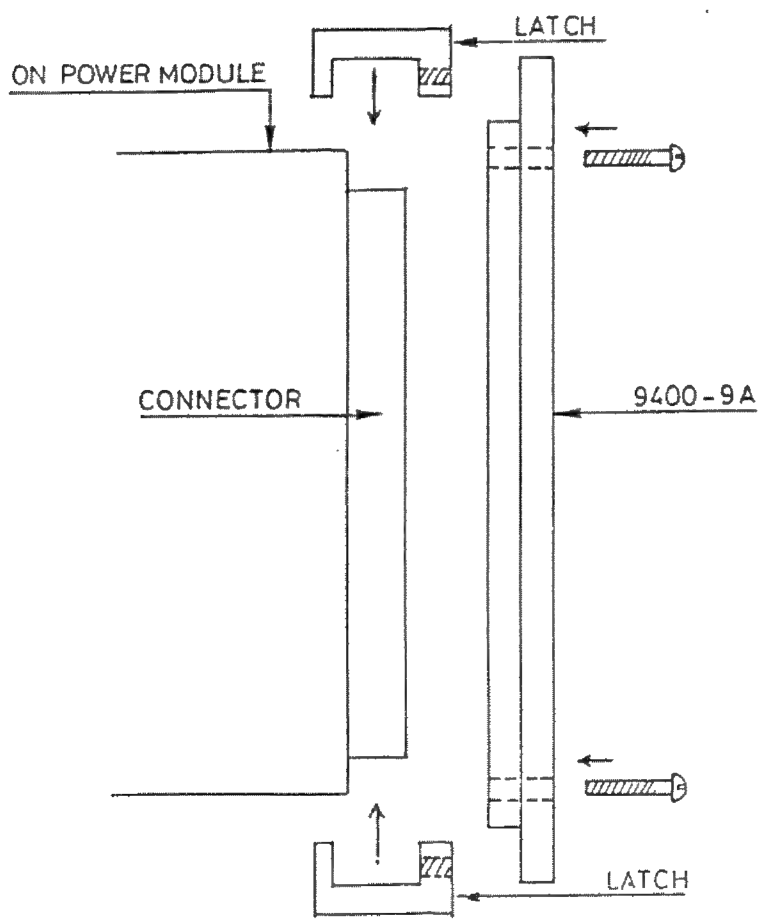
5.20.2 Replacement of Power Supplies

Simply reverse the procedure of 5.20.1.

5.20.3 Removing an Individual Power Supply

Remove the block of power supplies (5.20.1).

Each power supply is held to the 9400-9A by two latches, <5.20.1>, which can be released by taking out the two screws.



REMOVING ONE POWER SUPPLY

Figure 5.20.1

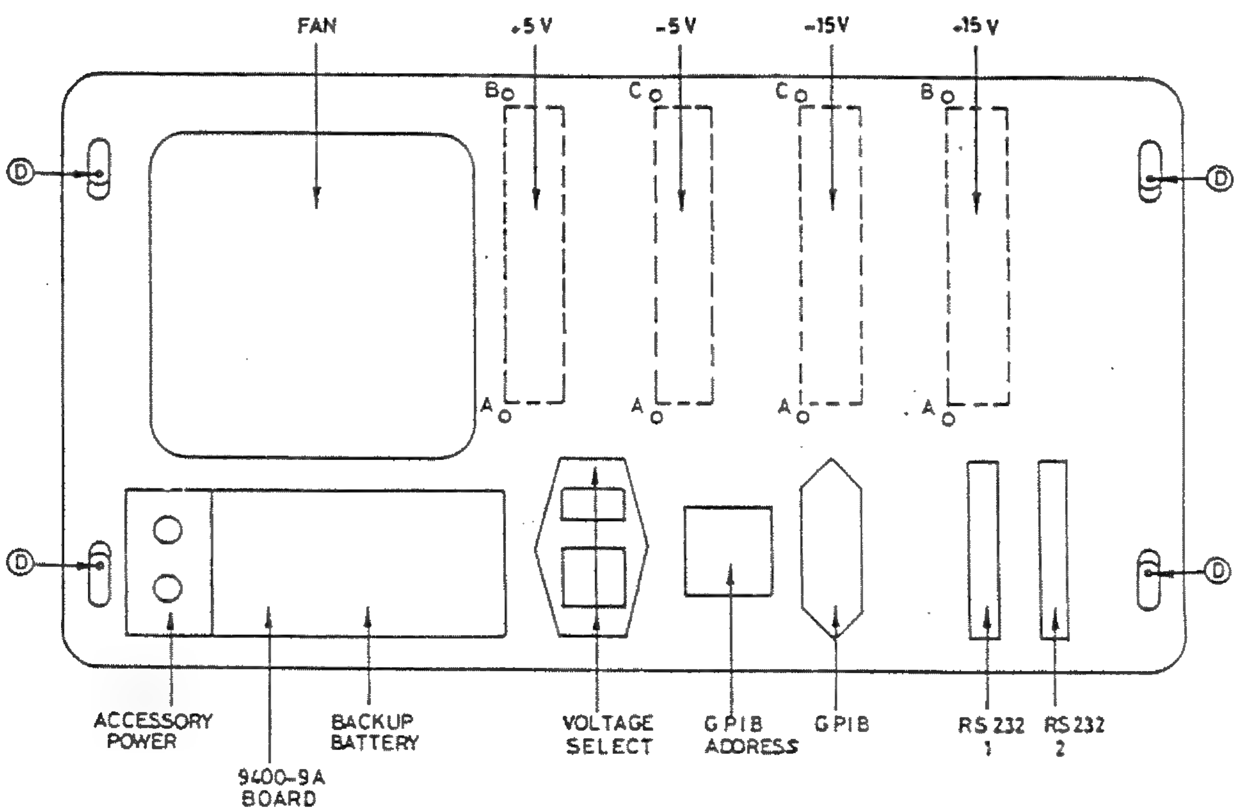
5.21 Removing the Back Panel

This can be done without removing the block of low voltage power supplies, but because of the constraint caused by the power cable to the front panel, it is difficult.

Remove the power supplies (5.20). Remove the cables connecting the back panel to the 9400-1:

- RS232 <5.1.1B>
- groundlink <5.1.1.C>
- AC link <5.1.1.E>
- GPIB <5.6.1.A> <5.6.1.B>

Remove the four screws running through the black feet at the corners of the back panel <5.21.1.D>. Remembering that there is a power cable connecting the back panel to the case at the lower left corner, as viewed from the back, ease out the back panel from the case.



BACK PANEL

Figure 5.21.1

When exchanging individual power modules it may be found that the new unit has no nuts on the rear flange for attachment to the back panel. In such a case the two nuts should be removed from the recesses in the old unit an placed carefully into the new unit. The nuts have a tendency to fall inside the power unit. Difficulty may be experienced in inserting the nuts because of fouling by the nuts which hold the cover on the power module. In such a case rotate the screw and nut to minimize the interference. The nuts should be held in the recesses with Loctite, nail varnish, or quick drying paint. When the block of power supplies is reassembled to the back panel, the eight screws <5.21.1.ABC> should be inserted gingerly to avoid pushing out the nuts from their sockets.

When attempting to insert the small black latches which hold the power modules to the 9400-9A some interference may be found from a green/yellow wire or a ceramic capacitor. In both cases the offending item may be moved aside with care.

5.22.1 Removal of Cathode Ray Tube

Remove the following:

- (5.0.1) Top cover of 9400
- (5.0.2) PCB retaining bar
- (5.7) 9400-7 CRT board
- (5.2.1) 9400-2 display board
- (5.5.1) 9400-5 front panel assembly

At this stage the cathode ray tube should have been discharged, but a final check just before removal can do no harm.

The tube can now, with care, be removed without any other boards having to be moved. Take off the long helical grounding spring which runs diagonally across the back of the bulb. With a suitable nut driver, remove the nut at each corner of the tube at the front of the frame. Make sure the stud and nut at the back are not lost in the DSO. Hold the CRT very carefully as the the studs are withdrawn, or place soft padding under it. Withdraw the CRT forward out of the frame.

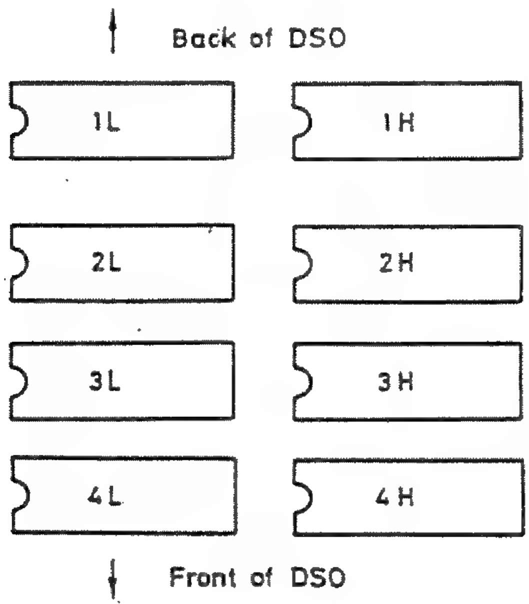
5.22.2 Replacement of Cathode Ray Tube

Before fitting a new tube, it is well to connect the EHT receptacle to the conductive coating, in case a charge has built up.

This proceeds exactly as the removal process in reverse. The fitting of the grounding spring, under the neck, away from the EHT lead, is essential, to prevent the outer conductive coating acquiring charge and then discharging to the logic circuits. The coating also forms the ground electrode of a smoothing capacitor.

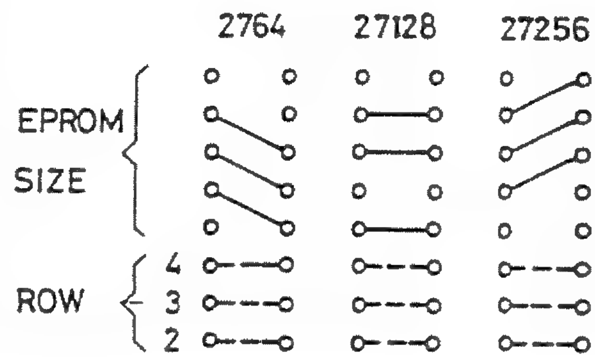
5.23 Changing EPROMs

These are on the top side of the 9400-1 board, and access is possible only by removing the power supply block (5.20). The EPROM positions and jumpers are shown in <5.23.1> and <5.23.2>. The EPROMs can be removed using an IC extractor. The usual precautions against static electricity are required. The EPROMs can be 64, 128, or 256 K types. The diagram shows how to jumper each type.



EPROM Positions

Figure 5.23.1



EPROM Jumpers

Figure 5.23.2

CHAPTER 6

PARTS LISTS FOR THE 9400 AND 9400A

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 1
FINISHED GOODS-MANUFACTURED
PART: 9400A/G
DESC: FINAL ASSEMBLY 9400A/G UOM: EA SC: M REV: A

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	EFFECTIV DATE	INACTIVE DATE	REFERENCE INFORMATION
M9400	LOOSE PARTS M9400		1	R	EA	1.00	1.000	00/00/00	99/99/99	
F9400-1	COMPLETED BOARD F9400-1		2	R	EA	1.00	1.000	00/00/00	99/99/99	
F9400-2	COMPLETED BOARD F9400-2	A	3	R	EA	1.00	1.000	00/00/00	99/99/99	
V9400-3A	VARIANT SUB'Y V9400-3A		4	R	EA	2.00	1.000	00/00/00	99/99/99	
V9400-4	VARIANT SUB'Y V9400-4		5	R	EA	1.00	1.000	00/00/00	99/99/99	
F9400A-51	COMPLETED BOARD F9400A-51		6	R	EA	1.00	1.000	00/00/00	99/99/99	
F9400-7	COMPLETED BOARD F9400-7		7	R	EA	1.00	1.000	00/00/00	99/99/99	
F9400-8	COMPLETED BOARD F9400-8		8	R	EA	1.00	1.000	00/00/00	99/99/99	
F9400-9/115V	COMPLETED BOARD F9400-9/115V		9	R	EA	0.60	1.000	00/00/00	99/99/99	
F9400-9/220V	COMPLETED BOARD F9400-9/220V		10	R	EA	0.40	1.000	00/00/00	99/99/99	
F9401-2	COMPLETED BOARD F9401-2		11	R	EA	0.25	1.000	00/00/00	99/99/99	
F9401-2/1	COMPLETED BOARD F9401-2/1		12	R	EA	0.75	1.000	00/00/00	99/99/99	
9400AMS02A	FINAL ASSEMBLY MS02A		13	R	EA	1.00	1.000	00/00/00	99/99/99	
9400AMS02B	FINAL ASSEMBLY MS02B	B	14	R	EA	1.00	1.000	00/00/00	99/99/99	
ACCESSORIES-9400A	ACCESSORIES FOR 9400A		15	R	EA	1.00	1.000	00/00/00	99/99/99	

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SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: M9400
DESC: LOOSE PARTS M9400 UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
1234567890123456789012345											
321220009	CRT ORANGE 90 DEG DEFL 9'		1	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
377051005	LABEL 'DANGER-------ONLY'	A	2	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
411261001	SWITCH ROCKER DPST		3	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
485000060	GROMMET 4.8MM ID/10.2 OD		4	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
512021867	BRACKET RIGHT ANGLE SMALL		5	B	EA	2.00	1.000	10	0	00/00/00	99/99/99
530010024	FOOT FOR COMPAC ENCLOSURE		6	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
530301005	HANDLE (U-SHAPE)		7	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
530410001	CARD GUIDE NON METALLIC		8	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
544310001	SPRING EXT TYPE 190 MM		9	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
550430104	SCREW CYL HD PHIL M3X4		10	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
550430106	SCREW CYL HD PHIL M3X6		11	P	EA	16.00	1.000	10	0	00/00/00	99/99/99
550430108	SCREW CYL HD PHIL M3X8		12	P	EA	9.00	1.000	10	0	00/00/00	99/99/99
550430114	SCREW CYL HD PHIL M3X14		13	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
550440108	SCREW CYL HD PHIL M4X8		14	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
550440110	SCREW CYL HD PHIL M4X10		15	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
550440416	CYL INT HEX M4X16		16	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
550440640	SCREW OVAL HD PHIL M4X40		17	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
550440708	SCREW LARGE HEAD M4X8		18	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
550450108	SCREW CYL HD PHIL M5X8		19	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
551430300	WASHER SHAKEPROOF M3		20	P	EA	26.00	1.000	10	0	00/00/00	99/99/99
551430301	WASHER SHAKEPROOF LGE M3		21	P	EA	9.00	1.000	10	0	00/00/00	99/99/99
551440300	WASHER SHAKEPROOF M4		22	P	EA	12.00	1.000	10	0	00/00/00	99/99/99
551440301	WASHER SHAKEPROOF LGE M4		23	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
551440501	WASHER FLAT (SPRING) M4		24	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
551450300	WASHER SHAKEPROOF M5		25	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
552430300	NUT OPEN-END ACORN M3		26	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
552440100	NUT HEX M4		27	P	EA	12.00	1.000	10	0	00/00/00	99/99/99
552450400	NUT SHAKEPROOF HEX M5		28	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
553230112	SPACER HEX M3X12MM		29	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
554040901	NUT GUIDE FOR 554440101		30	P	EA	12.00	1.000	10	0	00/00/00	99/99/99
554440101	NUT SQUARE M4		31	P	EA	12.00	1.000	10	0	00/00/00	99/99/99
554440201	GND WASHER FOR 554440101		32	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
554440202	FLAT WASHER M4		33	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
594120003	TIEWRAP		34	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
709400000	DSO COMPLETED BOX		35	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400005	DISPLAY SUPPORT 9400		36	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400011	MOTHER CARD SUPPORT		37	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400041	SUPPORT ANGLE BRACKET		38	B	EA	2.00	1.000	10	0	00/00/00	99/99/99
709400061	POWER SUPPLY SUPPORT		39	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400065	SPRING CONTACT		40	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400071	REAR PANEL FOOT	A	41	B	EA	4.00	1.000	10	0	00/00/00	99/99/99
709400151	HEAT SINK FOR HVV 200		42	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709450071	NEOPRENE WASHER	A	43	B	EA	4.00	1.000	10	0	00/00/00	99/99/99
780161135	FRONT PANEL CABLE		44	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
300090001	DEFLECTION YOKE		46	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
455020001	CONNECTOR PIN (FEMALE)		47	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
455121003	CONNECTOR HOUSING 3		48	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
455950002	CLAMP WITH STRAIN RELIEF		49	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
594120003	TIEWRAP		50	P	EA	2.00	1.000	0	0	02/05/89	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-1
DESC: COMPLETED BOARD F9400-1   UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
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102412022	CAP CERA DISC 100V 2.2 PF		1	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412056	CAP CERA DISC 100V 5.6 PF		2	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412082	CAP CERA DISC 100V 8.2 PF		3	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412100	CAP CERA DISC 100V 10 PF		4	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412101	CAP CERA DISC 100V 100PF		5	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
102412120	CAP CERA DISC 100V 12 PF		6	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412150	CAP CERA DISC 100V 15 PF		7	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412180	CAP CERA DISC 100V 18 PF		9	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
102412181	CAP CERA DISC 100V 180 PF		10	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412220	CAP CERA DISC 100V 22 PF		11	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
102412330	CAP CERA DISC 100V 33PF		12	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412390	CAP CERA DISC 100V 39 PF		13	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412560	CAP CERA DISC 100V 56 PF		14	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
102484471	CAP CERA DISC 100V 470 PF		15	P	EA	9.00	1.000	10	0	00/00/00	99/99/99
102534472	CAP CERA DISC .0047 UF		16	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
103307103	CAP CERA MONO 50V .01 UF		19	P	EA	170.00	1.000	10	0	00/00/00	99/99/99
103317222	CAP CERA MONO 50V 2200 PF		20	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103327102	CAP CERA MONO 50V .001 UF		22	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
103427104	CAP CERA MONO 100V .1 UF		24	P	EA	65.00	1.000	10	0	00/00/00	99/99/99
103506331	CAP CERA MONO 100V 330 PF		25	P	EA	12.00	1.000	10	0	00/00/00	99/99/99
103896222	CAP CERA MONO 200V 2200PF		26	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
124171203	CAP POLYSTYRENE .02 UF		28	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
124236223	CAP POLYESTER FILM .022UF		29	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
142214156	CAP TANT DIP CASE 15 UF		31	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
142424225	CAP TANT DIP CASE 2.2 UF		32	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
142824685	CAP TANT DIP CASE 6.8 UF		34	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
146354107	CAP MINI ALUM 20% 100 UF		36	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
146424106	CAP MINI ALUM 20% 10 UF		37	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
146554476	CAP MINI ALUM 20% 47 UF		39	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
146634106	CAP MINI ALUM 20% 10 UF		40	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
147634102	CAP MINI ALUM 20% 1000 UF		41	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
158849009	CAP VARIABLE .5 - 2.5 PF		42	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
158849010	CAP VARIABLE 1 - 5 PF		43	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
158849011	CAP VARIABLE 2.5 - 10 PF		44	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
158849012	CAP VARIABLE 5.0-15 PF		45	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225100	RES COMP 1/8W 5% 10 OHMS		46	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225101	RES COMP 1/8W 5% 100 OHMS		48	P	EA	15.00	1.000	10	0	00/00/00	99/99/99
161225102	RES 1/8W 5% 1K		49	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
161225103	RES COMP 1/8W 5% 10 K		51	P	EA	10.00	1.000	10	0	00/00/00	99/99/99
161225105	RES CARBON FILM 1 MEG		52	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161225132	RES CARBON FILM 1.3 K		53	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225150	RES COMP 1/8W 5% 15 OHMS		54	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
161225152	RES COMP 1/8W 5% 1.5 K		55	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
161225153	RES COMP 1/8W 5% 15 K		56	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225162	RES CARBON FILM 1.6 K		57	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225181	RES COMP 1/8W 5% 180 OHMS		58	P	EA	16.00	1.000	10	0	00/00/00	99/99/99
161225221	RES COMP 1/8W 5% 220 OHMS		59	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225243	RES COMP 1/8W 5% 24 K		60	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161225302	RES COMP 1/8W 5% 3 K		61	P	EA	1.00	1.000	10	0	00/00/00	99/99/99

INDENTED BILL OF MATERIALS

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-1
DESC: COMPLETED BOARD F9400-1 UOM: EA SC: R REV:

1234567890123456789012345

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
161225330	RES COMP 1/8W 5% 33 OHMS		62	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161225390	RES COMP 1/8W 5% 39 OHMS		63	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225471	RES COMP 1/8W 5% 470 OHMS		64	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161225510	RES COMP 1/8W 5% 51 OHMS		65	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
161225560	RES COMP 1/8W 5% 56 OHMS		66	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161225561	RES COMP 1/8W 5% 560 OHMS		67	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225751	RES COMP 1/8W 5% 750 OHMS		68	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335102	RES COMP 1/4W 5% 1 K		70	P	EA	36.00	1.000	10	0	00/00/00	99/99/99
161335103	RES COMP 1/4W 5% 10 K		71	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335105	RES COMP 1/4W 5% 1 MEG		72	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335106	RES COMP 1/4W 5% 10 MEG		74	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
161335124	RES COMP 1/4W 5% 120 K		75	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335131	RES COMP 1/4W 5% 130 OHMS		76	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335132	RES COMP 1/4W 5% 1.3 K		77	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335155	RES COMP 1/4W 5% 1.5 MEG		78	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335181	RES COMP 1/4W 5% 180 OHMS		79	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335200	RES COMP 1/4W 5% 20 OHMS		80	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335222	RES COMP 1/4W 5% 2.2 K		81	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335224	RES COMP 1/4W 5% 220 K		82	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335241	RES COMP 1/4W 5% 240 OHMS		83	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335272	RES COMP 1/4W 5% 2.7 K		85	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161335273	RES COMP 1/4W 5% 27 K		86	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335301	RES COMP 1/4W 5% 300 OHMS		87	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335303	RES COMP 1/4W 5% 30 K		88	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335331	RES COMP 1/4W 5% 330 OHMS		90	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161335391	RES COMP 1/4W 5% 390 OHMS		91	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335392	RES COMP 1/4W 5% 3.9 K		92	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335395	RES COMP 1/4W 5% 3.9 MEG		93	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335471	RES COMP 1/4W 5% 470 OHMS		94	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335472	RES COMP 1/4W 5% 4.7 K		95	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161335473	RES COMP 1/4W 5% 47 K		97	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335511	RES COMP 1/4W 5% 510 OHMS		99	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335512	RES COMP 1/4W 5% 5.1 K		101	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
161335514	RES COMP 1/4W 5% 510 K		102	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335561	RES COMP 1/4W 5% 560 OHMS		103	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161335562	RES COMP 1/4W 5% 5.6 K		104	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161335683	RES COMP 1/4W 5% 68 K		106	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161335754	RES COMP 1/4W 5% 750 K		107	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335913	RES COMP 1/4W 5% 91 K		109	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
165245180	RES 5% METAL FILM 18 OHMS		111	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
168009389	RES PREC MPR 24 909 OHMS		112	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
168009493	RES PREC MPR24 11K		113	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
168009585	RES PREC MPR24 100K		115	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
168009681	RES PREC MPR 24 1 MEG		116	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
168531277	RES PREC RN55D 61.9 OHMS		117	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531297	RES PREC RN55D 100 OHMS		118	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
168531325	RES PREC RN55D 196 OHMS		119	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
168531389	RES PREC RN55D 909 OHMS		120	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
168531401	RES PREC RN55D 1.21 K		121	P	EA	1.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-1
DESC: COMPLETED BOARD F9400-1 UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	ST SC	UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
1234567890123456789012345											
168531405	RES PREC RN55D 1.33 K		122	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531417	RES PREC RN55D 1.78 K		123	P	EA	10.00	1.000	10	0	00/00/00	99/99/99
168531422	RES PREC RN55D 2.00 K		124	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
168531439	RES PREC RN55D 3.01 K		125	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
168531489	RES PREC RN55D 10.0 K		126	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531509	RES PREC RN55D 16.2 K		127	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531541	RES PREC RN55D 34.8 K		128	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
168531565	RES PREC RN55D 61.9K		129	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
168531567	RES PREC RN55D 64.9 K		130	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
168531609	RES PREC RN55D 178 K		131	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
168531664	RES PREC RN55D 665 K		132	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
169416473	RESISTOR DISC NTC 47 K		133	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
179227502	RES VARI CERMET 5K		134	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
181437103	RES VARI CERMET 10 K		135	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
181437105	RES VARI CERMET 1 MEG		136	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
181437201	RES VARI CERMET 200 OHMS		137	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
181437501	RES VARI CERMET 500 OHMS		138	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
181447104	RES VARI CERMET 100 K		139	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
190042331	RESISTOR NETWORK 330 OHMS		140	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
190642102	RESISTOR NETWORK 1 K		141	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190642222	RESISTOR NETWORK 2.2 K		142	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
190842102	RES NETWORK 1 K		143	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
200012001	IC QUAD LINE REC MC 1489L		144	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200012002	IC QUAD LINE DR MC 1488L		146	P	EA	7.00	1.000	10	0	00/00/00	99/99/99
200031028	IC 2-IN NAND GT SN74LS00N		147	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
200031046	IC HEX INVERTER SN74LS04N		148	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200031047	IC 3-IN NAND GT SN74LS10N		149	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031048	IC 4-IN NAND GT SN74LS20N		150	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031049	IC FLIP-FLOP SN74LS74N		151	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
200031051	IC 2-IN NOR GT SN74LS02N		152	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200031055	IC SHIFT REG SN74LS164N		153	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
200031066	IC POS NAND GT SN74LS132N		154	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031073	IC 2-IN POS OR SN74LS32N		156	P	EA	7.00	1.000	10	0	00/00/00	99/99/99
200031074	IC POS-NAND BUF SN74LS37N		157	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031086	IC 2-IN AND GAT SN74LS08N		159	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
200031089	IC BUS BUFFER SN74LS125N		159	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
200031097	IC COUNTER SN74LS197N		160	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031101	IC BINARY CNTR SN74LS393N		161	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
200031106	IC 2-IN EXCL-OR SN74LS86N		162	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041033	IC D FLIP-FLOP SN74LS174N		163	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041042	IC UP/DN COUNT SN74LS191N		164	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200041044	IC MULTIVIBR SN74LS123N		165	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200041056	IC 8 BIT S REG SN74LS165N		166	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041062	IC DEC/DEMULTP SN74LS138N		167	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041067	IC PRIOR ENCOD SN74LS148N		168	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041068	IC MULTIPLEXER SN74LS158N		169	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200041070	IC DAT SEL/MP SN74LS257AN		170	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
200041139	IC DEC/MULTIPL SN74LS139N		171	P	EA	[illegible]	1.000	10	0	00/00/00	99/99/99
200071001	IC 8 X BUFFER SN74LS240		172	P	EA	[illegible]	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

ASS CODE: 2
BASSEMBLIES
RT: F9400-1
SC: COMPLETED BOARD F9400-1 UOM: EA SC: R REV:

MPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
2345678901234567890123456											
0071003	IC 8-BIT REGIST SN74LS374		173	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
0071007	IC OCTAL BUFF SN74LS244N		174	P	EA	7.00	1.000	10	0	00/00/00	99/99/99
0071245	IC BUS XCEIVER SN74LS245N		175	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
0071299	IC 8-BIT S/REG SN74LS299N		176	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
0071373	IC 8XLATCH D-TYPE 74LS373		177	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
0071534	IC OCTAL D-TYP FF 74LS534		178	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
0072966	IC 8X DYN MEM DRIV AM2966		179	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
0330000	IC 2-INPUT NAND 74F00		180	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0340074	IC D-TYPE POS FLOP 74F74		181	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0340117	IC DUAL OR-AND MC10H117		182	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0340138	IC 1-OF-8 DECODER 74F138		183	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0340379	IC QUAD D-FLOP 74F379		184	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0341175	IC D-TYPE FLOP 74F175		185	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0440191	IC UP/DN BIN COUNT 74F191		186	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
0440221	IC DUAL MULTIVIBR 74LS221		187	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0540014	IC MULTIPLIER 25LS14		188	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
0570684	IC 8BIT MAGN COMP 74LS684		189	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
5241264	IC65, 536-BIT RAM 4164-15		190	P	EA	16.00	1.000	10	0	00/00/00	99/99/99
5280116	IC 2048X8 RAM HM6116LP-2		191	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
5370256	IC UV E-PROM 27256G-25		192	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
7280800	IC 12-BIT D/A CONV DAC800		193	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
7340399	IC 2-IN MPLX SN74LS399N		194	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
7340508	IC 8-CH ANALOG MPLX DG508		195	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8011004	IC TIMER NE555		196	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8011008	IC VOLT COMPARATOR LM311N		197	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8031010	IC QUAD DIFF COMP LM339N		198	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8033001	IC TRANS ARRAY CA3046		199	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8041001	IC 8-BIT DAC MONODAC-08EQ		200	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8110007	IC LO OFFSET OP AMP OP-07		201	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
8110353	IC DUAL OP AMP LF353N		202	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8122337	IC ADJ -VOLT REG LM337T		203	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8130324	IC QUAD OP AMP LM324		204	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8131347	IC QUAD OP AMP LF347BN		205	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
8570317	IC POS VOLT REGUL LM317		206	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8591320	IC NEG VOLT REG LM320		207	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8591340	IC POS VOLT REG LM340		208	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8740321	IC X-TAL CONTR OSC74LS321		209	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
27391068	IC MICROPROCESSOR 68000L8		210	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
27762661	IC MICROPROC INTERF 2661		211	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
30020062	DIODE SWITCHING BAW62		213	P	EA	38.00	1.000	10	0	00/00/00	99/99/99
30040005	DIODE DUAL PICO-AMP DPAD5		214	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
30110005	DIODE SWITCHING 1N4448		216	P	EA	39.00	1.000	10	0	00/00/00	99/99/99
30150045	DIODE PICOAMPERE BAV 45		217	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
35010005	DIODE RECTIFIER 1N4005		218	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
40225703	DIODE ZENER 3.45V 1N703A		220	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
40225710	DIODE ZENER 6.8V 1N710A		221	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
40225713	DIODE ZENER 9.1V 1N713A		222	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
53010811	DIODE SCHOTTKY FAR HP2811		223	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
53010835	DIODE HOT CARRIER HP2835		224	P	EA	15.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-1
DESC: COMPLETED BOARD F9400-1 UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
1234567890123456789012345-----------	------------------------------	--	-----	--	--	----------	-----	-----	-------	--------	--------
256233209	DIODE LED (RED) TIL209A		225	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
270110003	TRANSISTOR NPN 2N2222A		226	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
270130401	TRANSISTOR NPN A401		227	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
270170001	TRANSISTOR NPN 2N5770		229	P	EA	10.00	1.000	10	0	00/00/00	99/99/99
270170002	TRANSISTOR NPN 2N5962		230	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
275110001	TRANSISTOR PNP 2N2907A		231	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
275170002	TRANSISTOR PNP 2N5771		233	P	EA	17.00	1.000	10	0	00/00/00	99/99/99
275170003	TRANSISTOR PNP A441		234	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
280170104	TRANSISTOR FET N VN0104N3		235	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
300010001	BEAD SHIELDING FERRITE		237	P	EA	33.00	1.000	10	0	00/00/00	99/99/99
300050001	CHOKE FERRITE SINGLE LEAD		239	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
301016103	INDUCTOR MOLDED 10 UH		240	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
301016104	INDUCTOR MOLDED 100 UH		241	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
301016471	INDUCTOR MOLDED .47 UH		242	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
310060491	CRYSTAL 4.915200 MHZ		243	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
310060800	CRYSTAL 8.000000 MHZ		244	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
400331016	SOCKET IC ST DIP-16		245	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
400360028	SOCKET IC ST DIP-28		246	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
400900116	PROGRAM PLUG "191" DIP-16		247	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
401343014	SOCKET IC WW 3-WRAP DIP14		248	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
402610002	CONN CO-AX PC MTG SMB		249	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
403950002	POLARIZING KEY		250	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
405749002	TAB PC MTG 4.8 X .8 MM		251	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
405760005	SOCKET SPRING SINGLE WIRE		252	P	EA	98.00	1.000	10	0	00/00/00	99/99/99
408063005	W-W PIN, ONE SIDE, 1 WRAP		253	P	EA	16.00	1.000	10	0	00/00/00	99/99/99
430540732	RELAY 2 FORM C 5V DPDT		254	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
454110020	HDR SOLD TAIL/MALE PIN 20		255	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454111012	HDR SOLD TAIL/MALE PIN 12		256	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454211034	HDR SOLD TAIL TO MALE 34		257	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454220032	HDR DIP SOLD TO FEM 32		258	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454310002	HDR DIP SOLD TO PC BD 2		260	P	EA	11.00	1.000	10	0	00/00/00	99/99/99
454320096	HDR DIP SOLD TO FEM 96		261	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
454902001	KEYING PLUG (SNAP IN) BLK		262	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
455221006	BLOC FOR CRIMP FEM PINS 6		263	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
500110001	TRANSIPAD "SMALL"		264	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
550430106	SCREW CYL HD PHIL M3X6		266	P	EA	13.00	1.000	10	0	00/00/00	99/99/99
550430108	SCREW CYL HD PHIL M3X8		267	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
551430300	WASHER SHAKEPROOF M3		268	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
551430400	WASHER SHAKEPROOF M3		269	P	EA	17.00	1.000	10	0	00/00/00	99/99/99
552430100	NUT HEX M3		271	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
553230108	SPACER HEX M3X8MM		272	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
585252236	RIVET HOLLOW 2.5X6MM		273	P	EA	10.00	1.000	10	0	00/00/00	99/99/99
590551028	WIRE TEFL 7-STRAND GRN 28		274	P	ME	0.04	1.000	10	0	00/00/00	99/99/99
709400101	CALIBRATION TERMINAL		275	B	EA	2.00	1.000	10	0	00/00/00	99/99/99
709400121	BNC CONN. ANGLE SOCKET		276	B	EA	3.00	1.000	10	0	00/00/00	99/99/99
709400131	UPPER RF-SHIELD		277	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400141	LOWER RF-SHIELD		278	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400143	LOWER RF-SHIELD		279	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400161	SELF FOR 9400-1A		280	B	EA	2.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-1
DESC: COMPLETED BOARD F9400-1 UOM: EA SC: R REV:

COMPONENT PART 1234567890123456789012345	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
709400171	SELF FOR 9400-1A		281	B	EA	2.00	1.000	10	0	00/00/00	99/99/99
709400181	THERMO-COUPLE FOR 9400-1A		282	B	EA	2.00	1.000	10	0	00/00/00	99/99/99
719400103	PC BD PREASS'Y 9400-1A		283	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
719400113	PC BD PREASS'Y 9400-1B		284	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
719400123	PC BD PREASS'Y 9400-1C		285	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
719400133	PC BD PREASS'Y 9400-1D		286	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
719400143	PC BD PREASS'Y 9400-1E		287	B	EA	2.00	1.000	10	0	00/00/00	99/99/99
719400153	PC BD PREASS'Y 9400-1F		288	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
HAB101	HYB BUFFER AMPLIF HAB101		289	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
HVV200	IC VOLTAGE AMPLIF HVV200		290	B	EA	2.00	1.000	10	0	00/00/00	99/99/99
MVL407	IC MONO QUAD DISCR MVL407		291	P	EA	1.00	1.000	10	0	00/00/00	99/99/99

INDENTED BILL OF MATERIALS

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-2
DESC: COMPLETED BOARD F9400-2 UOM: EA SC: R REV: A

COMPONENT PART 1234567890123456789012345	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
102412101	CAP CERA DISC 100V 100PF		1	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412120	CAP CERA DISC 100V 12 PF		2	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
102412270	CAP CERA DISC 100V 27 PF		3	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412470	CAP CERA DISC 100V 47 PF		4	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412560	CAP CERA DISC 100V 56 PF		5	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102940502	CAP CERA DISC 1KV .005 UF		6	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
103307103	CAP CERA MONO 50V .01 UF		7	P	EA	54.00	1.000	10	0	00/00/00	99/99/99
103317222	CAP CERA MONO 50V 2200 PF		8	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103327102	CAP CERA MONO 50V .001 UF		9	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103327224	CAP CERA MONO 50V .22UF		10	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
103427104	CAP CERA MONO 100V .1 UF		11	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
103437334	CAP CERA MONO 100V .33 UF		12	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
103506331	CAP CERA MONO 100V 330 PF		13	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103625221	CAP CERA MONO 100V 220 PF		14	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
116525821	CAP DIP MICA DM15 820 PF		15	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
124461823	CAP POLYSTYRENE .082 UF		16	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
142714685	CAP TANT DIP CASE 6.8UF		17	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
146424106	CAP MINI ALUM 20% 10 UF		18	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
146634106	CAP MINI ALUM 20% 10 UF		19	P	EA	12.00	1.000	10	0	00/00/00	99/99/99
147674102	CAP ALU METAL CAN 1000 UF		20	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161030000	RES COMP ZERO OHM		21	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
161335100	RES COMP 1/4W 5% 10 OHMS		22	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335101	RES COMP 1/4W 5% 100 OHMS		23	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
161335102	RES COMP 1/4W 5% 1 K		24	P	EA	12.00	1.000	10	0	00/00/00	99/99/99
161335103	RES COMP 1/4W 5% 10 K		25	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335104	RES COMP 1/4W 5% 100 K		26	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335105	RES COMP 1/4W 5% 1 MEG		27	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335121	RES COMP 1/4W 5% 120 OHMS		28	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335122	RES COMP 1/4W 5% 1.2 K		29	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
161335132	RES COMP 1/4W 5% 1.3 K		30	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335154	RES COMP 1/4W 5% 150 K		31	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335161	RES COMP 1/4W 5% 160 OHMS		32	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335162	RES COMP 1/4W 5% 1.6 K		33	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335202	RES COMP 1/4W 5% 2 K		34	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
161335221	RES COMP 1/4W 5% 220 OHMS		35	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335223	RES COMP 1/4W 5% 22 K		36	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335224	RES COMP 1/4W 5% 220 K		37	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335241	RES COMP 1/4W 5% 240 OHMS		38	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
161335242	RES COMP 1/4W 5% 2.4 K		39	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335271	RES COMP 1/4W 5% 270 OHMS		40	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335302	RES COMP 1/4W 5% 3 K		41	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335331	RES COMP 1/4W 5% 330 OHMS		42	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335333	RES COMP 1/4W 5% 33 K		43	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335362	RES COMP 1/4W 5% 3.6 K		44	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335431	RES COMP 1/4W 5% 430 OHMS		45	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
161335471	RES COMP 1/4W 5% 470 OHMS		46	P	EA	10.00	1.000	10	0	00/00/00	99/99/99
161335472	RES COMP 1/4W 5% 4.7 K		47	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335511	RES COMP 1/4W 5% 510 OHMS		49	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161335561	RES COMP 1/4W 5% 560 OHMS		50	P	EA	2.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

LASS CODE: 2
JBASSEMBLIES
ART: F9400-2
ESC: COMPLETED BOARD F9400-2 UOM: EA SC: R REV: A

OMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
1335621	RES COMP 1/4W 5% 620 OHMS		51	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
1335622	RES COMP 1/4W 5% 6.2 K		52	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
1335681	RES COMP 1/4W 5% 680 OHMS		53	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
1335682	RES COMP 1/4W 5% 6.8 K		54	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
1335821	RES COMP 1/4W 5% 820 OHMS		55	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
1335912	RES COMP 1/4W 5% 9.1 K		56	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
2805010	RESISTOR WW 5W 1.0 OHM		57	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
8045336	RES HV 33M		58	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8531365	RES PREC RN55D 511 OHMS		59	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
8531372	RES PREC RN55D 604 OHMS		60	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
8531385	RES PREC RN55D 825 OHMS		61	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
8531401	RES PREC RN55D 1.21 K		62	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
8531410	RES PREC RN55D 1.50 K		63	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
8531422	RES PREC RN55D 2.00 K		64	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8531429	RES PREC RN55D 2.37 K		65	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8531433	RES PREC RN55D 2.61 K		66	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
8531439	RES PREC RN55D 3.01 K		67	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
8531447	RES PREC RN55D 3.65 K		68	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8531465	RES PREC RN55D 5.62 K		69	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
8531471	RES PREC RN55D 6.49 K		70	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
8531489	RES PREC RN55D 10.0 K		71	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
8531541	RES PREC RN55D 34.8 K		72	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
2137022	RES WIREWOUND .22 OHMS		73	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
5235005	RES PWR WW 2.5W 5% .5 OHM		74	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
0487103	RES VARI CERMET 10K		75	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
0487501	RES VARI CERMET 500 OHMS		76	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
0487502	RES VARI CERMET 5K		77	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
0042222	RESISTOR NETWORK 2.2 K		78	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
0031028	IC 2-IN NAND GT SN74LS00N		79	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0031047	IC 3-IN NAND GT SN74LS10N		80	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0031049	IC FLIP-FLOP SN74LS74N		81	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
0031051	IC 2-IN NOR GT SN74LS02N		82	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
0031066	IC POS NAND GT SN74LS132N		83	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0031086	IC 2-IN AND GAT SN74LS08N		84	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0041044	IC MULTIVIBR SN74LS123N		85	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0041049	IC QUAD FL-FL SN74LS175N		86	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0041054	IC DATA SELCTR SN74LS153N		87	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0041155	IC DEC/DEMULTIPL 74LS155N		88	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0071003	IC 8-BIT REGIST SN74LS374		89	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
0071534	IC OCTAL D-TYP FF 74LS534		90	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0330000	IC 2-INPUT NAND 74F00		91	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0340074	IC D-TYPE POS FLOP 74F74		92	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0340109	IC J-K FLOP 74F109		93	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0442163	IC 4-BIT COUNTER 74LS163		94	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
0570015	IC SERIAL ADDER AM25LS15		95	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
5381716	IC 16K UV E-PROM 2716-1		96	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
5640096	IC 5-BIT SHIFT REG 74LS96		97	P	EA	9.00	1.000	10	0	00/00/00	99/99/99
7262010	IC 10-BIT D/A CONV DAC-10		98	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
8011005	IC VOLT FOLLOWER LM310N		99	P	EA	2.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-2
DESC: COMPLETED BOARD F9400-2 UOM: EA SC: R REV: A

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
1234567890123456789012345											
208031009	IC VOLT COMPARATOR LM319N		100	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
208041001	IC 8-BIT DAC MONODAC-08EQ		101	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
208041524	IC PULSE WIDTH MODUL 3524		102	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
208110353	IC DUAL OP AMP LF353N		103	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
230110005	DIODE SWITCHING 1N4448		104	P	EA	20.00	1.000	10	0	00/00/00	99/99/99
230150045	DIODE PICOAMPERE BAV 45		105	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
232990641	DIODE ARRAY (HV CASCADE)		106	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
235040060	DIODE RECTIFIER LM60		107	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
235820030	DIODE RECTIFIER EGP30D		108	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
235930816	DIODE RECTIFIER 1A MR816		109	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
240415754	DIODE ZENER 6.8V 1N754A		110	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
240423958	DIODE ZENER 7.5V 1N958B		111	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
240425751	DIODE ZENER 5.1V 1N751A		112	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
240425752	DIODE ZENER 5.6V 1N752A		113	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
253010800	DIODE HOT CARRIER HP2800		114	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
253010835	DIODE HOT CARRIER HP2835		115	P	EA	12.00	1.000	10	0	00/00/00	99/99/99
270170001	TRANSISTOR NPN 2N5770		117	P	EA	21.00	1.000	10	0	00/00/00	99/99/99
270170002	TRANSISTOR NPN 2N5962		118	P	EA	13.00	1.000	10	0	00/00/00	99/99/99
275110001	TRANSISTOR PNP 2N2907A		119	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
275170001	TRANSISTOR PNP 2N5087		120	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
275170002	TRANSISTOR PNP 2N5771		121	P	EA	20.00	1.000	10	0	00/00/00	99/99/99
280190513	TRANSISTOR FET 'N' IRF513		122	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
280190642	TRANSISTOR FET 'N' IRF642		123	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
281190523	TRANSISTOR FET 'P' 9523		124	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
300050001	CHOKE FERRITE SINGLE LEAD		125	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
301016103	INDUCTOR MOLDED 10 UH		126	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
302380480	FILTER CHOKE 2 AMP 48 UH		127	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
377051004	LABEL 'DANGER HI VOLTAGE'		128	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
400000318	SOCKET IC OPEN FRAME 18		129	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
400331016	SOCKET IC ST DIP-16		130	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
400341024	SOCKET IC ST DIP-24		131	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
408063005	W-W PIN, ONE SIDE, 1 WRAP		132	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
429220001	SWITCH THERMAL 1A N.O.		133	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
440290001	TRANSFORMER HV SWITCHING		134	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454110003	HDR SOLD TAIL/MALE PIN 3		135	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
454111008	HDR SOLD TAIL/MALE PIN 8		136	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454121003	BLOC FOR SOCKETS 3-PIN		137	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454310002	HDR DIP SOLD TO PC BD 2		138	P	EA	17.00	1.000	10	0	00/00/00	99/99/99
454311003	HDR DIP SOLDER TO MALE 3		139	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
454312004	HDR MALE PIN TO WW (2X2)4		140	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
454610032	HDR DIP SOLD TO MALE 32		141	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454902001	KEYING PLUG (SNAP IN) BLK		142	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
485011001	GROMMET 10MM OD 5MM ID		143	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
500110001	TRANSIPAD 'SMALL'		144	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
500460005	MOUNTING KIT FOR TO-220		145	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
550430106	SCREW CYL HD PHIL M3X6		146	P	EA	7.00	1.000	10	0	00/00/00	99/99/99
550430108	SCREW CYL HD PHIL M3X8		147	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
550440106	SCREW CYL HD PHIL M4X6		148	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
550440108	SCREW CYL HD PHIL M4X8		149	P	EA	2.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-2
DESC: COMPLETED BOARD F9400-2   UOM: EA SC: R REV: A

COMPONENT PART 1234567890123456789012345	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
551430300	WASHER SHAKEPROOF M3		150	P	EA	11.00	1.000	10	0	00/00/00	99/99/99
551440300	WASHER SHAKEPROOF M4		151	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
552430100	NUT HEX M3		152	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
553230113	SPACER HEX M3X13MM		153	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
554900201	SHOULDER WASHER		154	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
585252354	RIVET HOLLOW 2,5X9MM		155	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
594120003	TIEWRAP		156	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400201	FET SUPPORT BAR 9400-2		158	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400211	UPPER COVER 9400-2		159	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400221	LOWER HV COVER 9400-2		160	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
709400231	HV MULTIPLIER SUPPORT		161	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
719400203	PC BD PREASS'Y 9400-2		162	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
270110003	TRANSISTOR NPN 2N2222A		163	P	EA	7.00	1.000	0	0	12/04/89	99/99/99
161335512	RES COMP 1/4W 5% 5.1 K		164	P	EA	3.00	1.000	0	0	12/04/89	99/99/99
161335332	RES COMP 1/4W 5% 3.3 K		165	P	EA	1.00	1.000	0	0	12/04/89	99/99/99

INDENTED BILL OF MATERIALS

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: V9400-3A
DESC: VARIANT SUB'Y V9400-3A UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
1234567890123456789012345											
F9400-3A	COMPLETED BOARD F9400-3A	A	1	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412100	CAP CERA DISC 100V 10 PF		1	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103307103	CAP CERA MONO 50V .01 UF		2	P	EA	89.00	1.000	10	0	00/00/00	99/99/99
103327102	CAP CERA MONO 50V .001 UF		3	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103427104	CAP CERA MONO 100V .1 UF		4	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
103506331	CAP CERA MONO 100V 330 PF		5	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
142824685	CAP TANT DIP CASE 6.8 UF		6	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
146424106	CAP MINI ALUM 20% 10 UF		7	P	EA	7.00	1.000	10	0	00/00/00	99/99/99
146554476	CAP MINI ALUM 20% 47 UF		8	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
158849009	CAP VARIABLE .5 - 2.5 PF		9	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
158849010	CAP VARIABLE 1 - 5 PF		10	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161225100	RES COMP 1/8W 5% 10 OHMS		11	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225101	RES COMP 1/8W 5% 100 OHMS		12	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161225102	RES 1/8W 5% 1K		13	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161225152	RES COMP 1/8W 5% 1.5 K		14	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
161225161	RES COMP 1/8W 5% 160 OHMS		15	P	EA	17.00	1.000	10	0	00/00/00	99/99/99
161225220	RES COMP 1/8W 5% 22 OHMS		16	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225300	RES COMP 1/8W 5% 30 OHMS		17	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161225331	RES COMP 1/8W 5% 330 OHMS		18	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161225471	RES COMP 1/8W 5% 470 OHMS		19	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161225510	RES COMP 1/8W 5% 51 OHMS		20	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161225621	RES CARBON FILM 620 OHMS		21	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161225680	RES COMP 1/8W 5% 68 OHMS		22	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161225751	RES COMP 1/8W 5% 750 OHMS		23	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161225911	RES CARBON FILM 910 OHMS		24	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335102	RES COMP 1/4W 5% 1 K		25	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335103	RES COMP 1/4W 5% 10 K		26	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335151	RES COMP 1/4W 5% 150 OHMS		27	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335181	RES COMP 1/4W 5% 180 OHMS		28	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335201	RES COMP 1/4W 5% 200 OHMS		29	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335431	RES COMP 1/4W 5% 430 OHMS		30	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335620	RES COMP 1/4W 5% 62 OHMS		31	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161335820	RES COMP 1/4W 5% 82 OHMS		32	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335821	RES COMP 1/4W 5% 820 OHMS		33	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335910	RES COMP 1/4W 5% 91 OHMS		34	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531217	RES PREC RN55D 14.7 OHMS		35	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531281	RES PREC RN55D 68.1 OHMS		36	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531325	RES PREC RN55D 196 OHMS		37	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531357	RES PREC RN55D 422 OHMS		38	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531381	RES PREC RN55D 750 OHMS		39	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531425	RES PREC RN55D 2.15 K		40	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531489	RES PREC RN55D 10.0 K		41	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
179227202	RES VARI CERMET 2K		42	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
181437101	RES VARI CERMET 100 OHMS		43	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
181437102	RES VARI CERMET 1 K		44	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
181437103	RES VARI CERMET 10 K		45	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
181437201	RES VARI CERMET 200 OHMS		46	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
181437501	RES VARI CERMET 500 OHMS		47	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190042151	RESISTOR NETWORK 150 OHMS		48	P	EA	1.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

ASS CODE: 2
BASSEMBLIES
RT: V9400-3A
SC: VARIANT SUB'Y V9400-3A UOM: EA SC: R REV:

MPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
34567890123456789012345-----------	-----------------------------	--	-----	--	--	----------	-----	-----	-------	--------	--------
90042331	RESISTOR NETWORK 330 OHMS		49	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
90042471	RESISTOR NETWORK 470 OHMS		50	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
90642471	RESISTOR NETWORK 470 OHMS		51	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
90842471	RESISTOR NETWORK 470 OHMS		52	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
00031028	IC 2-IN NAND GT SN74LS00N		53	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
00031046	IC HEX INVERTER SN74LS04N		54	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
00031057	IC 3-IN POS NOR SN74LS27N		55	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
00031086	IC 2-IN AND GAT SN74LS08N		56	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
00032010	IC 2-IN NAND BUF 74LS38PC		57	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
00041027	IC QUAD SEL/MP SN74LS157N		58	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
00041062	IC DEC/DEMULTP SN74LS138N		59	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
00071001	IC 8 X BUFFER SN74LS240		60	P	EA	10.00	1.000	10	0	00/00/00	99/99/99
00340117	IC DUAL OR-AND MC10H117		61	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
00340378	IC PARALLEL D REG 74F378		62	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
00344131	IC DUAL D M-S FLOP 10H131		63	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
00344176	IC HEX D M-S FLOP 10H176		64	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
00371374	IC D-TYP FLOP 74F374PC		65	P	EA	14.00	1.000	10	0	00/00/00	99/99/99
04022002	IC HEX D M-S F-F MC10176L		66	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
04042002	IC NOR GATE MC10102P		67	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
04042008	IC QUAD TRANSL MC10125P		68	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
04042011	IC LINE RECEIVER MC10116P		69	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
04042141	IC SHIFT REGISTER MC10141		70	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
04043231	IC TYPE D FLOP MC10231P		71	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
05280316	IC 2KX8 SRAM UM6116-3		72	P	EA	16.00	1.000	10	0	06/04/89	99/99/99
07200200	IC 8-BIT FLASH ADC 77200		73	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
07444116	IC TRIPL LINE RCVR 10H116		74	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
08011356	IC JFET OP AMP LF356A		75	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
08122002	IC VOLT REG POS UA7805		76	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
08124002	IC VOLT REG -5V UA7905UC		77	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
08591320	IC NEG VOLT REG LM320		78	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
08591340	IC POS VOLT REG LM340		79	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
30110005	DIODE SWITCHING 1N4448		80	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
40425750	DIODE ZENER 4.7V 1N750A		81	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
70170001	TRANSISTOR NPN 2N5770		82	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
71170090	TRANSISTOR NPN UHF BFR90		83	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
75030032	TRANSISTOR PNP UHF BFQ32		84	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
75110001	TRANSISTOR PNP 2N2907A		85	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
90140010	DELAY LINE 10 N-SEC		86	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
00010001	BEAD SHIELDING FERRITE		87	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
00050001	CHOKE FERRITE SINGLE LEAD		88	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
05760005	SOCKET SPRING SINGLE WIRE		89	P	EA	24.00	1.000	10	0	00/00/00	99/99/99
05764110	SOCKET SINGLE WIRE 10-POS		90	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
54310002	HDR DIP SOLD TO PC BD 2		91	P	EA	9.00	1.000	10	0	00/00/00	99/99/99
54314016	HDR DIP SOLD TO MALE 16		92	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
54370012	HEADER 2-SIDED FEMALE 12		93	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
54610096	HDR DIP SOLD TO MALE 96		94	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
80033001	CABLE CO-AX 30CM SMB-SMC		95	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
50430106	SCREW CYL HD PHIL M3X6		96	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
51430100	FLAT WASHER M3		97	P	EA	4.00	1.000	10	0	00/00/00	99/99/99

INDENTED BILL OF MATERIALS

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: V9400-3A
DESC: VARIANT SUB'Y V9400-3A   UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
552430100	NUT HEX M3		93	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
585252354	RIVET HOLLOW 2,5X9MM		99	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
719400313	PC BD PREASS'Y 9400-3A		100	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
HSH202	IC SAMPLE & HOLD HSH202		101	B	EA	1.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: V9400-4
DESC: VARIANT SUB'Y V9400-4 UOM: EA SC: R REV:

COMPONENT PART 12345678901234567890123456	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
F9400-4	COMPLETED BOARD F9400-4		1	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412047	CAP CERA DISC 100V 4.7 PF		1	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412056	CAP CERA DISC 100V 5.6 PF		2	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412180	CAP CERA DISC 100V 18 PF		3	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412330	CAP CERA DISC 100V 33PF		4	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
102412820	CAP CERA DISC 100V 82 PF		5	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
103307103	CAP CERA MONO 50V .01 UF		6	P	EA	79.00	1.000	10	0	00/00/00	99/99/99
103427104	CAP CERA MONO 100V .1 UF		7	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
103437334	CAP CERA MONO 100V .33 UF		8	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103506331	CAP CERA MONO 100V 330 PF		9	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
116305181	CAP DIP MICA DM5 180 PF		10	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
146634106	CAP MINI ALUM 20% 10 UF		11	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
158819001	CAP VARI CERA 3.5 - 18 PF		12	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
158880001	CAP VARIABL 2.8-12.5PF		13	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335047	RES COMP 1/4W 5% 4.7 OHMS		14	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335100	RES COMP 1/4W 5% 10 OHMS		15	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335102	RES COMP 1/4W 5% 1 K		16	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335103	RES COMP 1/4W 5% 10 K		17	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335151	RES COMP 1/4W 5% 150 OHMS		18	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335152	RES COMP 1/4W 5% 1.5 K		19	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335153	RES COMP 1/4W 5% 15 K		20	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335180	RES COMP 1/4W 5% 18 OHMS		21	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335181	RES COMP 1/4W 5% 180 OHMS		22	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335202	RES COMP 1/4W 5% 2 K		23	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335220	RES COMP 1/4W 5% 22 OHMS		24	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335221	RES COMP 1/4W 5% 220 OHMS		25	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
161335270	RES COMP 1/4W 5% 27 OHMS		26	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335330	RES COMP 1/4W 5% 33 OHMS		27	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335331	RES COMP 1/4W 5% 330 OHMS		28	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335470	RES COMP 1/4W 5% 47 OHMS		29	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335471	RES COMP 1/4W 5% 470 OHMS		30	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335510	RES COMP 1/4W 5% 51 OHMS		31	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
161335512	RES COMP 1/4W 5% 5.1 K		32	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335560	RES COMP 1/4W 5% 56 OHMS		33	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335824	RES COMP 1/4W 5% 820 K		34	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335910	RES COMP 1/4W 5% 91 OHMS		35	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531377	RES PREC RN55D 681 OHMS		36	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
168531409	RES PREC RN55D 1.47K		37	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531433	RES PREC RN55D 2.61 K		38	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531457	RES PREC RN55D 4.64 K		39	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531597	RES PREC RN55D 133K		40	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
181457203	RES VARI CERMET 20 K		41	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190642102	RESISTOR NETWORK 1 K		42	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
190642331	RESISTOR NETWORK 330 OHMS		43	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190642471	RESISTOR NETWORK 470 OHMS		44	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
190842471	RESISTOR NETWORK 470 OHMS		45	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
200031028	IC 2-IN NAND GT SN74LS00N		46	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031051	IC 2-IN NOR GT SN74LS02N		47	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031072	IC 4-IN PGS AND SN74LS21N		48	P	EA	1.00	1.000	10	0	00/00/00	99/99/99

INDENTED BILL OF MATERIALS

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: V9400-4
DESC: VARIANT SUB'Y V9400-4 UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	ST SC	UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
200031086	IC 2-IN AND GAT SN74LS08N		49	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
200031089	IC BUS BUFFER SN74LS125N		50	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
200031101	IC BINARY CNTR SN74LS393N		51	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
200041008	IC J-K FLIP-FL SN74S112N		52	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
200041026	IC 4-BIT CTR SN74LS161N		53	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
200041027	IC QUAD SEL/MP SN74LS157N		54	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
200041042	IC UP/DN COUNT SN74LS191N		55	P	EA	6.00	1.000	10	0	00/00/00	99/99/9
200041054	IC DATA SELCTR SN74LS153N		56	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
200041062	IC DEC/DEMULTP SN74LS138N		57	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
200041073	IC 4-BIT CNTR SN74LS160N		58	P	EA	5.00	1.000	10	0	00/00/00	99/99/9
200071003	IC 8-BIT REGIST SN74LS374		59	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
200071005	IC D-TYP FL-FL SN74LS273N		60	P	EA	4.00	1.000	10	0	00/00/00	99/99/9
200071007	IC OCTAL BUFF SN74LS244N		61	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
200071245	IC BUS XCEIVER SN74LS245N		62	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
200071373	IC 8XLATCH D-TYPE 74LS373		63	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
200081007	IC MULTIPLEXER SN74LS151		64	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
200330010	IC 3-INPUT NAND 74F10		65	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
200330126	IC BUS BUFFER SN74LS126A		66	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
200340074	IC D-TYPE POS FLOP 74F74		67	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
200344105	IC 2-3-2-IN OR/NOR 10H105		68	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
200344131	IC DUAL D M-S FLOP 10H131		69	P	EA	5.00	1.000	10	0	00/00/00	99/99/9
200444016	IC BINARY COUNTER 10H016		70	P	EA	5.00	1.000	10	0	00/00/00	99/99/9
204042004	IC 4-3-3 IN GATE MC10105P		71	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
204042007	IC QUAD TRANSL MC10124P		72	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
204042008	IC QUAD TRANSL MC10125P		73	P	EA	4.00	1.000	10	0	00/00/00	99/99/9
204042011	IC LINE RECEIVER MC10116P		74	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
204042016	IC 2-INPUT OR/NOR F10101P		75	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
207444116	IC TRIPL LINE RCVR 10H116		76	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
208011003	IC SINGLE OP AMP LM301AN		77	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
208021501	IC VOLT REG DUAL SG4501J		78	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
230110005	DIODE SWITCHING 1N4448		79	P	EA	4.00	1.000	10	0	00/00/00	99/99/9
253010811	DIODE SCHOTTKY BAR HP2811		80	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
270130401	TRANSISTOR NPN A401		81	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
275170001	TRANSISTOR PNP 2N5087		82	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
275170002	TRANSISTOR PNP 2N5771		83	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
300020002	BEAD SHIELDING FERRITE		84	P	EA	6.00	1.000	10	0	00/00/00	99/99/9
300050001	CHOKE FERRITE SINGLE LEAD		85	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
301016103	INDUCTOR MOLDED 10 UH		86	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
310062100	CRYSTAL 10PPM 100MHZ		87	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
454310002	HDR DIP SOLD TO PC BD 2		88	P	EA	8.00	1.000	10	0	00/00/00	99/99/9
454370012	HEADER 2-SIDED FEMALE 12		89	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
454510002	HDR DIP SOLDER TO MALE 2		90	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
454610096	HDR DIP SOLD TO MALE 96		91	P	EA	1.00	1.000	10	0	00/00/00	99/99/9
480033001	CABLE CO-AX 30CM SMB-SMC		92	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
500110001	TRANSIPAD 'SMALL'		93	P	EA	3.00	1.000	10	0	00/00/00	99/99/9
585252354	RIVET HOLLOW 2,5X9MM		94	P	EA	2.00	1.000	10	0	00/00/00	99/99/9
SM661286103	CAP CERA CHIP 10% .01 UF		95	P	EA	6.00	1.000	10	0	00/00/00	99/99/9
719400403	PC BD PREAASS'Y 9400-4		96	B	EA	1.00	1.000	10	0	00/00/00	99/99/9
MVL407	IC MONO QUAD DISCR MVL407		97	P	EA	1.00	1.000	10	0	00/00/00	99/99/9

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

ASS CODE: 2
3ASSEMBLIES
RT: F9400A-51
SC: COMPLETED BOARD F9400A-51 UOM: EA SC: R REV:

PONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UN	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
3456789012345678901234 5-----------	------------------------------	--	-----	--	--	----------	-----	-----	-------	--------	--------
5068001	KNOB FOR 6MM SHAFT		1	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
5068002	KNOB FOR 3MM SHAFT		2	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
5068003	CAP (FOR KNOB 020-2215)		3	P	EA	7.00	1.000	10	0	00/00/00	99/99/99
5068005	CAP FOR 020-3215 OR -3415		4	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
5068006	CAP FOR 021-1110 OR -2215		5	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
5168001	KNOB FOR 1/8" SHAFT		6	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
168002	KNOB FOR 1/8" SHAFT		7	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168003	KNOB FOR 1/8" SHAFT		8	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
425500	SPEED NUT ID 2.5MM		11	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
400501	DISPLAY FRAME 9400-5		12	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
400513	FRONT PANEL 9400A-5		13	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
327103	CAP CERA MONO 50V .01 UF		15	P	EA	12.00	1.000	0	0	02/05/89	99/99/99
824685	CAP TANT DIP CASE 6.8 UF		16	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
225102	RES 1/8W 5% 1K		17	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
225121	RES COMP 1/8W 5% 120 OHMS		18	P	EA	14.00	1.000	0	0	02/05/89	99/99/99
225201	RES COMP 1/8W 5% 200 OHMS		19	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
417502	RES VARI COND PLASTIC 5 K		20	P	EA	6.00	1.000	0	0	02/05/89	99/99/99
427502	RES VARI COND PLASTIC 5 K		21	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
437502	RES VARI COND PLASTIC 5 K		22	P	EA	5.00	1.000	0	0	02/05/89	99/99/99
041062	IC DEC/DEMULTP SN74LS138N		23	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
041139	IC DEC/MULTIPL SN74LS139N		24	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
630164	IC SHIFT REGISTER 74F164		25	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
345051	IC MUX/DEMUX HCT4051		26	P	EA	3.00	1.000	0	0	02/05/89	99/99/99
020062	DIODE SWITCHING BAW62		27	P	EA	47.00	1.000	0	0	02/05/89	99/99/99
110005	DIODE SWITCHING 1N4448		28	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
243300	DIODE LED RED HLMP-0300		29	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
443421	DIODE LED YEL HLMP-0421		30	P	EA	30.00	1.000	0	0	02/05/89	99/99/99
151034	HEADER STRAIGHT ST 34-PIN		31	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
950002	POLARIZING KEY		32	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
001012	SWITCH ROT N/STOP 12-PINS		33	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
161002	SWITCH PUSHBUTTON SPST		34	P	EA	41.00	1.000	0	0	02/05/89	99/99/99
430106	SCREW CYL HD PHIL M3X6		35	P	EA	20.00	1.000	0	0	02/05/89	99/99/99
430300	WASHER SHAKEPROOF M3		36	P	EA	20.00	1.000	0	0	02/05/89	99/99/99
230108	SPACER HEX M3X8MM		37	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
400511	LED COVER 9400-5	A	38	B	EA	32.00	1.000	0	0	02/05/89	99/99/99
450523	PUSH SWITCH EXTENDER		39	B	EA	41.00	1.000	0	0	02/05/89	99/99/99
400533	PC BD PREASS'Y 9400A-51		40	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
400543	PC BD PREASS'Y 9400A-52		41	B	EA	1.00	1.000	0	0	02/05/89	99/99/99

MFG:RE,291,2 LeCroy SA MANUFACTURING MANAGEMENT DATABASE 999 DATABASE: 999 REQUESTER: BRUNO_K
16-MAY-1989 09:44 INDENTED BILL OF MATERIALS PAGE NO: 1

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SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-7
DESC: COMPLETED BOARD F9400-7 UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
1234567890123456789012345------------	------------------------------	--	-----	--	--	----------	-----	-----	-------	--------	--------
102412220	CAP CERA DISC 100V 22 PF		1	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102940502	CAP CERA DISC 1KV .005 UF		2	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
103307103	CAP CERA MONO 50V .01 UF		3	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103327102	CAP CERA MONO 50V .001 UF		4	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103427104	CAP CERA MONO 100V .1 UF		5	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
146634106	CAP MINI ALUM 20% 10 UF		6	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
147956047	CAP ALUM METAL CAN 47 UF		7	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161030000	RES COMP ZERO OHM		8	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335102	RES COMP 1/4W 5% 1 K		9	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
161335103	RES COMP 1/4W 5% 10 K		10	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335104	RES COMP 1/4W 5% 100 K		11	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335105	RES COMP 1/4W 5% 1 MEG		12	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335152	RES COMP 1/4W 5% 1.5 K		13	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335162	RES COMP 1/4W 5% 1.6 K		14	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335203	RES COMP 1/4W 5% 20 K		15	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
161335223	RES COMP 1/4W 5% 22 K		16	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335224	RES COMP 1/4W 5% 220 K		17	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335273	RES COMP 1/4W 5% 27 K		18	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335302	RES COMP 1/4W 5% 3 K		19	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335303	RES COMP 1/4W 5% 30 K		20	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335473	RES COMP 1/4W 5% 47 K		21	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335474	RES COMP 1/4W 5% 470 K		22	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335512	RES COMP 1/4W 5% 5.1 K		23	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335513	RES COMP 1/4W 5% 51 K		24	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335682	RES COMP 1/4W 5% 6.8 K		25	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335912	RES COMP 1/4W 5% 9.1 K		26	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161445560	RES CARBON FILM 56 OHMS		27	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
165375824	RES METAL FILM HV 820 K		28	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168035125	RES METAL FILM HV 1.2 MEG		29	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
168531529	RES PREC RN55D 26.1 K		30	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
180487205	RES VARI CERMET 2 MEG		31	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
230110005	DIODE SWITCHING 1N4448		32	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
240225712	DIODE ZENER 8.2V 1N5237		33	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
240513977	DIODE ZENER 47V 1N977B		34	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
270170002	TRANSISTOR NPN 2N5962		35	P	EA	7.00	1.000	10	0	00/00/00	99/99/99
275170001	TRANSISTOR PNP 2N5087		36	P	EA	5.00	1.000	10	0	00/00/00	99/99/99
322307002	SOCKET CRT TUBE PC MTG		37	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
433220003	FUSE SUB-MINI 1/2 AMP		38	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
455122008	CONNECTOR HOUSING 8		39	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
455950002	CLAMP WITH STRAIN RELIEF		40	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
594120003	TIEWRAP		41	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
719400703	PC BD PREASS'Y 9400-7		43	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
780060010	WIRE TYPE 006 BLACK 10CM		44	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
780061110	WIRE TYPE 006 BROWN 10CM		45	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
780062210	WIRE TYPE 006 RED 10CM		46	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
780064410	WIRE TYPE 006 YELLOW 10CM		47	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
780065510	WIRE TYPE 006 GREEN 10CM		48	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
780066610	WIRE TYPE 006 BLUE 10CM		49	B	EA	1.00	1.000	10	0	00/00/00	99/99/99
780069910	WIRE TYPE 006 WHITE 10CM		50	B	EA	1.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-8
DESC: COMPLETED BOARD F9400-8 UOM: EA SC: R REV:

COMPONENT PART 2345678901234567890123456789012345	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
02412101	CAP CERA DISC 100V 100PF		1	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
03307103	CAP CERA MONO 50V .01 UF		2	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
61225220	RES COMP 1/8W 5% 22 OHMS		3	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
61225360	RES COMP 1/8W 5% 36 OHMS		4	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
61225430	RES COMP 1/8W 5% 43 OHMS		5	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
54311012	HDR DIP SOLD TO MALE 12		6	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
19400803	PC BD PREASS'Y 9400-8		7	R	EA	1.00	1.000	10	0	00/00/00	99/99/99

MFG,RE,291,2 LeCroy SA MANUFACTURING MANAGEMENT DATABASE 999 DATABASE: 999 REQUESTER: BRUNO_K
16-MAY-1989 09:44 INDENTED BILL OF MATERIALS PAGE NO: 1

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-9/115V
DESC: COMPLETED BOARD F9400-9/115V UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
123456789012345678901234 5-----------	-------------------------------	--	-----	--	--	----------	-----	-----	-------	--------	--------
315680057	P S 115V AC 10A 5V		1	P	EA	2.00	1.000	10	0	01/01/88	99/99/99
315680058	P S 115V AC 3.3A 15V		2	P	EA	2.00	1.000	10	0	01/01/88	99/99/99
433162315	FUSE SLO-BLO 250V 3.15AMP		4	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
550425510	SCREW FLATHD PHIL M2.5X10		5	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
550425512	SCR FLAT HD PHIL M2.5X12		6	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
550430108	SCREW CYL HD PHIL M3X8		7	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
709400931	GRIP BRACKET		11	B	EA	8.00	1.000	10	0	00/00/00	99/99/99
433162200	FUSE SLO-BLO 250V 2AMP		14	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
434512001	FUSEHOLDER HORIZ PC MTG		15	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
454110012	HDR SOLD TAIL/MALEPINS 12		16	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
454420015	HDR SOLD TAIL-FEMALE 15		17	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
455111003	BLOCK FOR MALE PIN 3		18	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
455210006	BLOC FOR CRIMP MALE PIN 6		19	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
594120003	TIEWRAP		20	P	EA	15.00	1.000	0	0	02/05/89	99/99/99
719400913	PC BD PREASS'Y 9400-9A		21	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080010	WIRE TYPE 008 BLACK 10CM		22	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080011	WIRE TYPE 008 BLACK 11CM		23	B	EA	2.00	1.000	0	0	02/05/89	99/99/99
780080024	WIRE TYPE 008 BLACK 24CM		24	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080025	WIRE TYPE 008 BLACK 25CM		25	B	EA	2.00	1.000	0	0	02/05/89	99/99/99
780080026	WIRE TYPE 008 BLACK 26CM		26	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080029	WIRE TYPE 008 BLACK 29CM		27	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080030	WIRE TYPE 008 BLACK 30CM		28	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
312590125	BATTERY NICAD 1.25V		29	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
315940001	LINE FILTER 115-220V		30	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
402001304	CONN BULKHEAD MTG 4-POS		31	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
405748003	TERMINAL WIRE END SPADE		32	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
453910002	METRIC SCREW LOCK HDW KIT		33	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
515404030	BATTERY HOLDER		34	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
530409199	FAN AXIAL 115V-220V		35	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
530409996	FILTER FOR PAPST FAN 4014		36	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
550425508	SCREW FLAT HD PHIL M2.5X8		37	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
550430106	SCREW CYL HD PHIL M3X6		38	P	EA	3.00	1.000	0	0	02/05/89	99/99/99
550430110	SCREW CYL HD PHIL M3X10		39	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
550430416	SCREW CYL INT HEX M3X16		40	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
550430508	SCREW FLAT HD PHIL M3X8		41	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
551230100	FLAT WASHER M3.2		42	P	EA	9.00	1.000	0	0	02/05/89	99/99/99
551430400	WASHER SHAKEPROOF M3		43	P	EA	18.00	1.000	0	0	02/05/89	99/99/99
552425300	NUT OPEN-END ACORN M2.5		44	P	EA	10.00	1.000	0	0	02/05/89	99/99/99
552430200	NUT ACORN M3		45	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
552430300	NUT OPEN-END ACORN M3		46	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
553230120	SPACER HEX M3X20MM		47	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
554500001	TAPPING SCREW W/U-THREAD		48	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
591101022	WIRE BUS TIN-COPP AWG 22		49	P	ME	0.30	1.000	0	0	02/05/89	99/99/99
RP9400-9	COMPLETED BOARD RP9400-9		51	R	EA	1.00	1.000	0	0	02/05/89	99/99/99
709400901	REAR PANEL 9400-9		1	B	EA	1.00	1.000	0	0	00/00/00	99/99/99
709400913	REAR PANEL GRID 9400-9		53	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
709400923	SERIAL NUMBER PLATE		54	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
709400961	COVER PLATE FOR 9400-A		55	B	EA	0.10	1.000	0	0	02/05/89	99/99/99
780128846	CABLE RS 232		56	B	EA	1.00	1.000	0	0	02/05/89	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

ASS CODE: 2
BASSEMBLIES
RT: F9400-9/115V
SC: COMPLETED BOARD F9400-9/115V   UOM: EA   SC: R   REV:

MPONENT PART 3456789012345678901234 5	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
0141140	CABLE GPIB		57	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0151136	SWITCH CABLE		58	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0171656	LINE CABLE		59	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
1335122	RES COMP 1/4W 5% 1.2 K		60	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
1335153	RES COMP 1/4W 5% 15 K		61	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
5749003	TAB PC MTG 2.8 X .5 MM		62	P	EA	6.00	1.000	0	0	02/05/89	99/99/99
5111012	BLOCK FOR FEM PINS 12		63	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
5121012	CONNECTOR HOUSING 12		64	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
5950002	CLAMP WITH STRAIN RELIEF		65	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
5802205	SLEEVING PLASTIC 5MM ID		67	P	ME	0.30	1.000	0	0	02/05/89	99/99/99
9400940	LINE SYNC TRANSFORMER		68	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
9400943	PC BD PREASS'Y 9400-9D		69	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0031135	WIRE TYPE 003 BROWN 35CM		70	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0032235	WIRE TYPE 003 RED 35CM		71	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0034435	WIRE TYPE 003 YELLOW 35CM		72	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0036635	WIRE TYPE 003 BLUE 35CM		73	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0060017	WIRE TYPE 006 BLACK 17CM		74	B	EA	2.00	1.000	0	0	02/05/89	99/99/99
0062217	WIRE TYPE 006 RED 17CM		75	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0064417	WIRE TYPE 006 YELLOW 17CM		76	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0065517	WIRE TYPE 006 GREEN 17CM		77	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0066617	WIRE TYPE 006 BLUE 17CM		78	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0069917	WIRE TYPE 006 WHITE 17CM		79	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0090004	WIRE TYPE 009 BLACK 4CM		80	B	EA	4.00	1.000	0	0	02/05/89	99/99/99
0111111	WIRE TYPE 011 BROWN 11CM		81	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0112211	WIRE TYPE 011 RED 11CM		82	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0114411	WIRE TYPE 011 YELLOW 11CM		83	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
0116611	WIRE TYPE 011 BLUE 11CM		84	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
4786223	CAP POLY FILM .022 UF		85	P	EA	5.00	1.000	0	0	02/05/89	99/99/99

INDENTED BILL OF MATERIALS
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SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-9/220V
DESC: COMPLETED BOARD F9400-9/220V UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
1234567890123456789012345-----------	------------------------------	--	-----	--	--	----------	-----	-----	--------	--------	--------
315680053	P S 220V AC 10A 5V		1	P	EA	2.00	1.000	10	0	01/01/88	99/99/99
315680054	P S 220V AC 3.3A 15V		2	P	EA	2.00	1.000	10	0	01/01/88	99/99/99
433162160	FUSE SLO-BLO 250V 1.6AMP		3	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
550425510	SCREW FLATHD PHIL M2.5X10		5	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
550425512	SCR FLAT HD PHIL M2.5X12		6	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
550430108	SCREW CYL HD PHIL M3X8		7	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
709400931	GRIP BRACKET		11	B	EA	8.00	1.000	10	0	00/00/00	99/99/99
433162200	FUSE SLO-BLO 250V 2AMP		14	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
434512001	FUSEHOLDER HORIZ PC MTG		15	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
454110012	HDR SOLD TAIL/MALEPINS 12		16	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
454420015	HDR SOLD TAIL-FEMALE 15		17	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
455111003	BLOCK FOR MALE PIN 3		18	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
455210006	BLOC FOR CRIMP MALE PIN 6		19	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
594120003	TIEWRAP		20	P	EA	15.00	1.000	0	0	02/05/89	99/99/99
719400913	PC BD PREASS'Y 9400-9A		21	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080010	WIRE TYPE 008 BLACK 10CM		22	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080011	WIRE TYPE 008 BLACK 11CM		23	B	EA	2.00	1.000	0	0	02/05/89	99/99/99
780080024	WIRE TYPE 008 BLACK 24CM		24	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080025	WIRE TYPE 008 BLACK 25CM		25	B	EA	2.00	1.000	0	0	02/05/89	99/99/99
780080026	WIRE TYPE 008 BLACK 26CM		26	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080029	WIRE TYPE 008 BLACK 29CM		27	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780080030	WIRE TYPE 008 BLACK 30CM		28	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
312590125	BATTERY NICAD 1.25V		29	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
315940001	LINE FILTER 115-220V		30	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
402001304	CONN BULKHEAD MTG 4-POS		31	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
405748003	TERMINAL WIRE END SPADE		32	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
453910002	METRIC SCREW LOCK HDW KIT		33	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
515404030	BATTERY HOLDER		34	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
530409199	FAN AXIAL 115V-220V		35	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
530409996	FILTER FOR PAPST FAN 4014		36	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
550425508	SCREW FLAT HD PHIL M2.5X8		37	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
550430106	SCREW CYL HD PHIL M3X6		38	P	EA	3.00	1.000	0	0	02/05/89	99/99/99
550430110	SCREW CYL HD PHIL M3X10		39	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
550430416	SCREW CYL INT HEX M3X16		40	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
550430508	SCREW FLAT HD PHIL M3X8		41	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
551230100	FLAT WASHER M3.2		42	P	EA	9.00	1.000	0	0	02/05/89	99/99/99
551430400	WASHER SHAKEPROOF M3		43	P	EA	18.00	1.000	0	0	02/05/89	99/99/99
552425300	NUT OPEN-END ACORN M2.5		44	P	EA	10.00	1.000	0	0	02/05/89	99/99/99
552430200	NUT ACORN M3		45	P	EA	4.00	1.000	0	0	02/05/89	99/99/99
552430300	NUT OPEN-END ACORN M3		46	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
553230120	SPACER HEX M3X20MM		47	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
554500001	TAPPING SCREW W/U-THREAD		48	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
591101022	WIRE BUS TIN-COPP AWG 22		49	P	ME	0.30	1.000	0	0	02/05/89	99/99/99
RF9400-9	COMPLETED BOARD RF9400-9		51	R	EA	1.00	1.000	0	0	02/05/89	99/99/99
709400901	REAR PANEL 9400-9		1	B	EA	1.00	1.000	0	0	00/00/00	99/99/99
709400913	REAR PANEL GRID 9400-9		53	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
709400923	SERIAL NUMBER PLATE		54	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
709400961	COVER PLATE FOR 9400-A		55	B	EA	0.10	1.000	0	0	02/05/89	99/99/99
780128846	CABLE RS 232		56	B	EA	1.00	1.000	0	0	02/05/89	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9400-9/220V
DESC: COMPLETED BOARD F9400-9/220V UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
780141140	CABLE GPIB		57	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780151136	SWITCH CABLE		58	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780171656	LINE CABLE		59	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
161335122	RES COMP 1/4W 5% 1.2 K		60	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
161335153	RES COMP 1/4W 5% 15 K		61	P	EA	2.00	1.000	0	0	02/05/89	99/99/99
105749003	TAB PC MTG 2.8 X .5 MM		62	P	EA	6.00	1.000	0	0	02/05/89	99/99/99
155111012	BLOCK FOR FEM PINS 12		63	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
155121012	CONNECTOR HOUSING 12		64	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
155950002	CLAMP WITH STRAIN RELIEF		65	P	EA	1.00	1.000	0	0	02/05/89	99/99/99
395802205	SLEEVING PLASTIC 5MM ID		67	P	ME	0.30	1.000	0	0	02/05/89	99/99/99
709400940	LINE SYNC TRANSFORMER		68	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
719400943	PC BD PREASS'Y 9400-9D		69	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780031135	WIRE TYPE 003 BROWN 35CM		70	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780032235	WIRE TYPE 003 RED 35CM		71	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780034435	WIRE TYPE 003 YELLOW 35CM		72	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780036635	WIRE TYPE 003 BLUE 35CM		73	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780060017	WIRE TYPE 006 BLACK 17CM		74	B	EA	2.00	1.000	0	0	02/05/89	99/99/99
780062217	WIRE TYPE 006 RED 17CM		75	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780064417	WIRE TYPE 006 YELLOW 17CM		76	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780065517	WIRE TYPE 006 GREEN 17CM		77	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780066617	WIRE TYPE 006 BLUE 17CM		78	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780069917	WIRE TYPE 006 WHITE 17CM		79	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780090004	WIRE TYPE 009 BLACK 4CM		80	B	EA	4.00	1.000	0	0	02/05/89	99/99/99
780111111	WIRE TYPE 011 BROWN 11CM		81	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780112211	WIRE TYPE 011 RED 11CM		82	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780114411	WIRE TYPE 011 YELLOW 11CM		83	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
780116611	WIRE TYPE 011 BLUE 11CM		84	B	EA	1.00	1.000	0	0	02/05/89	99/99/99
124786223	CAP POLY FILM .022 UF		85	P	EA	5.00	1.000	0	0	02/05/89	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9401-2
DESC: COMPLETED BOARD F9401-2 UOM: EA SC: R REV:

COMPONENT PART 123456789012345678901234 5	DESCRIPTION	RV	ITEM NUMBR	ST SC	UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
102412101	CAP CERA DISC 100V 100PF		1	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412180	CAP CERA DISC 100V 18 PF		2	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412330	CAP CERA DISC 100V 33PF		3	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412560	CAP CERA DISC 100V 56 PF		4	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103307103	CAP CERA MONO 50V .01 UF		5	P	EA	23.00	1.000	10	0	00/00/00	99/99/99
103427104	CAP CERA MONO 100V .1 UF		6	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103506331	CAP CERA MONO 100V 330 PF		7	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103625471	CAP CERA MONO 100V 470 PF		8	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
142214156	CAP TANT DIP CASE 15 UF		9	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
146424106	CAP MINI ALUM 20% 10 UF		10	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335102	RES COMP 1/4W 5% 1 K		11	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
161335103	RES COMP 1/4W 5% 10 K		12	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335163	RES COMP 1/4W 5% 16 K		13	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335301	RES COMP 1/4W 5% 300 OHMS		14	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335471	RES COMP 1/4W 5% 470 OHMS		15	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335511	RES COMP 1/4W 5% 510 OHMS		16	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335512	RES COMP 1/4W 5% 5.1 K		17	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190042103	RESISTOR NETWORK 10 K		18	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190642102	RESISTOR NETWORK 1 K		19	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190842562	RES NETWORK 5.6K		20	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031028	IC 2-IN NAND GT SN74LS00N		21	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031049	IC FLIP-FLOP SN74LS74N		22	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031051	IC 2-IN NOR GT SN74LS02N		23	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031066	IC POS NAND GT SN74LS132N		24	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031073	IC 2-IN POS OR SN74LS32N		25	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031086	IC 2-IN AND GAT SN74LS08N		26	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200031089	IC BUS BUFFER SN74LS125N		27	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031095	IC HEX INVERTER SN74LS14N		28	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041044	IC MULTIVIBR SN74LS123N		29	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041066	IC FLIP-FLOP SN74LS109N		30	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041139	IC DEC/MULTIPL SN74LS139N		31	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200071007	IC OCTAL BUFF SN74LS244N		32	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200071245	IC BUS XCEIVER SN74LS245N		33	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200330033	IC QUAD 2-IN NOR SN74LS33		34	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200441002	IC MULTIVIBRATOR AM26S02		35	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
207197210	IC BUS INTERF CONTR 7210		36	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
207470160	IC OCTAL BUS XCVR 75160A		37	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
207470161	IC OCTL BUS XCEIR 75161A		38	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
240225703	DIODE ZENER 3.45V 1N703A		39	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
253010835	DIODE HOT CARRIER HP2835		40	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
270170002	TRANSISTOR NPN 2N5962		41	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
275170002	TRANSISTOR PNP 2N5771		42	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
400331016	SOCKET IC ST DIP-16		43	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
403950002	POLARIZING KEY		44	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
454211016	HDR SOLD TAIL TO MALE 16		45	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454211026	HDR SOLD TAIL TO MALE 26		46	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454610096	HDR DIP SOLD TO MALE 96		47	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
454620096	HDR SOLD TAIL/FEM PIN 96		48	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
585252354	RIVET HOLLOW 2,5X9MM		49	P	EA	4.00	1.000	10	0	00/00/00	99/99/99

INDENTED BILL OF MATERIALS

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

.ASS CODE: 2
JBASSEMBLIES
ART: F9401-2
ESC: COMPLETED BOARD F9401-2   UOM: EA SC: R REV:

OMPONENT PART 234567890123456789012345	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
.9401203	PC BD PREASS'Y 9401-2		50	B	EA	1.00	1.000	10	0	00/00/00	99/99/99

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9401-2/1
DESC: COMPLETED BOARD F9401-2/1   UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	ST SC	UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
1234567890123456789012345------------	------------------------------	--	-----	--	--	----------	-----	------	-------	--------	--------
102412101	CAP CERA DISC 100V 100PF		1	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412121	CAP CERA DISC 100V 120 PF		2	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412180	CAP CERA DISC 100V 18 PF		3	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
102412330	CAP CERA DISC 100V 33PF		4	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
102412560	CAP CERA DISC 100V 56 PF		5	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103307103	CAP CERA MONO 50V .01 UF		6	P	EA	35.00	1.000	10	0	00/00/00	99/99/99
103427104	CAP CERA MONO 100V .1 UF		7	P	EA	17.00	1.000	10	0	00/00/00	99/99/99
103506331	CAP CERA MONO 100V 330 PF		8	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103625471	CAP CERA MONO 100V 470 PF		9	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
142214156	CAP TANT DIP CASE 15 UF		10	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
146424106	CAP MINI ALUM 20% 10 UF		11	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335102	RES COMP 1/4W 5% 1 K		12	P	EA	8.00	1.000	10	0	00/00/00	99/99/99
161335103	RES COMP 1/4W 5% 10 K		13	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335163	RES COMP 1/4W 5% 16 K		14	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
161335301	RES COMP 1/4W 5% 300 OHMS		15	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335471	RES COMP 1/4W 5% 470 OHMS		16	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335511	RES COMP 1/4W 5% 510 OHMS		17	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
161335512	RES COMP 1/4W 5% 5.1 K		18	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190042103	RESISTOR NETWORK 10 K		19	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190642102	RESISTOR NETWORK 1 K		20	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
190842562	RES NETWORK 5.6K		21	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031028	IC 2-IN NAND GT SN74LS00N		22	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200031049	IC FLIP-FLOP SN74LS74N		23	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031051	IC 2-IN NOR GT SN74LS02N		24	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031066	IC POS NAND GT SN74LS132N		25	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031073	IC 2-IN POS OR SN74LS32N		26	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200031086	IC 2-IN AND GAT SN74LS08N		27	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200031089	IC BUS BUFFER SN74LS125N		28	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031095	IC HEX INVERTER SN74LS14N		29	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200031101	IC BINARY CNTR SN74LS393N		30	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200041044	IC MULTIVIBR SN74LS123N		31	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041066	IC FLIP-FLOP SN74LS109N		32	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200041070	IC DAT SEL/MP SN74LS257AN		33	P	EA	3.00	1.000	10	0	00/00/00	99/99/99
200041139	IC DEC/MULTIPL SN74LS139N		34	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200071007	IC OCTAL BUFF SN74LS244N		35	P	EA	6.00	1.000	10	0	00/00/00	99/99/99
200071245	IC BUS XCEIVER SN74LS245N		36	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200072966	IC 8X DYN MEM DRIV AM2966		37	P	EA	2.00	1.000	10	0	00/00/00	99/99/99
200330033	IC QUAD 2-IN NOR SN74LS33		38	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200340074	IC D-TYPE POS FLOP 74F74		39	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200341175	IC D-TYPE FLOP 74F175		40	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
200441002	IC MULTIVIBRATOR AM26S02		41	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
205240256	IC RAM HM50256-15		42	P	EA	16.00	1.000	10	0	00/00/00	99/99/99
207197210	IC BUS INTERF CONTR 7210		43	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
207470160	IC OCTAL BUS XCVR 75160A		44	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
207470161	IC OCTL BUS XCEIR 75161A		45	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
240225703	DIODE ZENER 3.45V 1N703A		46	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
253010835	DIODE HOT CARRIER HP2835		47	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
270170002	TRANSISTOR NPN 2N5962		48	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
275170002	TRANSISTOR PNP 2N5771		49	P	EA	1.00	1.000	10	0	00/00/00	99/99/99

INDENTED BILL OF MATERIALS

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: F9401-2/1
DESC: COMPLETED BOARD F9401-2/1 UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
100331016	SOCKET IC ST DIP-16		50	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
103950002	POLARIZING KEY		51	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
154211016	HDR SOLD TAIL TO MALE 16		52	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
154211026	HDR SOLD TAIL TO MALE 26		53	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
154610096	HDR DIP SOLD TO MALE 96		54	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
154620096	HDR SOLD TAIL/FEM PIN 96		55	P	EA	1.00	1.000	10	0	00/00/00	99/99/99
185252354	RIVET HOLLOW 2,5X9MM		56	P	EA	4.00	1.000	10	0	00/00/00	99/99/99
719401203	PC BD PREASS'Y 9401-2		57	B	EA	1.00	1.000	10	0	00/00/00	99/99/99

MFG,RE,291,2 LeCroy SA MANUFACTURING MANAGEMENT DATABASE 999 DATABASE: 999 REQUESTER: BRUNO_I
16-MAY-1989 09:46 PAGE NO:

INDENTED BILL OF MATERIALS
==========================

SORTED BY ASSEMBLY PART NUMBER, ITEM NUMBER
AS OF 16/05/89

CLASS CODE: 2
SUBASSEMBLIES
PART: ACCESSORIES-9400A
DESC: ACCESSORIES FOR 9400A UOM: EA SC: R REV:

COMPONENT PART	DESCRIPTION	RV	ITEM NUMBR	SC	ST UM	QTY PER ASSEMBLY	YIELD FACTR	ROUTE TO SEQ	OFFSET LEAD TIME	EFFECTIV DATE	INACTIVE DATE
589203218	AC CORD/US-CANADA PLUG		1	P	EA	0.60	1.000	0	0	00/00/00	99/99/9
589202100	AC CORD/PLUG FOR FRANCE		2	P	EA	0.10	1.000	0	0	00/00/00	99/99/9
589202200	AC CORD/PLUG FOR GERMANY		3	P	EA	0.15	1.000	0	0	00/00/00	99/99/9
589203100	AC CORD/'SEV-ASE' PLUG		4	P	EA	0.05	1.000	0	0	00/00/00	99/99/9
407099008	PLUG FOR AC LINE -ENGLAND		5	P	EA	0.10	1.000	0	0	00/00/00	99/99/9
433162315	FUSE SLO-BLO 250V 3.15AMP		6	P	EA	1.20	1.000	0	0	00/00/00	99/99/9
433162160	FUSE SLO-BLO 250V 1.6AMP		7	P	EA	0.80	1.000	0	0	00/00/00	99/99/9
P9010	PROBE DC-250MHZ/ATTN 10:1		8	P	EA	2.00	1.000	0	0	00/00/00	99/99/9
597940011	SHIPPING CARTON 9400		9	P	EA	1.00	1.000	0	0	00/00/00	99/99/9
597940012	SHIPPING INSERT 9400		10	P	EA	2.00	1.000	0	0	00/00/00	99/99/9
597940014	PLASTIC BAG FOR 9400		11	P	EA	2.00	1.000	0	0	00/00/00	99/99/9
597940015	MANUAL/ACCESSORY CTN 9400		12	P	EA	1.00	1.000	0	0	00/00/00	99/99/9
OM9400A-E	OPERATOR'S MANUAL 9400A		13	B	EA	0.80	1.000	0	0	25/04/89	99/99/9
OM9400A-F	OPERATOR'S MANUAL 9400A		14	B	EA	0.10	1.000	0	0	25/04/89	99/99/9
OM9400A-G	OPERATOR'S MANUAL 9400A		15	B	EA	0.10	1.000	0	0	25/04/89	99/99/9

MODEL NO 9400 DIGITAL OSCILLOS. PRINTED 12-Apr-88
ECON 2035 REV DATE 25-Nov-87
MCN 0 MCN DATE 25-Nov-87

LRS	PART NO		DESCRIPTION				QTY
323	120	*10	PROBE DC-250MHZ/ATTN 10:1 LECROY LOGO/1.2 M/1.4NS RISE/EUROPE				2
829	400	**0	LOOSE PARTS	M9400		PL:M9400	1
869	400	100	COMPLETED BOARD	F9400-1	839400101(1)	PL:F9400-1	1
869	400	200	COMPLETED BOARD	F9400-2	839400200(1)	PL:F9400-2	1
869	400	310	COMPLETED BOARD	F9400-3A	839400310(1)	PL:F9400-3A	2
869	400	400	COMPLETED BOARD	F9400-4	839400400(1)	PL:F9400-4	1
869	400	500	COMPLETED BOARD	F9400-5	859400500(1)	PL:F9400-5	1
869	400	700	COMPLETED BOARD	F9400-7	839400700(1)	PL:F9400-7	1
869	400	800	COMPLETED BOARD	F9400-8	839400800(1)	PL:F9400-8	1
869	400	900	COMPLETED BOARD	F9400-9	859400900(1)839400901(1)	PL:F9400-9	1
869	401	200	COMPLETED BOARD	F9401-2	839401200 (1)	PL:F9401-2	1

NOTE: 1
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MODEL NO 9400A　　　　DUAL 175MHZ OSCIL.　　　　PRINTED 12-Apr-88
ECON 2000　　　　REV DATE 10-Mar-88
MCN 0　　　　MCN DATE 10-Mar-88

LRS	PART NO		DESCRIPTION				QTY
323	120	*10	PROBE DC-250MHZ/ATTN 10:1 LECROY LOGO/1.2 M/1.4NS RISE/EUROPE				2
829	400	**0	LOOSE PARTS	M9400		PL:M9400	1
869	400	100	COMPLETED BOARD	F9400-1	839400101(1)	PL:F9400-1	1
869	400	200	COMPLETED BOARD	F9400-2	839400200(1)	PL:F9400-2	1
869	400	310	COMPLETED BOARD	F9400-3A	839400310(1)	PL:F9400-3A	2
869	400	400	COMPLETED BOARD	F9400-4	839400400(1)	PL:F9400-4	1
869	400	510	COMPLETED BOARD	F9400A-5	859400500(1)	PL:F9400A-5	1
869	400	700	COMPLETED BOARD	F9400-7	839400700(1)	PL:F9400-7	1
869	400	800	COMPLETED BOARD	F9400-8	839400800(1)	PL:F9400-8	1
869	400	900	COMPLETED BOARD	F9400-9	859400900(1)839400901(1)	PL:F9400-9	1
869	401	200	COMPLETED BOARD	F9401-2	839401200 (1)	PL:F9401-2	1

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MODEL NO F9400-3 COMPLETED BOARD PRINTED 12-Apr-88
ECON 1010 REV DATE 19-Dec-86
MCN 1 MCN DATE 12-Aug-87
FAN HIST. NO 1010 FAN HIST. DATE

LRS PART NO	DESCRIPTION		QTY
207 281 *29	IC MONOLOTHIC ADC TDC1029 DIP-24 CERAMIC/100 MSPS 1029		1
210 *60 *32	IC A/D/A CONVERT HADAC G DIP 32		1
210 *80 202	IC SAMPLE & HOLD HSH202 DIP-24	PL:HSH202	1
480 *33 **1	CABLE CO-AX 30CM SMB-SMC RG316/U PER DWG 9400-H2		1
550 430 106	SCREW CYL HD PHIL M3X6 ZINC PLATED STEEL		4
550 430 112	SCREW CYL HD PHIL M3X12 ZINC PLATED STEEL		2
551 430 100	FLAT WASHER M3 ZINC PLATED STEEL/OD 7MM		4
551 430 400	WASHER SHAKEPROOF M3 ZINC PLATED STEEL/EXTERNAL STAR		2
552 430 100	NUT HEX M3 ZINC PLATED STEEL		4
554 435 **1	SCREW SHEET METAL M3.5 ZINC PLATED STEEL CYL HD/PHILLIPS		2
709 400 301	HEATSINK PER DWG 9400-3-M1		1
759 400 300	DELAY LINE 12.0 NS 9400-3 MECHANICAL & WIRE 593190316(9)		1
839 400 300	SOLDERED BOARD S9400-3 719400303(1)	PL:S9400-3	1

NOTE: 1 PER DWG 9400-3-L1
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MODEL NO S9400-3 SOLDERED BOARD PRINTED 12-Apr-88
ECON 1010 REV DATE 19-Dec-86
MCN 1 MCN DATE 12-Aug-87
FAN HIST. NO 1010 FAN HIST. DATE

LRS PART NO	DESCRIPTION	QTY
102 412 181	CAP CERA DISC 100V 180 PF 2% VIO "N18"	1
103 307 103	CAP CERA MONO 50V .01 UF 20% GEN PURP/LEADS CUT TO 1/2"	89
103 427 104	CAP CERA MONO 100V .1 UF 20% GENERAL PURPOSE	11
103 506 331	CAP CERA MONO 100V 330 PF 10% STABLE	1
146 424 106	CAP MINI ALUM 20% 10 UF 16V/RADIAL LEADS/.06 CTRS/.157X.295	12
146 554 476	CAP MINI ALUM 20% 47 UF 25V/RADIAL LEADS .100 CTRS/ .25X472	3
146 634 106	CAP MINI ALUM 20% 10 UF 35V/RADIAL LEADS/.10 CTRS/.248X.295	2
158 849 **9	CAP VARIABLE .5 - 2.5 PF RED MARK/.040 HI .125 DIA	1
158 849 *10	CAP VARIABLE 1 - 5 PF BLK MARK/.040 HI .125 DIA	1
161 225 101	RES COMP 1/8W 5% 100 OHMS	1
161 225 103	RES COMP 1/8W 5% 10 K	1
161 225 150	RES COMP 1/8W 5% 15 OHMS	2
161 225 220	RES COMP 1/8W 5% 22 OHMS	3
161 225 300	RES COMP 1/8W 5% 30 OHMS	2
161 225 330	RES COMP 1/8W 5% 33 OHMS	3
161 225 430	RES COMP 1/8W 5% 43 OHMS	2
161 225 471	RES COMP 1/8W 5% 470 OHMS	1
161 225 680	RES COMP 1/8W 5% 68 OHMS	2
161 225 820	RES COMP 1/8W 5% 82 OHMS	2
161 225 911	RES CARBON FILM 910 OHMS 1/8W 5%	1
161 335 101	RES COMP 1/4W 5% 100 OHMS	3
161 335 102	RES COMP 1/4W 5% 1 K	2
161 335 103	RES COMP 1/4W 5% 10 K	3
161 335 151	RES COMP 1/4W 5% 150 OHMS	1
161 335 201	RES COMP 1/4W 5% 200 OHMS	1
161 335 202	RES COMP 1/4W 5% 2 K	2
161 335 220	RES COMP 1/4W 5% 22 OHMS	2
161 335 221	RES COMP 1/4W 5% 220 OHMS	1
161 335 222	RES COMP 1/4W 5% 2.2 K	1
161 335 270	RES COMP 1/4W 5% 27 OHMS	2
161 335 272	RES COMP 1/4W 5% 2.7 K	2
161 335 301	RES COMP 1/4W 5% 300 OHMS	2
161 335 331	RES COMP 1/4W 5% 330 OHMS	3
161 335 333	RES COMP 1/4W 5% 33 K	1
161 335 471	RES COMP 1/4W 5% 470 OHMS	4
161 335 473	RES COMP 1/4W 5% 47 K	1
161 335 560	RES COMP 1/4W 5% 56 OHMS	1
161 335 620	RES COMP 1/4W 5% 62 OHMS	1
161 335 750	RES COMP 1/4W 5% 75 OHMS	3
161 335 820	RES COMP 1/4W 5% 82 OHMS	11
161 335 911	RES COMP 1/4W 5% 910 OHMS	1
168 531 281	RES PREC RN55D 68.1 OHMS	1
168 531 305	RES PREC RN55D 121 OHMS	1
168 531 325	RES PREC RN55D 196 OHMS	1
168 531 349	RES PREC RN55D 348 OHMS	1
168 531 357	RES PREC RN55D 422 OHMS	1
168 531 381	RES PREC RN55D 750 OHMS	1

MODEL NO S9400-3 SOLDERED BOARD PRINTED 12-Apr-88
ECON 1010 REV DATE 19-Dec-86
MCN 1 MCN DATE 12-Aug-87
FAN HIST. NO 1010 FAN HIST. DATE

LRS	PART NO	DESCRIPTION	QTY
168	531 425	RES PREC RN55D 2.15 K	1
168	531 439	RES PREC RN55D 3.01 K	1
168	531 553	RES PREC RN55D 46.4 K	1
168	531 585	RES PREC RN55D 100 K	4
181	437 101	RES VARI CERMET 100 OHMS 1/2W 10%	1
181	437 102	RES VARI CERMET 1 K 1/2W 10%	3
181	437 103	RES VARI CERMET 10 K 1/2W 10%	2
181	437 201	RES VARI CERMET 200 OHMS 1/2W 10%	1
181	437 500	RES VARI CERMET 50 OHMS 1/2W 10%	1
181	437 501	RES VARI CERMET 500 OHMS 1/2W 10%	2
190	*42 221	RESISTOR NETWORK 220 OHMS SIP-10	1
190	*42 471	RESISTOR NETWORK 470 OHMS SIP-10	2
190	*42 820	RESISTOR NETWORK 82 OHMS SIP-10	1
190	642 471	RESISTOR NETWORK 470 OHMS SIP-6	2
190	642 820	RESISTOR NETWORK 82 OHMS SIP-6	1
190	842 471	RESISTOR NETWORK 470 OHMS SIP-8	1
190	842 820	RESISTOR NETWORK 82 OHMS SIP-8	1
200	*31 *28	IC 2-IN NAND GT SN74LS00N DIP-14	1
200	*31 *46	IC HEX INVERTER SN74LS04N DIP-14	1
200	*31 *57	IC 3-IN POS NOR SN74LS27N TRIPLE PKG/DIP-14	1
200	*31 *86	IC 2-IN AND GAT SN74LS08N QUAD PKG/DIP-14	1
200	*32 *10	IC 2-IN NAND BUF 74LS38PC QUAD PKG/OP COLL/DIP-14	1
200	*41 *27	IC QUAD SEL/MP SN74LS157N 2-LINE-TO-1-LINE/DIP-16	3
200	*41 *62	IC DEC/DEMULTP SN74LS138N DIP-16	1
200	*71 **1	IC 8 X BUFFER SN74LS240 MOLDED DIP-20 TRI-STATE OUTPUTS	10
200	340 113	IC EXCL-OR GATE MC10H113 DIP-16/QUAD PKG 10H113	2
200	340 378	IC PARALLEL D REG 74F378 DIP-16/6-BIT/BUFF COMM EN 74F378	4
200	341 106	IC 4-3-3 IN NOR 10H106 DIP-16/ECL/TRIPLE PKG 10H106	1
200	344 101	IC QUAD OR/NOR 10H101P DIP-16/MECL 10KH	1
200	344 104	IC QUAD 2-IN NAND 10H104 DIP 16/MECL 10KH	1
200	371 374	IC D-TYP FLOP 74F374PC DIP-20/OCTAL PKG/3-STATE	14
204	*22 **2	IC HEX D M-S F-F MC10176L DIP-16 CERAMIC	5
204	*42 **8	IC QUAD TRANSL MC10125P MECL-TO-MTTL/DIP-16	5
204	*42 *11	IC LINE RECEIVER MC10116P TRIPLE PKG/DIP-16	1
204	*42 141	IC SHIFT REGISTER MC10141 DIP-16/4-BIT/UNIVERSAL 10141	1
204	*43 231	IC TYPE D FLOP MC10231P DIP-16/DUAL PKG	5
205	280 116	IC 2048X8 RAM HM6116LP-2 DIP 24	16
207	444 116	IC TRIPL LINE RCVR 10H116 DIP-16/MECL 10KH	1
208	122 **2	IC VOLT REG POS UA7805 5V OUTPUT TO-220 PACKAGE	1
208	122 337	IC ADJ -VOLT REG LM337T TO-220/OUTPUT -1.2V TO -37V	1
208	123 **2	IC +12 VOLT REG LM340T-12 TO-220 PKG	1
208	124 **2	IC VOLT REG -5V UA7905UC TO -220 PKG	1
208	124 **3	IC VOLT REG NEG LM320T-12 T0-220	1
208	130 324	IC QUAD OP AMP LM324 DIP-14	1
230	110 **5	DIODE SWITCHING 1N4448	1
235	*10 **5	DIODE RECTIFIER 1N4005	3
270	170 **1	TRANSISTOR NPN 2N5770 TO-92	1

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MODEL NO S9400-3              SOLDERED BOARD                  PRINTED  12-Apr-88
ECON  1010                                                    REV DATE 19-Dec-86
MCN     1                                                     MCN DATE 12-Aug-87
FAN HIST. NO        1010              FAN HIST. DATE
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LRS PART NO        DESCRIPTION                                                QTY

271 170 *90 TRANSISTOR NPN UHF  BFR90 CASE W56 (D.A.T.A.)                      2
275 170 **2 TRANSISTOR PNP     2N5771 TO-92                                    3
290 110 *16 DELAY LINE        16 N-SEC SIP                                     1
300 *10 **1 BEAD SHIELDING    FERRITE                                          2
300 *50 **1 CHOKE FERRITE SINGLE LEAD                                          4
405 760 **5 SOCKET SPRING SINGLE WIRE 5M REEL/KAPTON/FOR MANUAL INSERTION     80
454 310 **2 HDR DIP SOLD TO PC BD   2 .100 CTRS/STRAIGHT/BREAKAWAY STOCK      11
454 314 *16 HDR DIP SOLD TO MALE   16 .100 CTRS/STRAIGHT/NO EARS               1
454 370 *12 HEADER 2-SIDED FEMALE  12 .100 CTRS/SINGLE ROW                     1
454 610 *96 HDR DIP SOLD TO MALE   96 DIN 41612 RT ANGLE                       1
585 252 354 RIVET HOLLOW       2,5X9MM BRASS                                   2
719 400 303 PC BD PREASS'Y      9400-3                                         1


NOTE:  1       PER DWG 9400-3-L1
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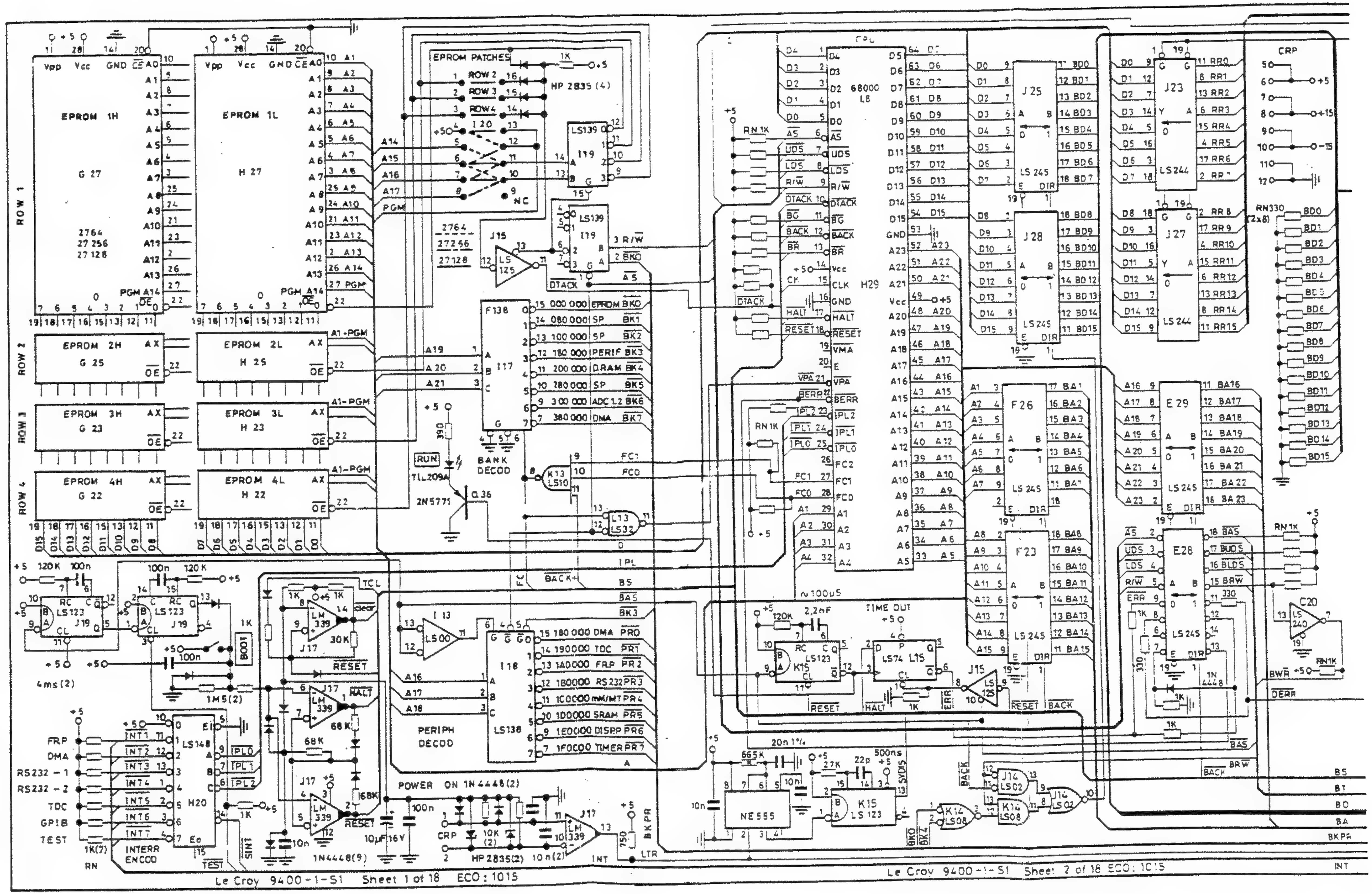
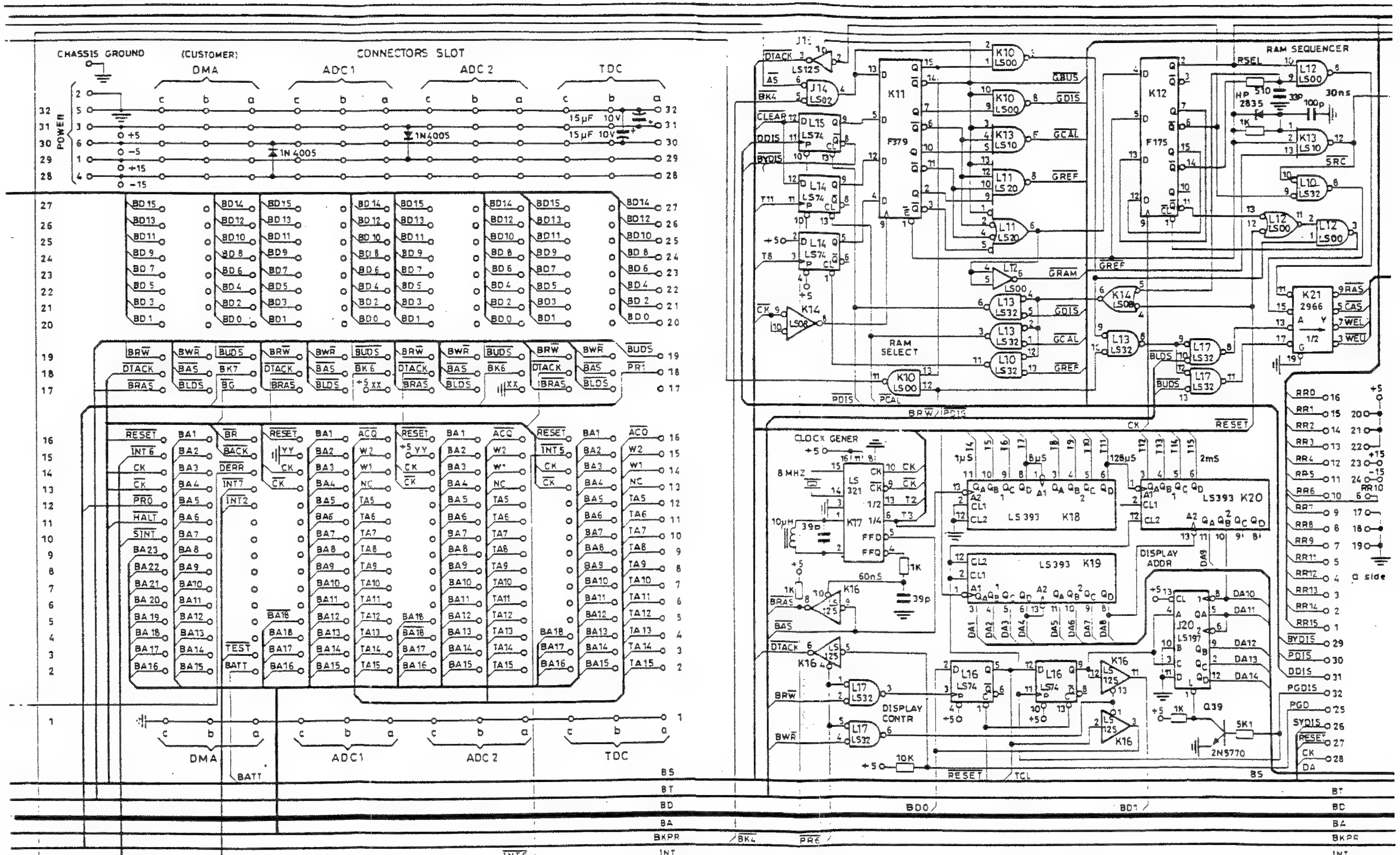
CHAPTER 7

COMPLETE SCHEMATICS FOR THE 9400 AND 9400A

The schematics are are presented in the numerical order of the boards.

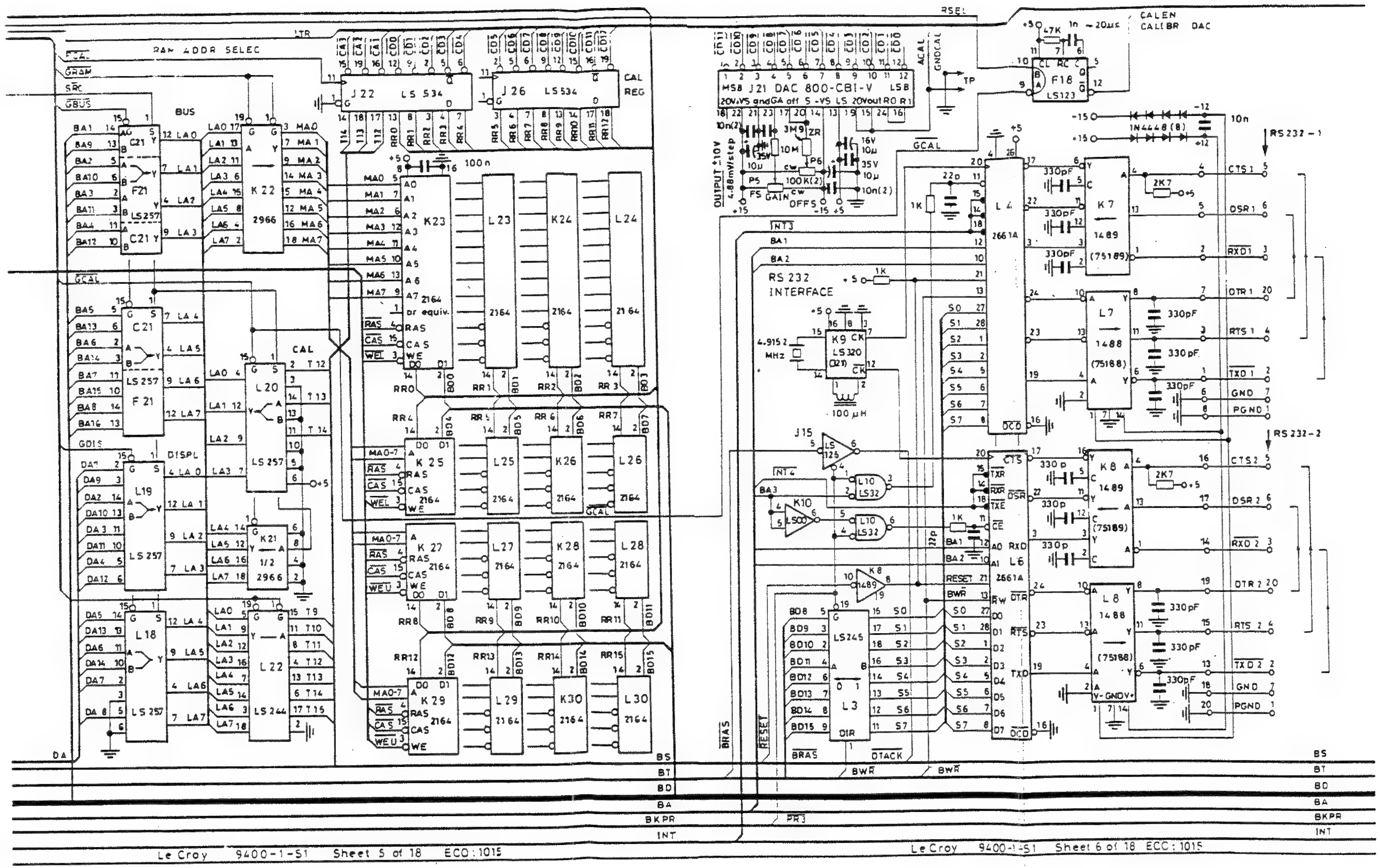


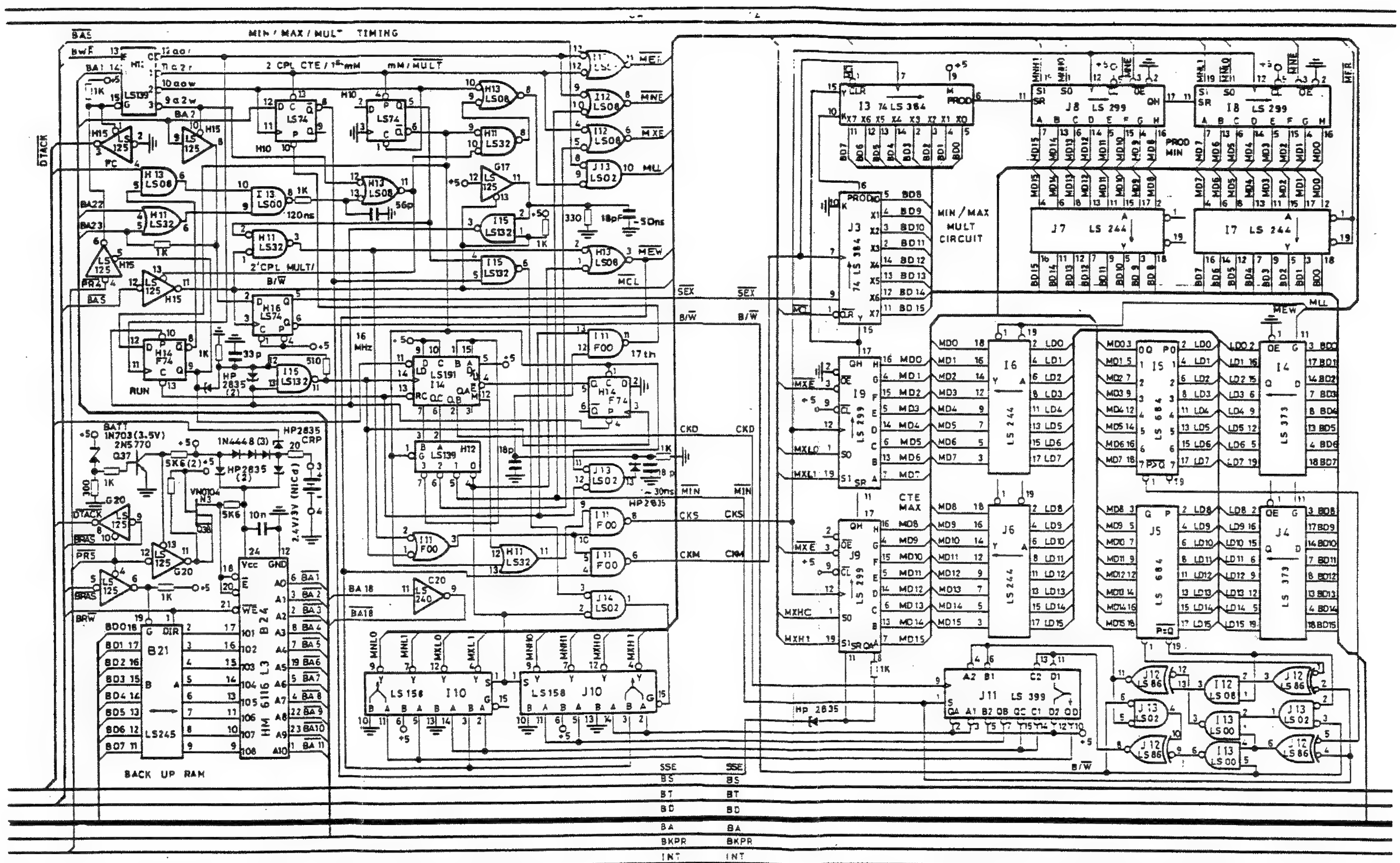
Le Croy 9400-1-S1 Sheet 1 of 18 ECO: 1015
Le Croy 9400-1-S1 Sheet 2 of 18 ECO: 1015

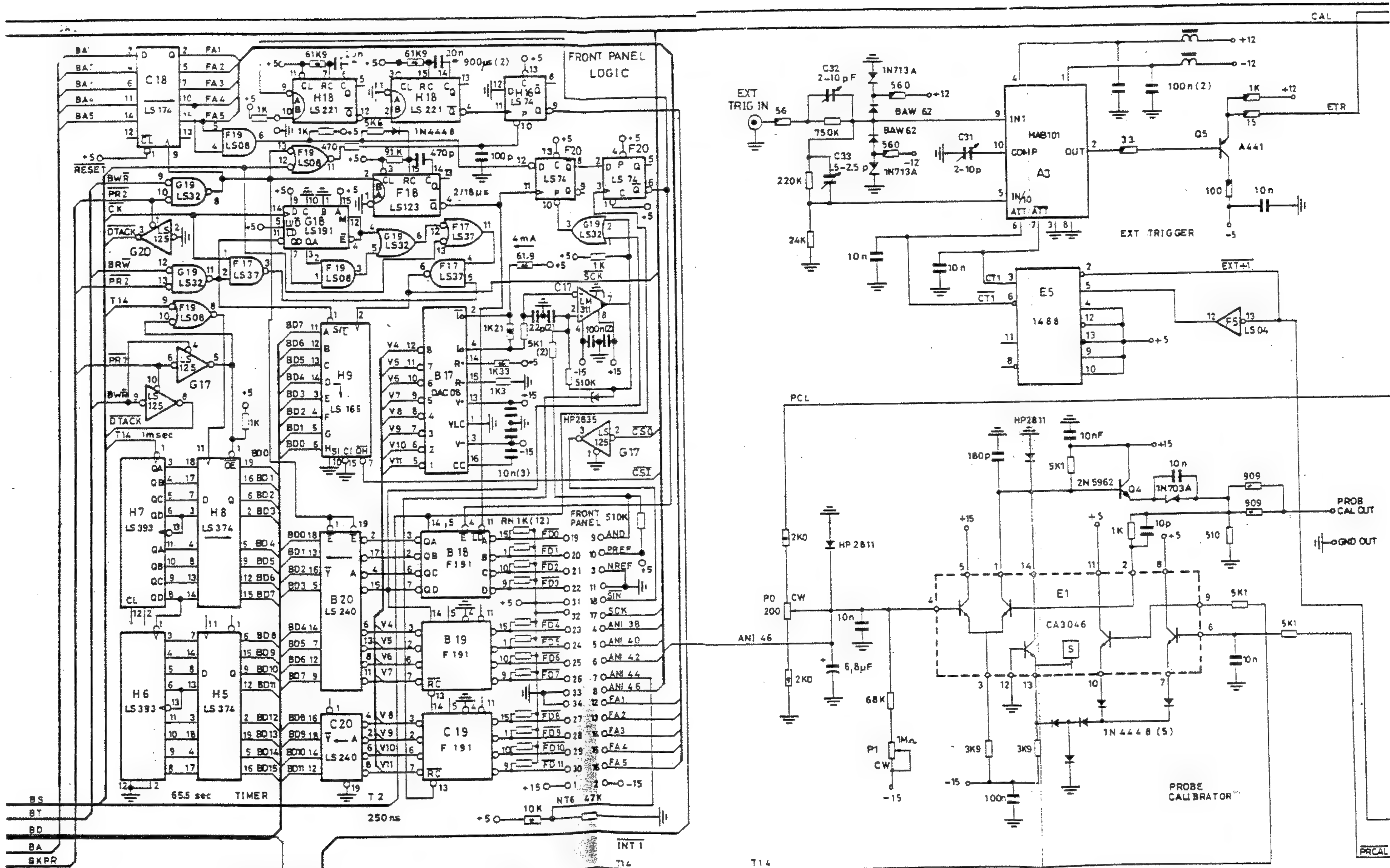


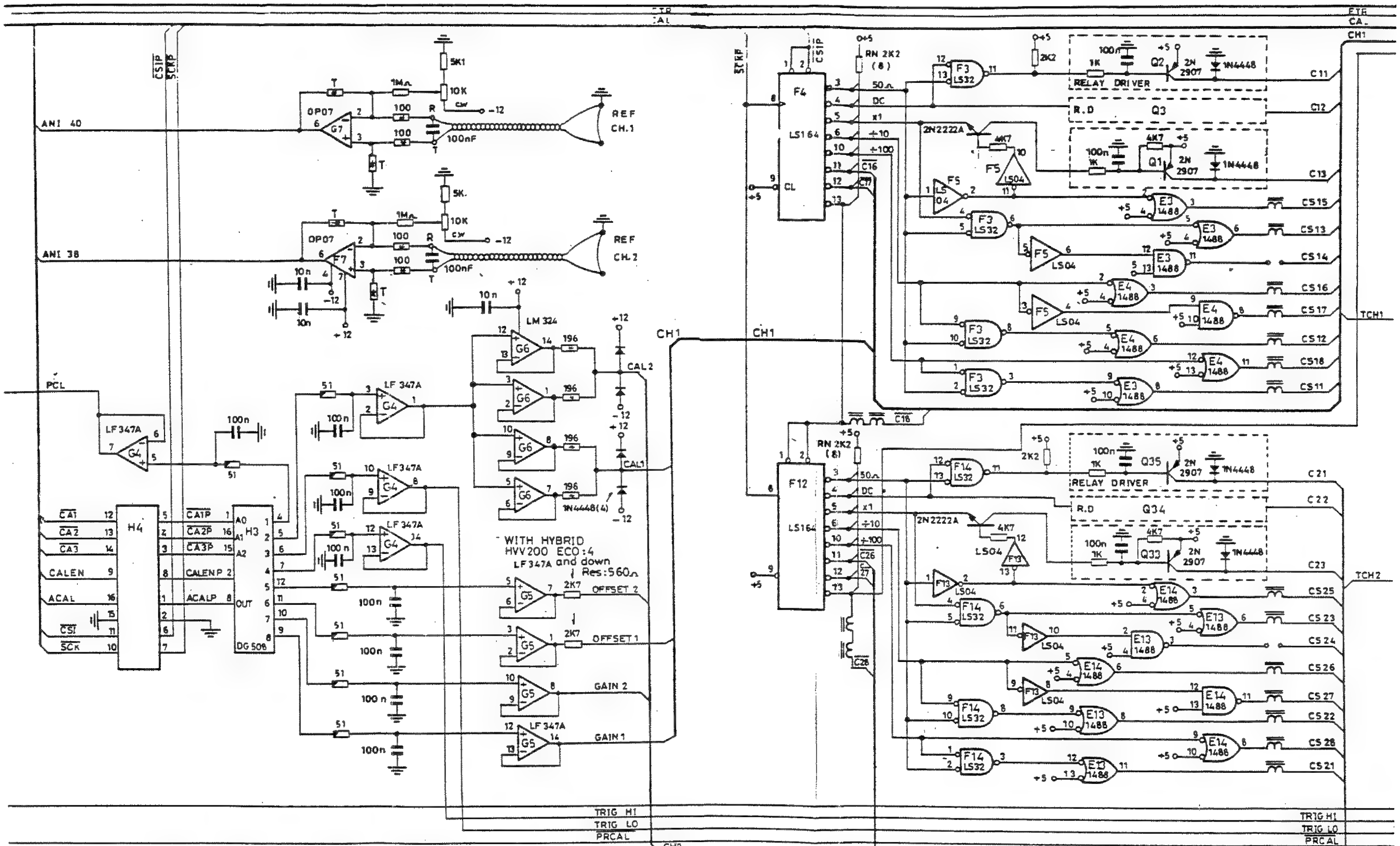
LeCroy 9400-1-S1 Sheet 3 of 18 ECO: 1015

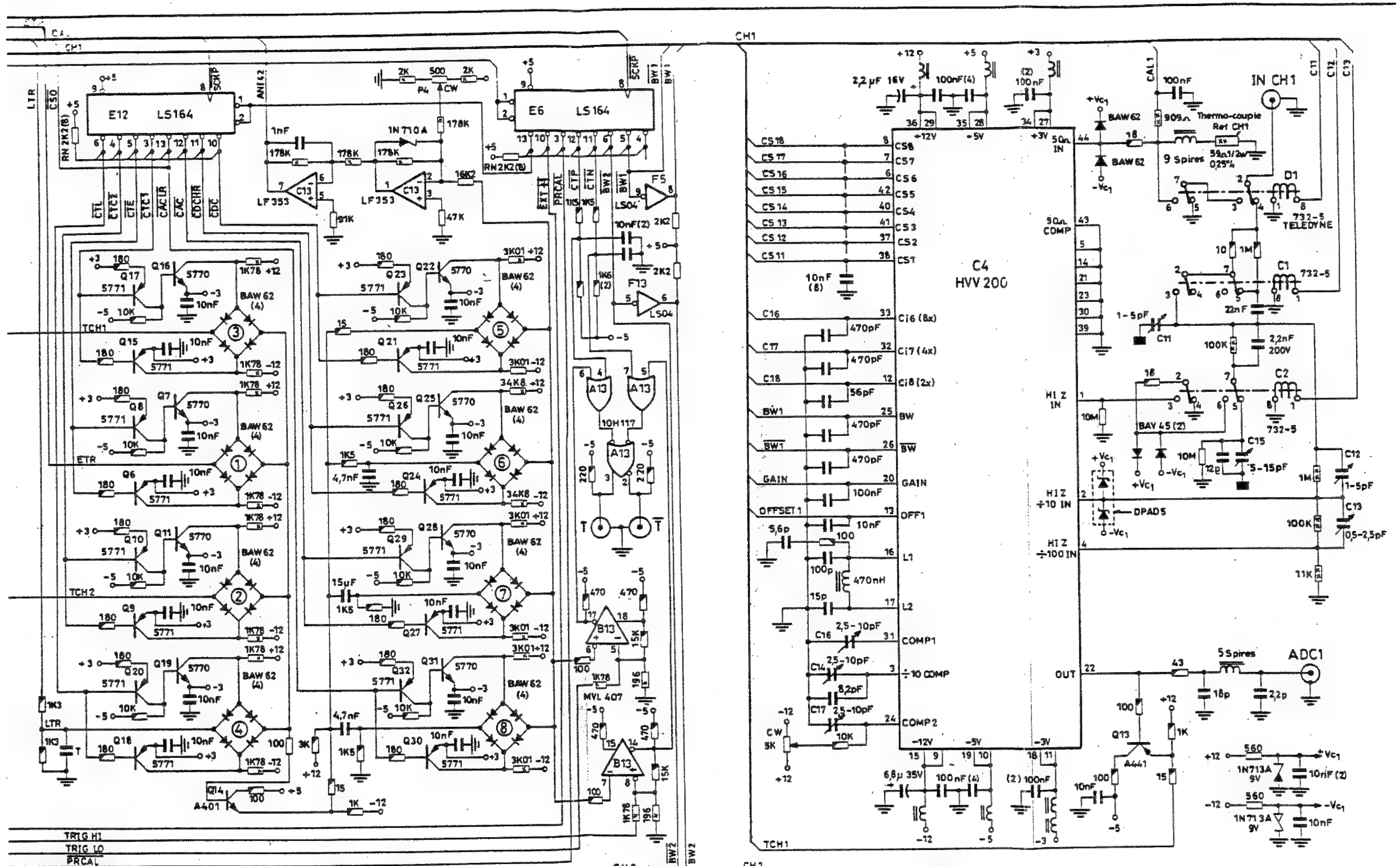
LeCroy 9400-1-S1 Sheet 4 of 18 ECO: 1015


RAW ADDR SELEC
BUS
CAL
DISPL
CAL REG
RSEL
CALEN
CALIBR DAC
MSB J21 DAC 800-CBI-V LSB
OUTPUT ±10V 4.88mV/step
RS 232 INTERFACE
RS 232 - 1
RS 232 - 2
BS
BT
BD
BA
BKPR
INT
Le Croy 9400-1-S1 Sheet 5 of 18 ECO: 1015
Le Croy 9400-1-S1 Sheet 6 of 18 ECO: 1015


MIN / MAX / MULT TIMING
MIN / MAX MULT CIRCUIT
CTE MAX
BACK UP RAM

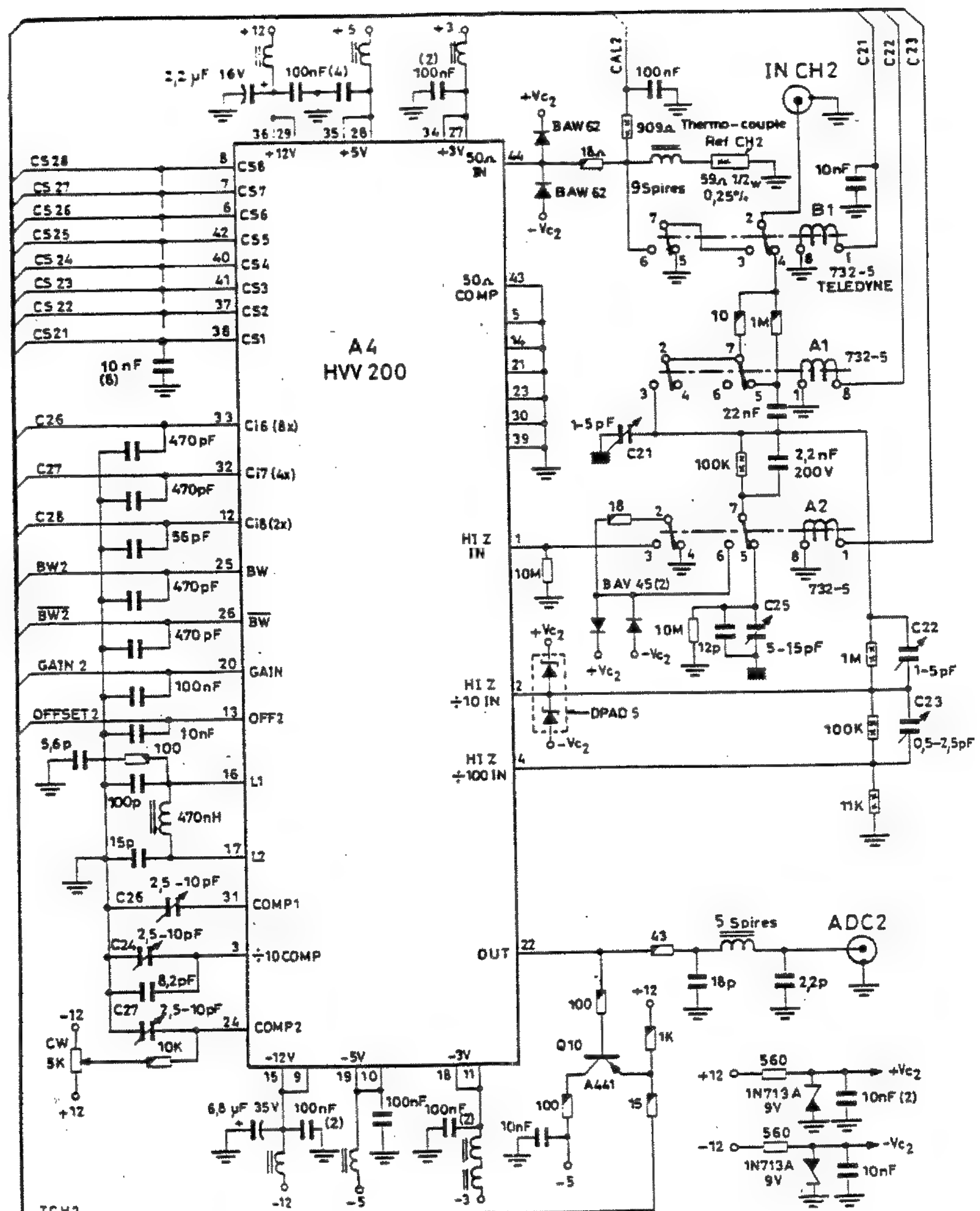

FRONT PANEL LOGIC
EXT TRIG IN
EXT TRIGGER
PROBE CALIBRATOR
PROB CAL OUT
GND OUT
TIMER
65.5 sec
250 ns
T14 1msec
CAL
ETR
PRCAL
PCL
ANI 46
INT 1
BS
BT
BD
BA
BKPR
INT
RESET


ANI 40
ANI 38
PCL
REF CH.1
REF CH.2
OP07
LF347A
LM324
DG508
LS164
LS32
LS04
1488
2N2222A
2N 2907
1N4448
RELAY DRIVER
R.D
CAL 2
CAL1
OFFSET 2
OFFSET 1
GAIN 2
GAIN 1
WITH HYBRID
HVV200 ECO:4
LF347A and down
Res: 560Ω
CH1
CH2
TCH1
TCH2
TRIG HI
TRIG LO
PRCAL
CALEN
ACAL
CALENP 2
ACALP

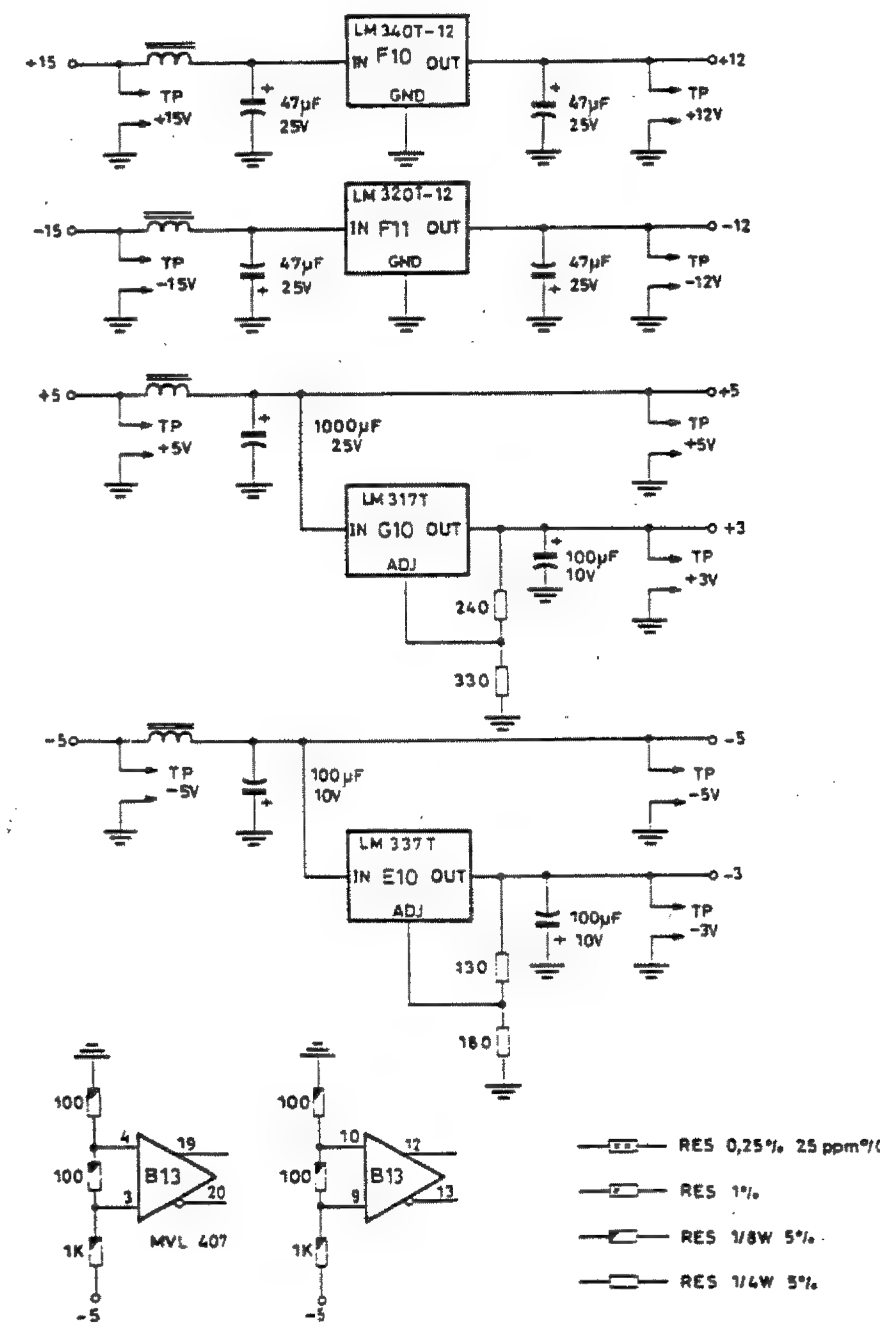


LeCroy 9400-1-S1 Sheet 13 of 18 ECO: 1015

LeCroy 9400-1-S1 Sheet 14 of 18 ECO: 1015



LeCroy 9400-1-S1 Sheet 15 of 18 ECO: 1015



LeCroy 9400-1-S1 Sheet 16 of 18 ECO: 1015

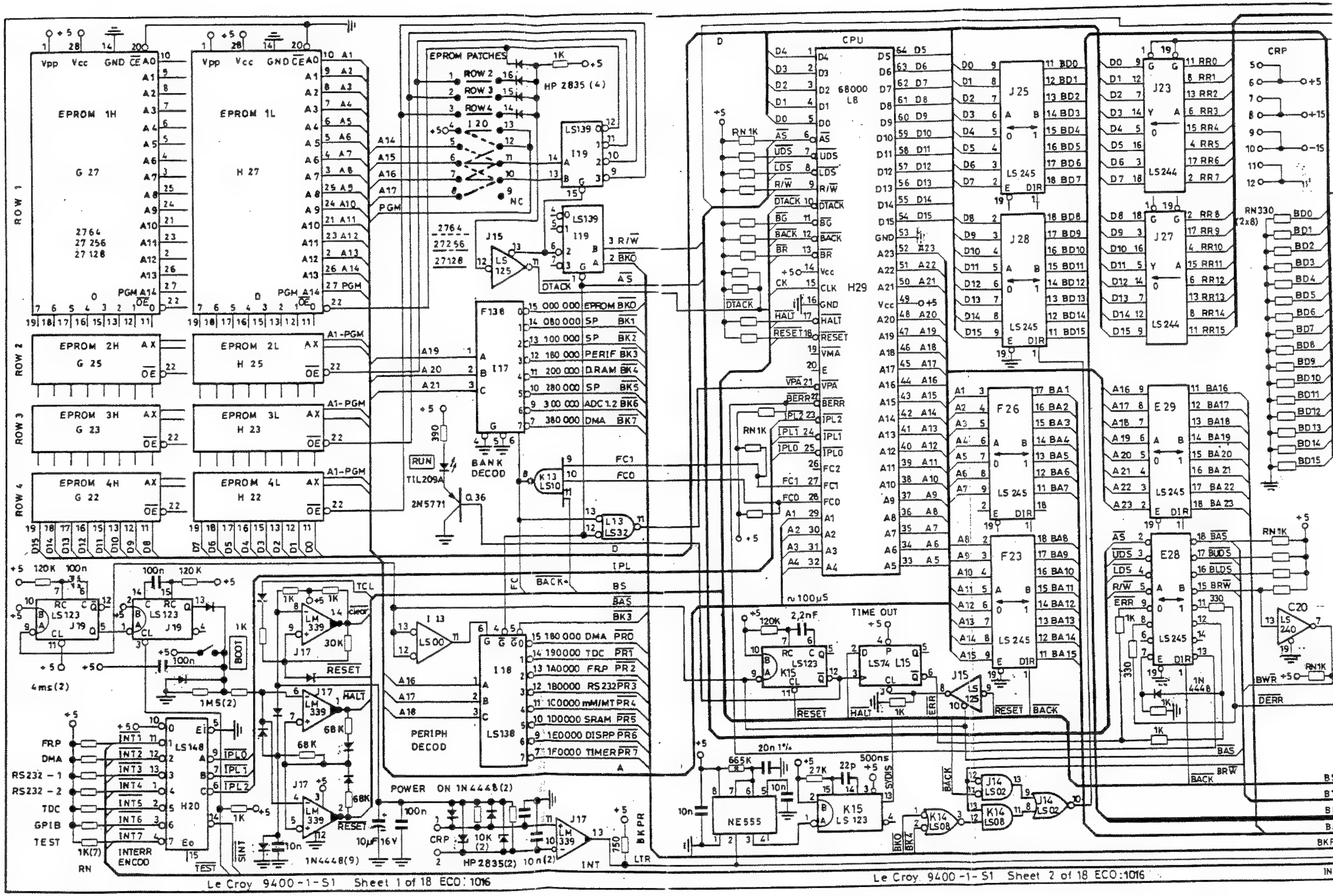
LeCroy parts	IC	Designation	-5	+5	+12	GND	-12
200 012 001	MC 14 89 L	K7,K8		14		7	
200 012 002	MC 14 88 L	L7,L8 E3,E4,E5,E13,E14			14	7	1
200 031 028	74 LS 00 N	I13,K10,L12		14		7	
200 031 046	74 LS 04 N	F5,F13		14		7	
200 031 047	74 LS 10 N	K13		14		7	
200 031 048	74 LS 20 N	L11		14		7	
200 031 049	74 LS 74 N	H10,H16,L14,L15,L16		14		7	
200 031 051	74 LS 02 N	J13,J14		14		7	
200 031 055	74 LS 164 N	E6,E12,F4,F12		14		7	
200 031 066	74 LS 132 N	I15		14		7	
200 031 073	74 LS 32 N	F3,F14,G19,H11,L10,L13,L17		14		7	
200 031 074	74 LS 37 N	F17		14		7	
200 031 086	74 LS 08 N	F19,H13,I12,K14		14		7	
200 031 089	74 LS 125 N	G17,G20,H15,J15,K16		14		7	
200 031 097	74 LS 197 N	J20		14		7	
200 031 101	74 LS 393 N	H6,H7,K18,K19,K20		14		7	
200 031 106	74 LS 86 N	J12		14		7	
200 031 320	74 LS 320	K9		16		8	
200 041 017	74 LS 112 N	F20		16		8	
200 041 033	74 LS 174 N	C18		16		8	
200 041 039	74 LS 221 N	H18		16		8	
200 041 042	74 LS 191 N	G18,I14		16		8	
200 041 044	74 LS 123 N	F18,J19,K15		16		8	
200 041 056	74 LS 165 N	H9		16		8	
200 041 062	74 LS 138 N	I18		16		8	
200 041 067	74 LS 148 N	H20		16		8	
200 041 068	74 LS 158 N	I10,J10		16		8	
200 041 070	74 LS 257 AN	C21,F21,L18,L19,L20		16		8	
200 041 139	74 LS 139 N	H12,I19		16		8	
200 071 001	74 LS 240	B20,C20		20		10	
200 071 003	74 LS 374	H5,H8		20		10	
200 071 007	74 LS 244 N	I6,I7,J6,J7,J23,J27,L22		20		10	
200 071 245	74 LS 245 N	B21,E28,E29,F23,F26,J25,J28,L3		20		10	
200 071 299	74 LS 299 N	I8,I9,J9		20		10	
200 071 373	74 LS 373 N	I4,J4		20		10	
200 071 534	74 LS 534	J22,J26		20		10	
200 072 966	AM 29 66	K21,K22		20		10	
200 330 000	74 F 00	I11		14		7	
200 340 074	74 F 74	H14		14		7	
200 340 117	MC 10 H 117	A13	8			1,16	
200 340 138	74 F 138	I17		16		8	
200 340 379	74 F 379	K11		16		8	
200 341 175	74 F 175	K12		16		8	
200 440 191	74 F 191	B18,B19,C19		16		8	
200 540 384	74 LS 384	I3,J3		16		8	
200 570 684	74 LS 684	I5,J5		20		10	
205 240 264	RAM 41 64-15	K23,K24,K25,K26,K27,K28,K29,K30 L23,L24,L25,L26,L27,L28,L29,L30		8		16	
205 280 116	HM 611 GLP-2	B24				12	

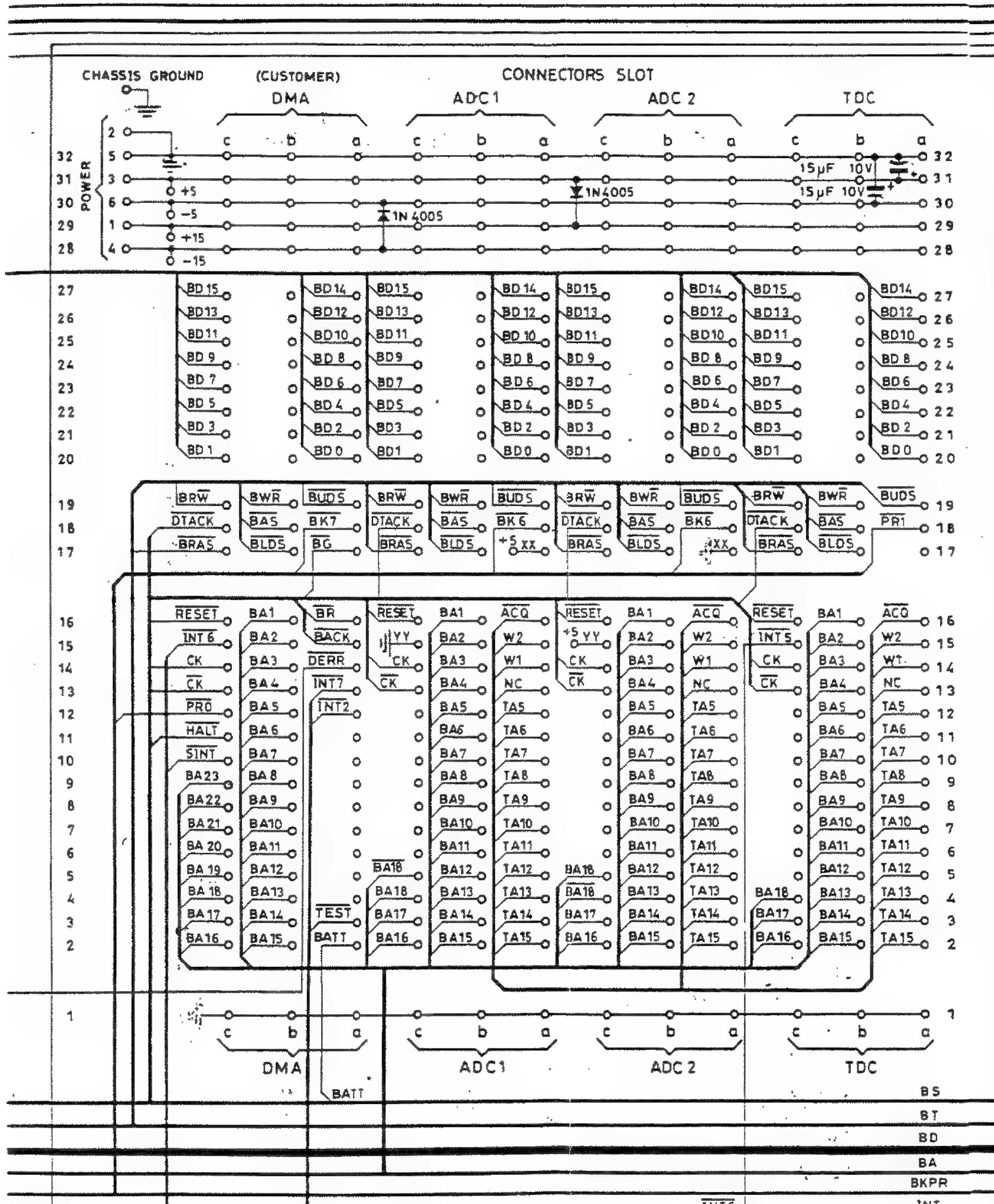
LeCroy 9400-1-S1 Sheet 17 of 18 ECO: 1016

LeCroy parts	IC	Designation	+3	-3	-5	+5	+12	GND	+15	-15	-12
206 042 508	06 508 C J	H 3						14	13	3	
207 280 800	DAC 800	J 21				13		21	22	14	
207 340 399	74 LS 399 N	J 11				16		8			
208 011 008	LM 311 N	C 17						1	8	4	
208 031 010	LM 339 N	J 17 F 17			12	3 3	12				
208 033 001	CA 30 46	E 1				8-11		12	5		
208 041 001	DAC-08 EQ	B 17						1	13	3	
208 110 353	LF 353 N	C 13							8	4	
208 122 337	LM 337 N	E 10									
208 123 002	LM 340 T-12	F 10									
208 130 324	LM 324	G 6					4				11
208 130 347	LF 347	G 4, G 5					4				11
208 570 317	LM 317	G 10									
208 124 003	LM 320T-12	F 11									
208 740 321	74 LS 321	K 17				16		8			
225 070 407	MUL 407	B 13			11	2		1,16			
227 391 068	68 000 L 8	N 29						16,53			
227 762 661	2661	L 4, L 6				26		4,16			
210 440 200	HVV 200	A 4, C 4	27 34	11 18	10 19	28 35	29 36	5,14,21 23,30,39			9,15
220 010 101	HAB 101	A 3					4	3,8			1
208 011 004	NE 555					8		1			

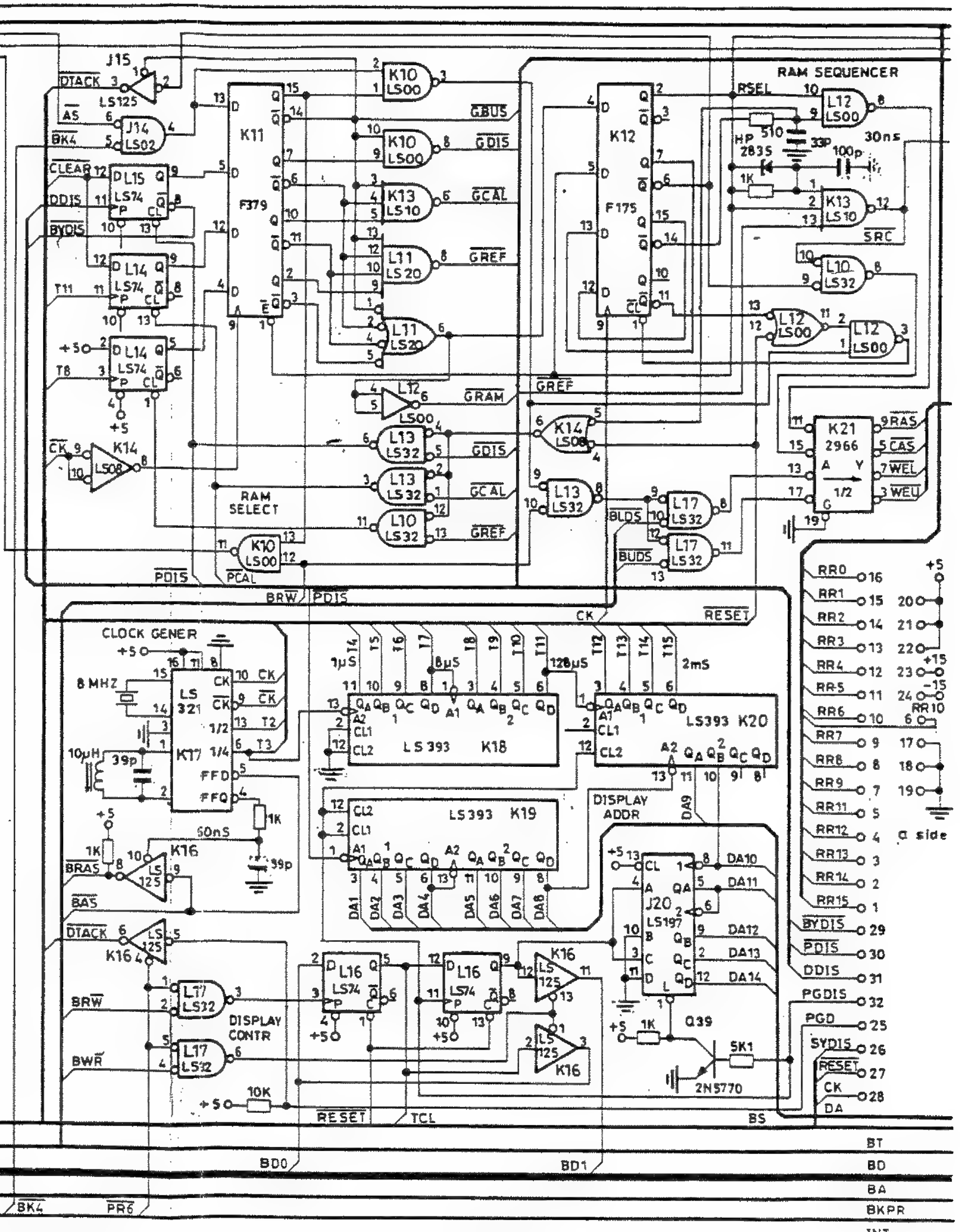
LeCroy RESEARCH SYSTEMS

DRAWN BY/DATE P_PERRIN 19.12.85	MODEL 9400-1 MOTHER CARD SCHEMA
CHKD BY/DATE B-M J-F-G	
APPROVED BY/DATE 05-02-87	DWG NO: 9400-1-S1 SIZE
SCALE 1/1	SH. 18 OF 18 ECO NO. 1016 ENG. REV. APP.

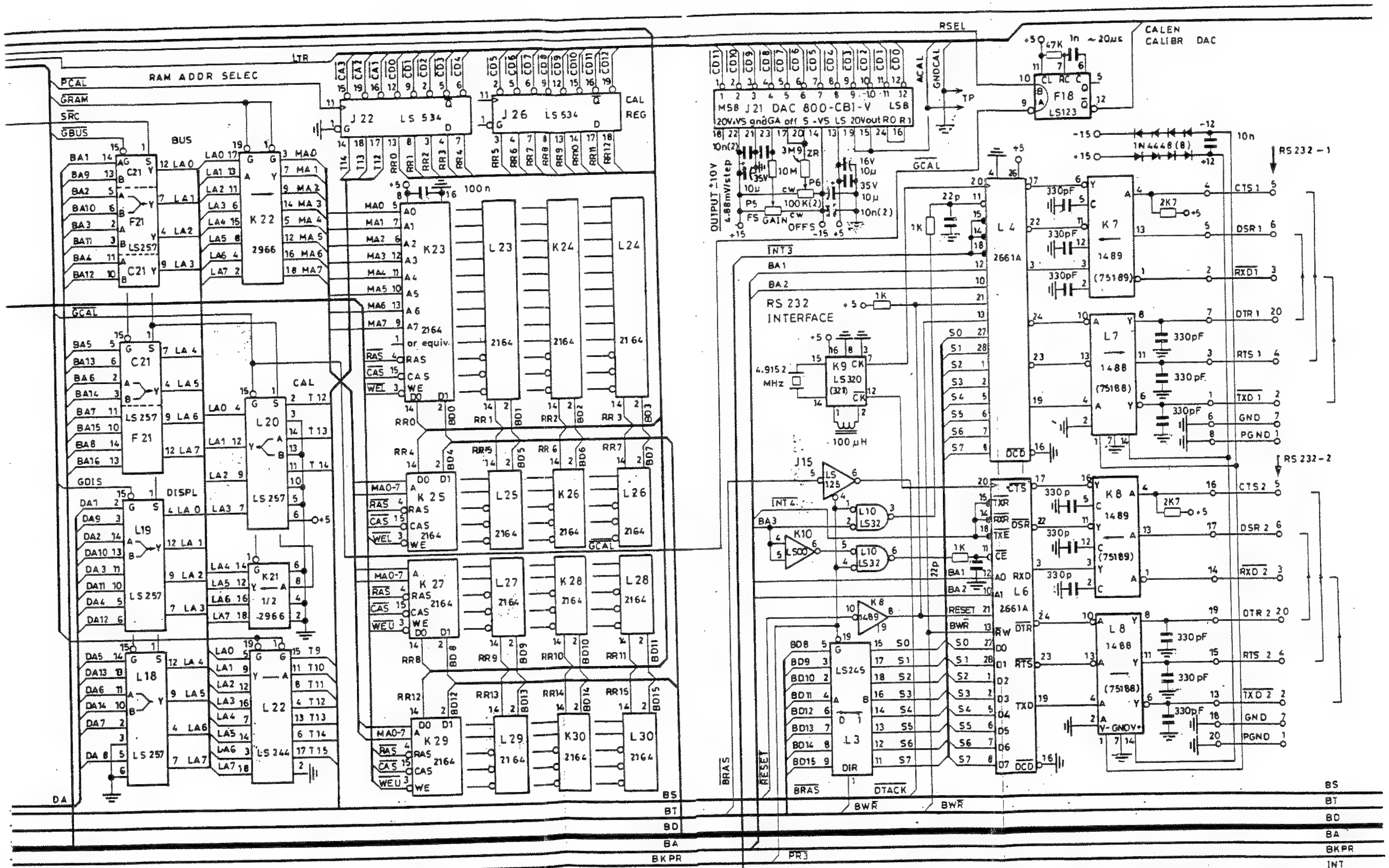

CPU
68000 L8
H29
EPROM 1H
G 27
EPROM 1L
H 27
EPROM 2H
G 25
EPROM 2L
H 25
EPROM 3H
G 23
EPROM 3L
H 23
EPROM 4H
G 22
EPROM 4L
H 22
ROW 1
ROW 2
ROW 3
ROW 4
2764
27256
27128
EPROM PATCHES
HP 2835 (4)
BANK DECOD
PERIPH DECOD
INTERR ENCOD
POWER ON 1N4448(2)
TIME OUT
CRP
RUN
TIL209A
2N5771
NE555
Le Croy 9400-1-S1 Sheet 1 of 18 ECO: 1016
Le Croy 9400-1-S1 Sheet 2 of 18 ECO:1016



Le Croy 9400-1-S1 Sheet 3 of 18 ECO: 1016

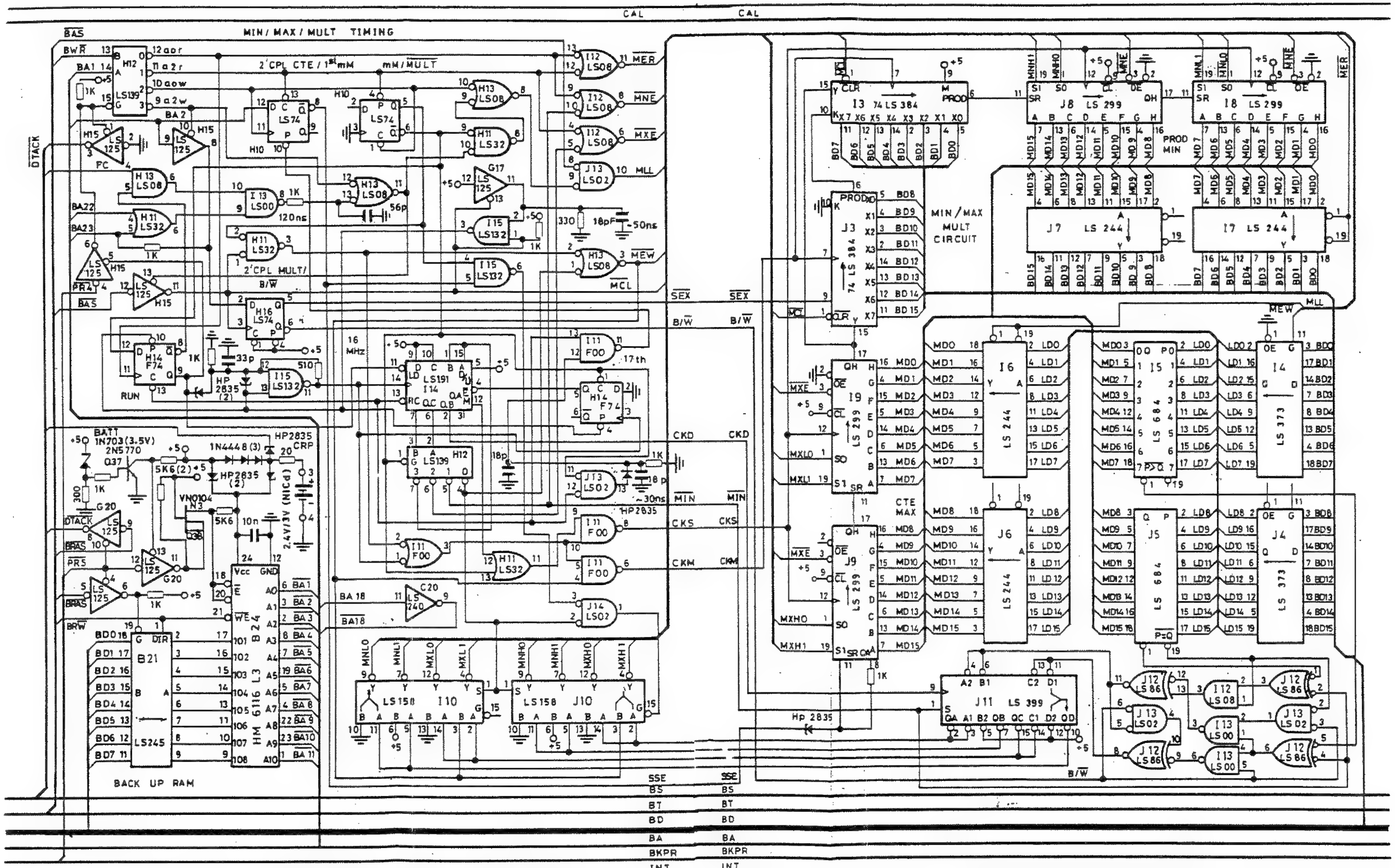


Le Croy 9400-1-S1 Sheet 4 of 18 ECO: 1015



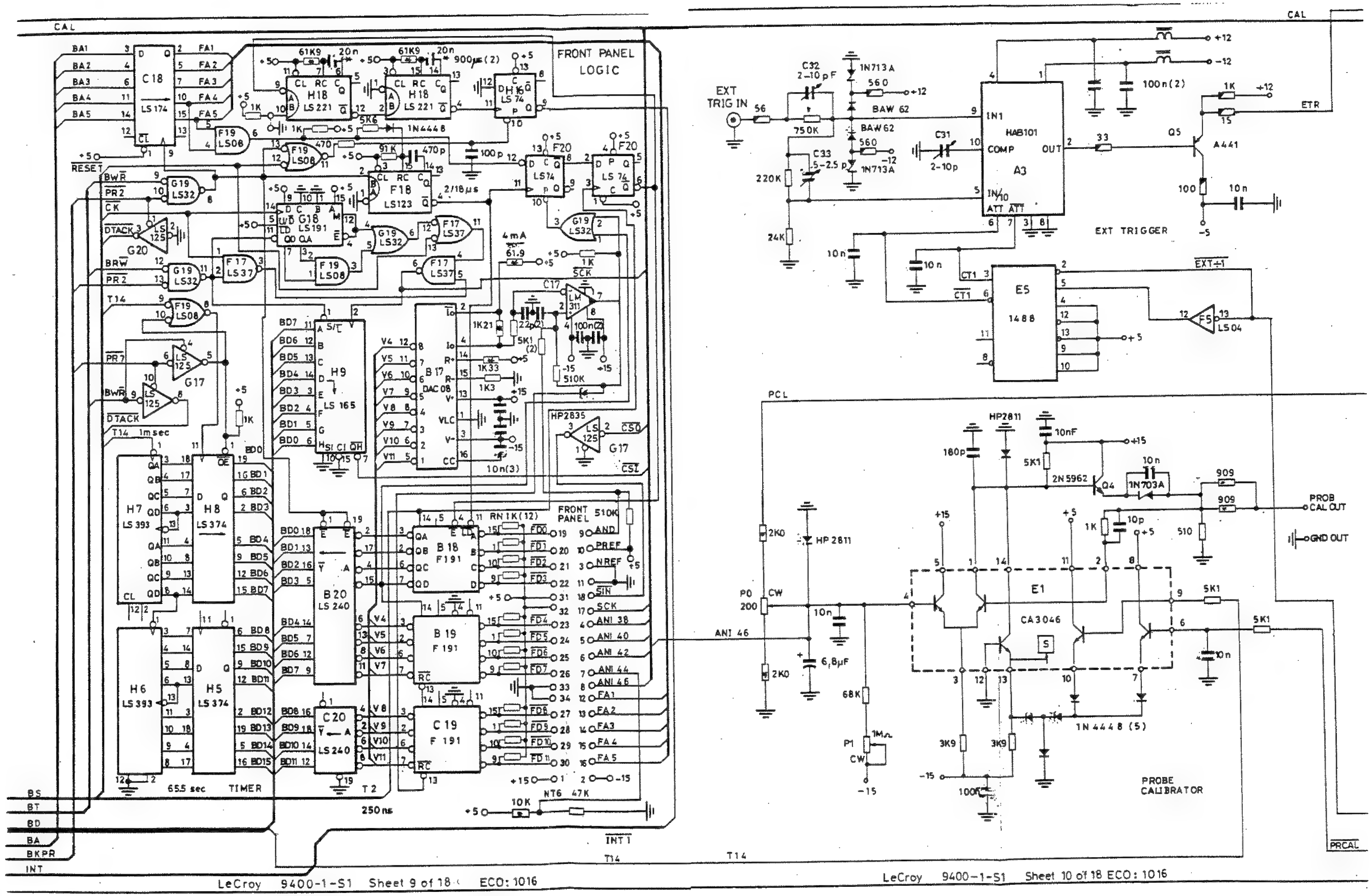
Le Croy 9400-1-S1 Sheet 5 of 18 ECO:1016

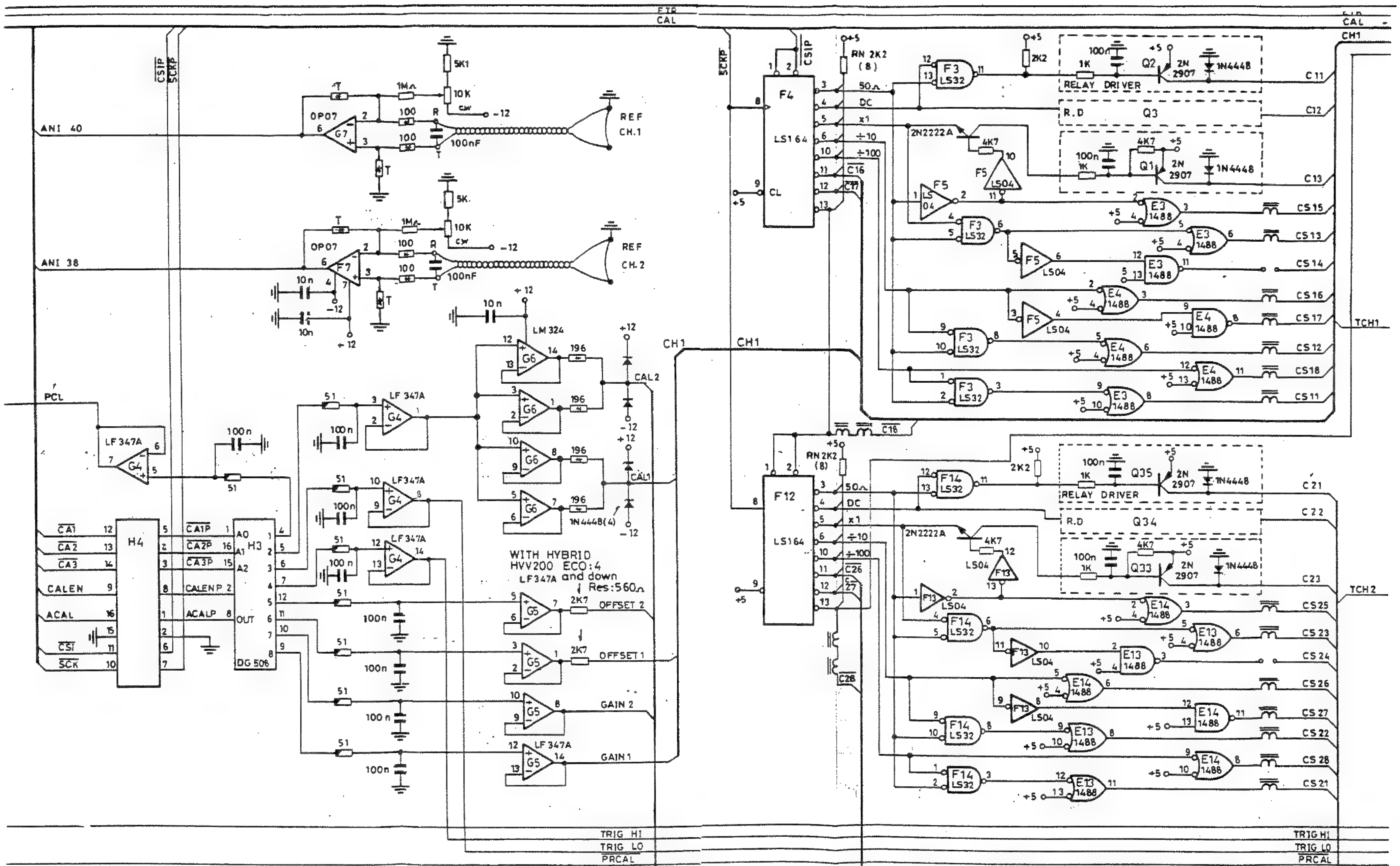
Le Croy 9400-1-S1 Sheet 6 of 18 ECO: 1016



LeCroy 9400-1-S1 Sheet 7 of 18 ECO: 1016

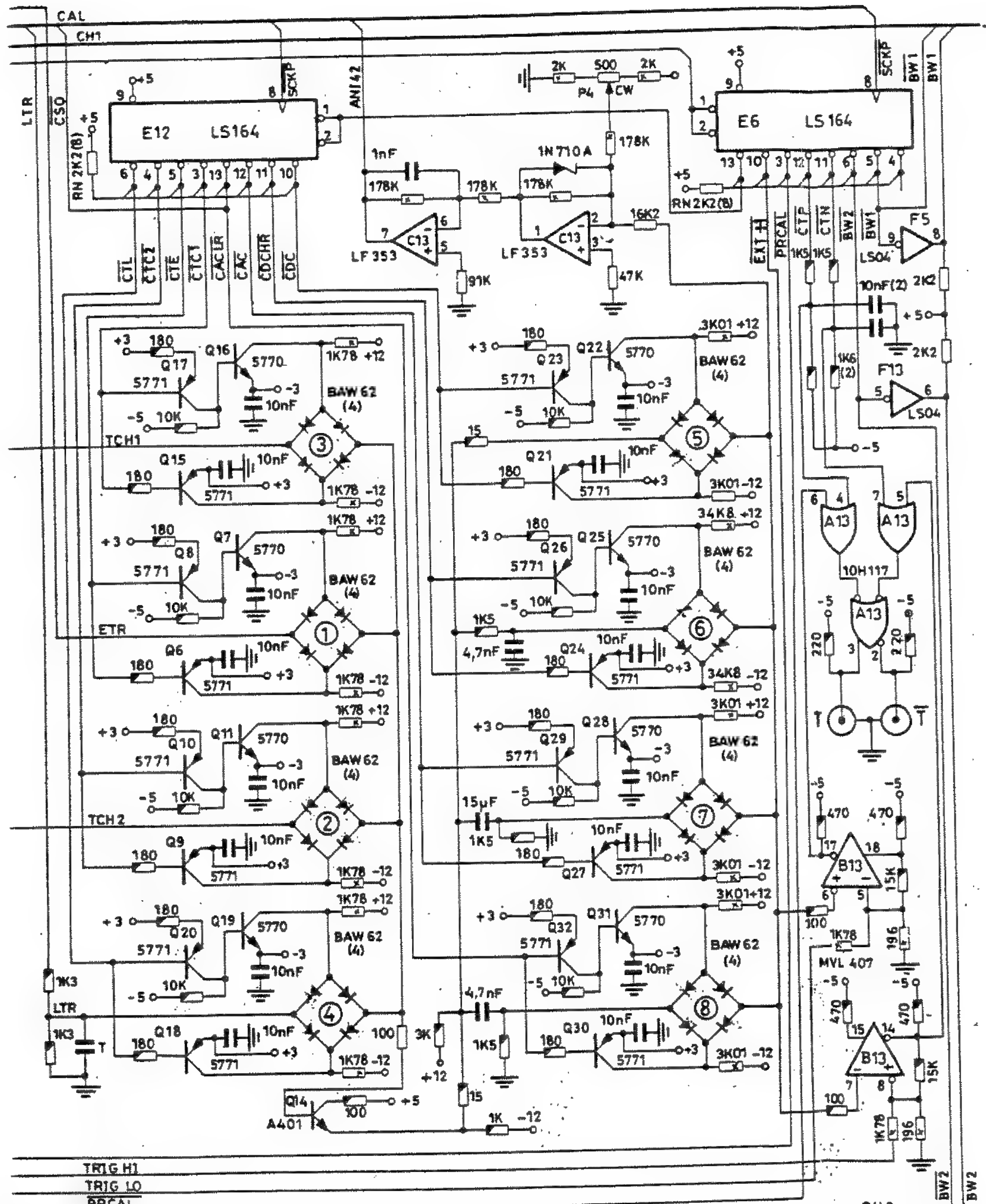
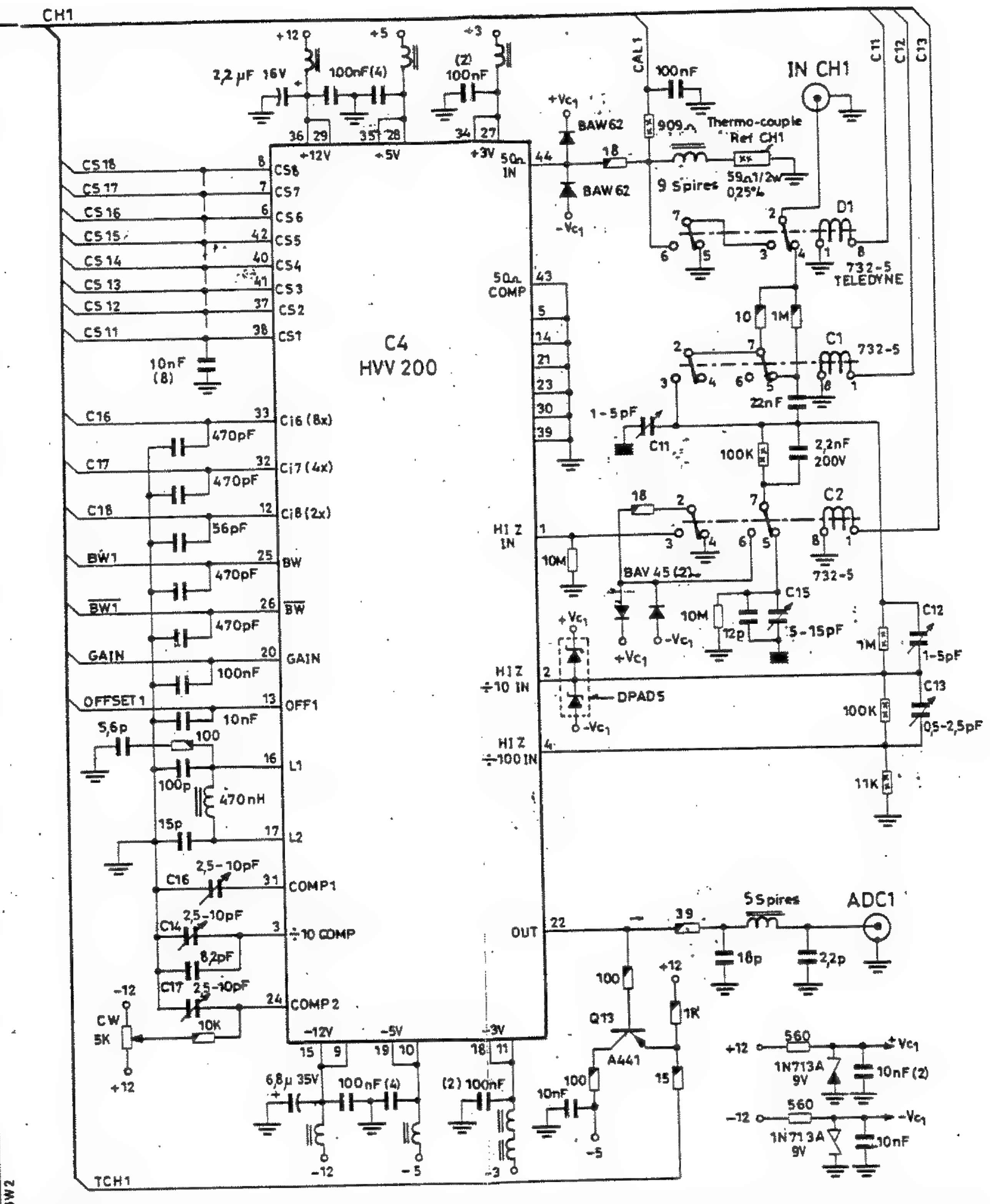
LeCroy 9400-1-S1 Sheet 8 of 18 ECO: 1016

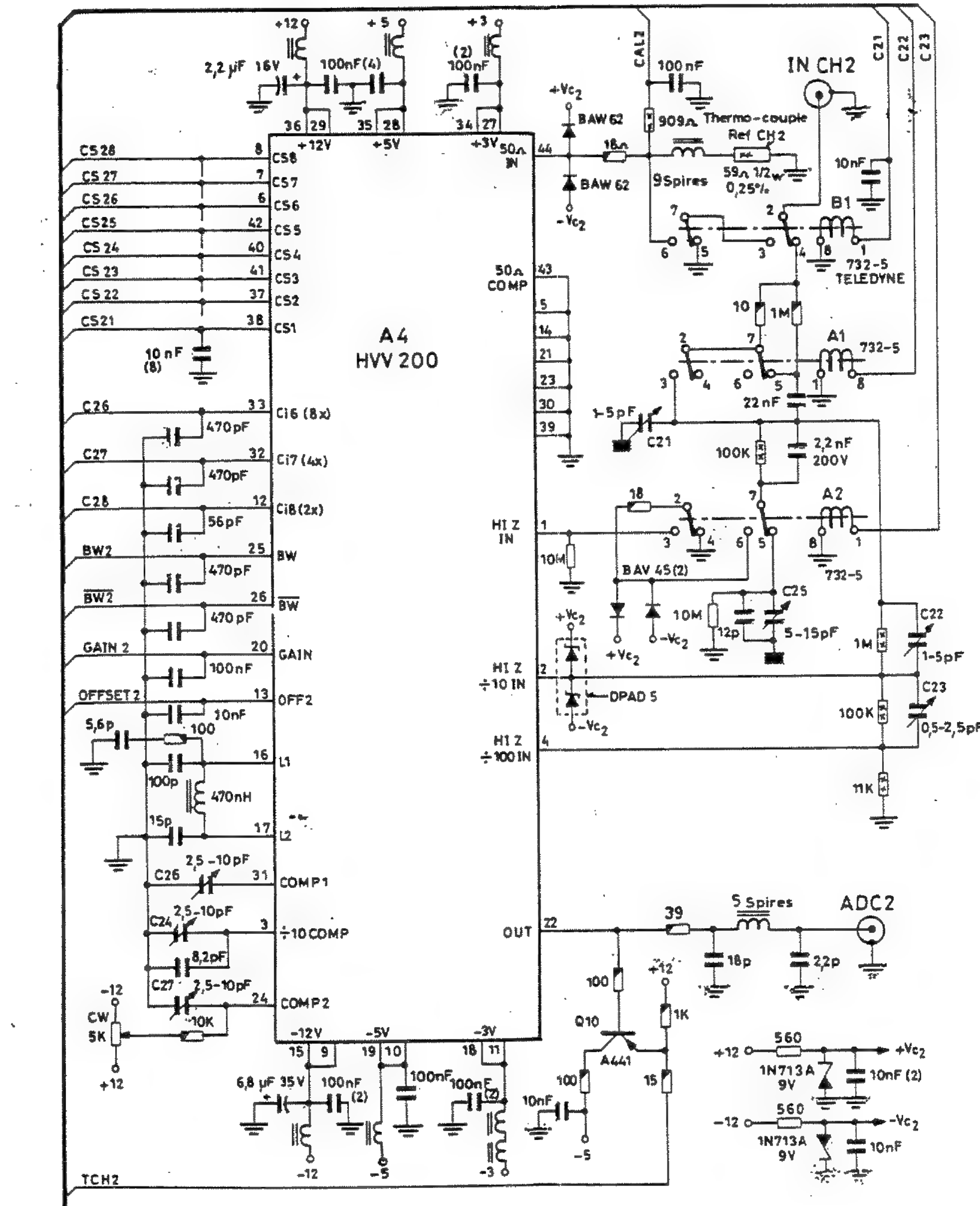

FRONT PANEL LOGIC
EXT TRIGGER
PROBE CALIBRATOR
EXT TRIG IN
CAL
ETR
PCL
PRCAL
PROB CAL OUT
GND OUT
250ns
65.5 sec
TIMER
LeCroy 9400-1-S1 Sheet 9 of 18 ECO: 1016
LeCroy 9400-1-S1 Sheet 10 of 18 ECO: 1016



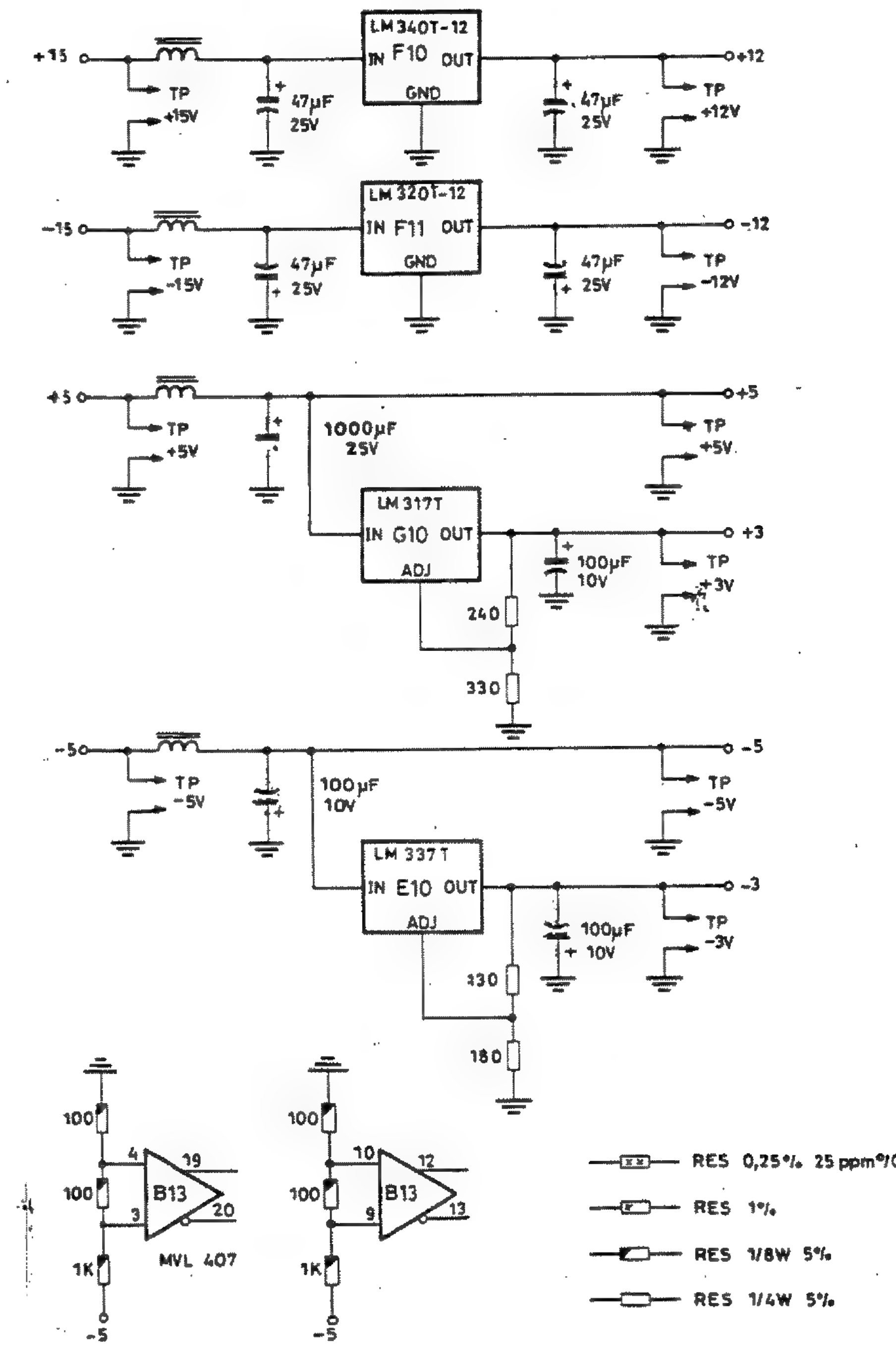
LeCroy 9400-1-S1 Sheet 11 of 18 ECO: 1016

LeCroy 9400-1-S1 Sheet 12 of 18 ECO: 1016


LTR
CAL
CH1
E12 LS164
E6 LS164
LF 353
HVV 200
C4
IN CH1
ADC1
TRIG HI
TRIG LO
PRCAL
CH 2
TCH1




LeCroy 9400-1-S1 Sheet 15 of 18 ECO: 1016



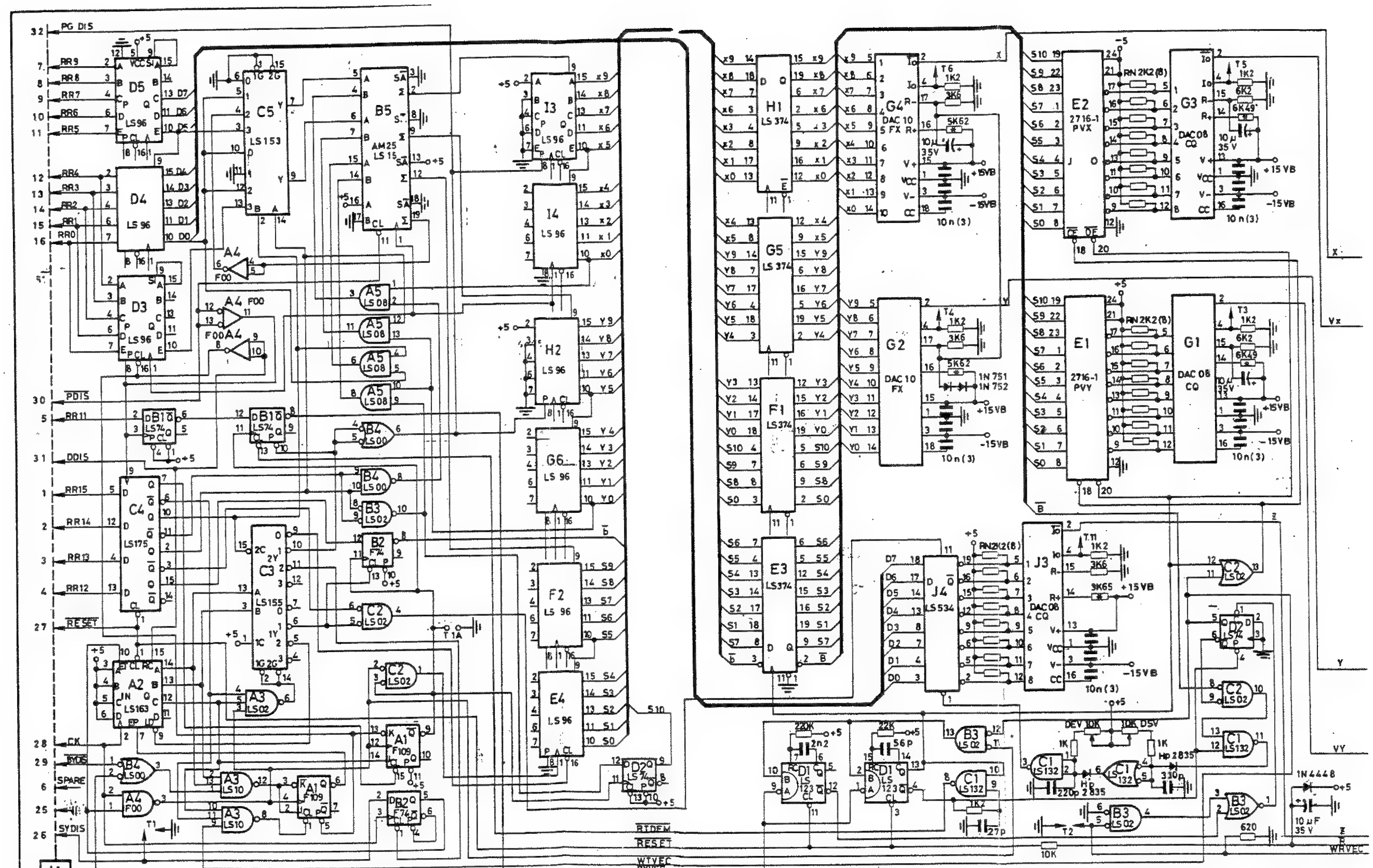
LeCroy 9400-1-S1 Sheet 16 of 18 ECO: 1015

LeCroy parts	IC	Designation	−5	+5	+12	GND	−12
200 012 001	MC 14 89 L	K7,K8		14		7	
200 012 002	MC 14 88 L	L7,L8			14	7	1
		E3,E4,E5,E13,E14					
200 031 028	74 LS 00 N	I13,K10,L12		14		7	
200 031 046	74 LS 04 N	F5,F13		14		7	
200 031 047	74 LS 10 N	K13		14		7	
200 031 048	74 LS 20 N	L11		14		7	
200 031 049	74 LS 74 N	H10,H16,L14,L15,L16		14		7	
200 031 051	74 LS 02 N	J13,J14		14		7	
200 031 055	74 LS 164 N	E6,E12,F4,F12		14		7	
200 031 066	74 LS 132 N	I15		14		7	
200 031 073	74 LS 32 N	F3,F14,G19,H11,L10,L13,L17		14		7	
200 031 074	74 LS 37 N	F17		14		7	
200 031 086	74 LS 08 N	F19,H13,I12,K14		14		7	
200 031 089	74 LS 125 N	G17,G20,H15,J15,K16		14		7	
200 031 097	74 LS 197 N	J20		14		7	
200 031 101	74 LS 393 N	H6,H7,K18,K19,K20		14		7	
200 031 106	74 LS 86 N	J12		14		7	
200 031 320	74 LS 320	K9		16		8	
200 041 017	74 LS 112 N	F20		16		8	
200 041 033	74 LS 174 N	C18		16		8	
200 041 039	74 LS 221 N	H18		16		8	
200 041 042	74 LS 191 N	G18,I14		16		8	
200 041 044	74 LS 123 N	F18,J19,K15		16		8	
200 041 056	74 LS 165 N	H9		16		8	
200 041 062	74 LS 138 N	I18		16		8	
200 041 067	74 LS 148 N	H20		16		8	
200 041 068	74 LS 158 N	I10,J10		16		8	
200 041 070	74 LS 257 AN	C21,F21,L18,L19,L20		16		8	
200 041 139	74 LS 139 N	H12,I19		16		8	
200 071 001	74 LS 240	B20,C20		20		10	
200 071 003	74 LS 374	H5,H8		20		10	
200 071 007	74 LS 244 N	I6,I7,J6,J7,J23,J27,L22		20		10	
200 071 245	74 LS 245 N	B21,E28,E29,F23,F26,J25,J28,L3		20		10	
200 071 299	74 LS 299 N	I8,I9,J9		20		10	
200 071 373	74 LS 373 N	I4,J4		20		10	
200 071 534	74 LS 534	J22,J26		20		10	
200 072 936	AM 29 66	K21,K22		20		10	
200 330 000	74 F 00	I11		14		7	
200 340 074	74 F 74	H14		14		7	
200 340 117	MC 10 H 117	A13	8			1,16	
200 340 138	74 F 138	I17		16		8	
200 340 379	74 F 379	K11		16		8	
200 341 175	74 F 175	K12		16		8	
200 440 191	74 F 191	B18,B19,C19		16		8	
200 540 384	74 LS 384	I3,J3		16		8	
200 570 684	74 LS 684	I5,J5		20		10	
205 240 264	RAM 41 64-15	K23,K24,K25,K26,K27,K28,K29,K30 L23,L24,L25,L26,L27,L28,L29,L30		8		16	
205 280 116	HM 611 GLP-2	B24				12	

LeCroy 9400-1-S1 Sheet 17 of 18 ECO: 1015

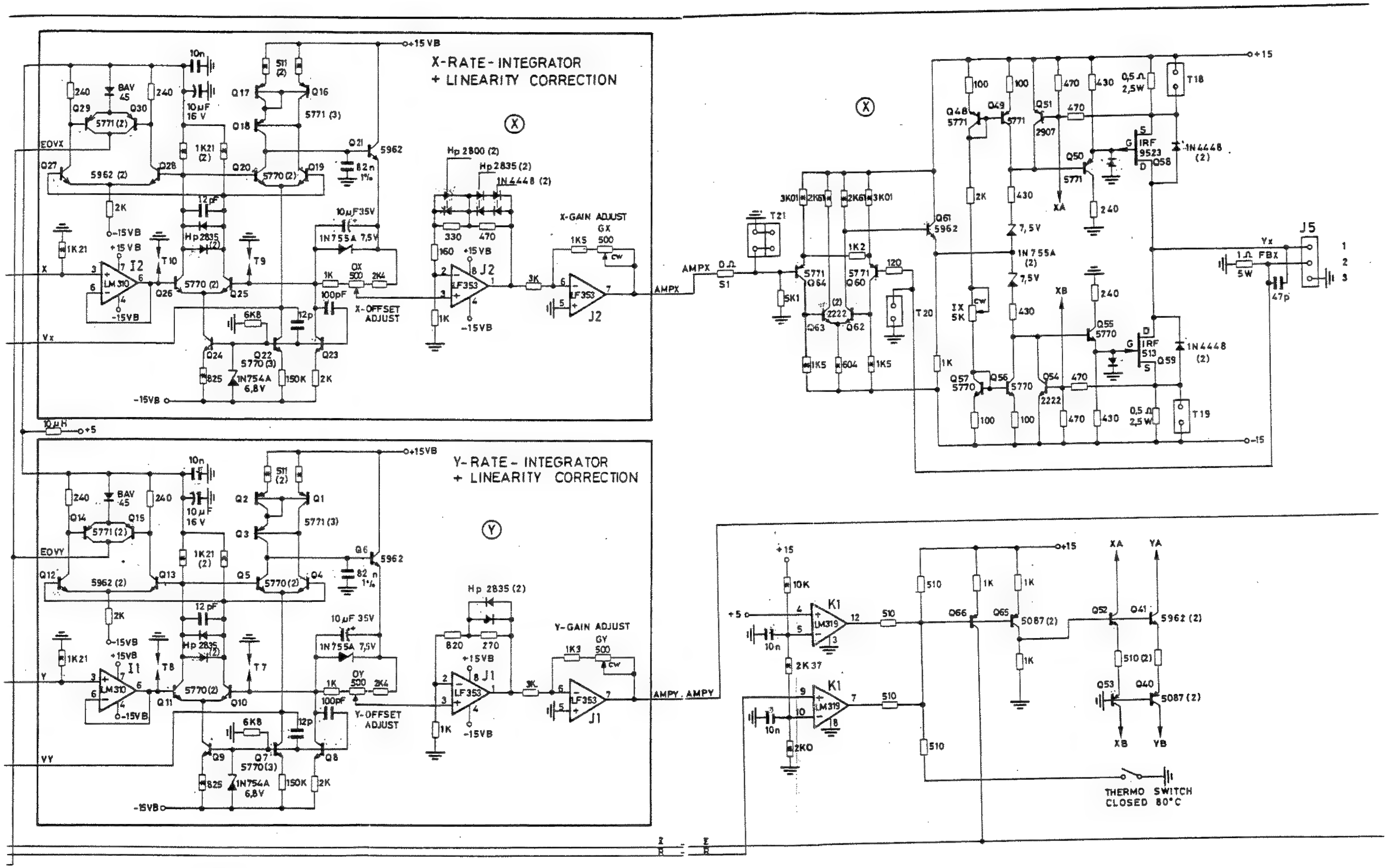
LeCroy parts	IC	Designation	+3	−3	−5	+5	+12	GND	+15	−15	−12
206 042 508	06 508 C J	H 3						14	13	3	
207 280 800	DAC 800	J 21				13		21	22	14	
207 340 399	74 LS 399 N	J 11				16		8			
208 011 008	LM 311 N	C 17						1	8	4	
208 031 010	LM 339 N	J 17 F 17			 12	3 3	12 				
208 033 001	CA 30 46	E 1				8–11		12	5		
208 041 001	DAC-08 EQ	B 17						1	13	3	
208 110 353	LF 353 N	C 13							8	4	
208 122 337	LM 337 N	E 10									
208 123 002	LM 340 T-12	F 10									
208 130 324	LM 324	G 6					4				11
208 130 347	LF 347	G 4, G 5					4				11
208 570 317	LM 317	G 10									
208 124 003	LM 320T-12	F 11									
208 740 321	74 LS 321	K 17				16		8			
225 070 407	MUL 407	B 13			11	2		1,16			
227 391 068	68 000 L 8	N 29						16,53			
227 762 661	2661	L 4, L 6				26		4,16			
210 440 200	HVV 200	A 4, C 4	27 34	11 18	10 19	28 35	29 36	5,14,21 23,30,39			9,15
220 010 101	HAB 101	A 3					4	3,8			1

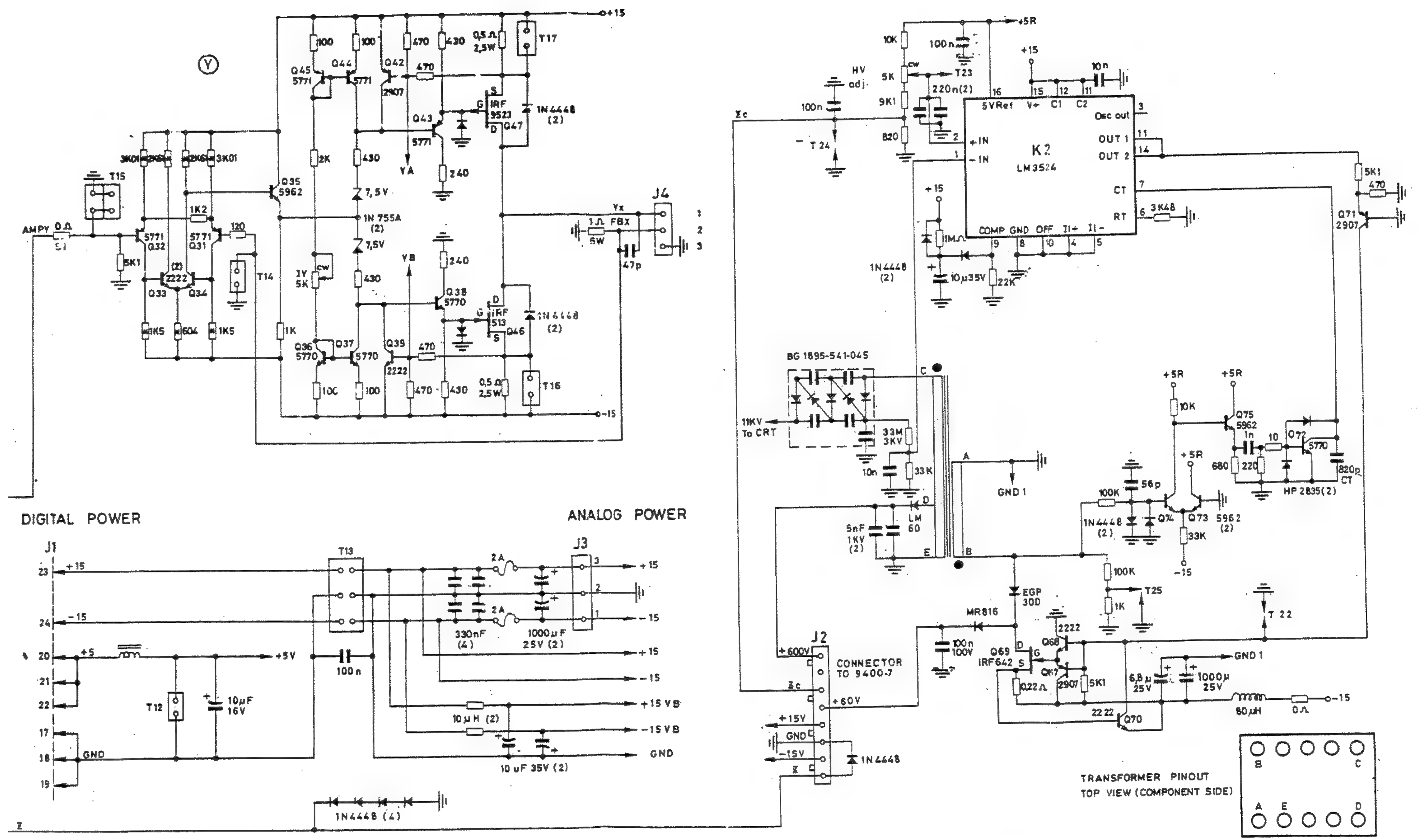
LeCroy RESEARCH SYSTEMS	
DRAWN BY/DATE P_PERRIN 19.12.85	MODEL 9400-1 MOTHER CARD SCHEMA
CHKD BY/DATE B_M J-F-G	
APPROVED BY/DATE 05-02-87	DWG NO: 9400-1-S1
SCALE 1/1	SH 18 OF 18 ECO NO. 1015



LeCroy 9400-2-S1 Sheet 1 of 7 Eco:1014

LeCroy 9400-2-S1 Sheet 2 of 7 Eco:1014

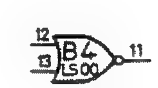

X-RATE - INTEGRATOR
+ LINEARITY CORRECTION
X-GAIN ADJUST
X-OFFSET ADJUST
Y-RATE - INTEGRATOR
+ LINEARITY CORRECTION
Y-GAIN ADJUST
Y-OFFSET ADJUST
AMPX
AMPY
J5
THERMO SWITCH
CLOSED 80°C



LeCroy 9400-2-S1 Sheet 5 of 7 Eco 1014

LeCroy 9400-2-S1 Sheet 6 of 7 Eco 1014

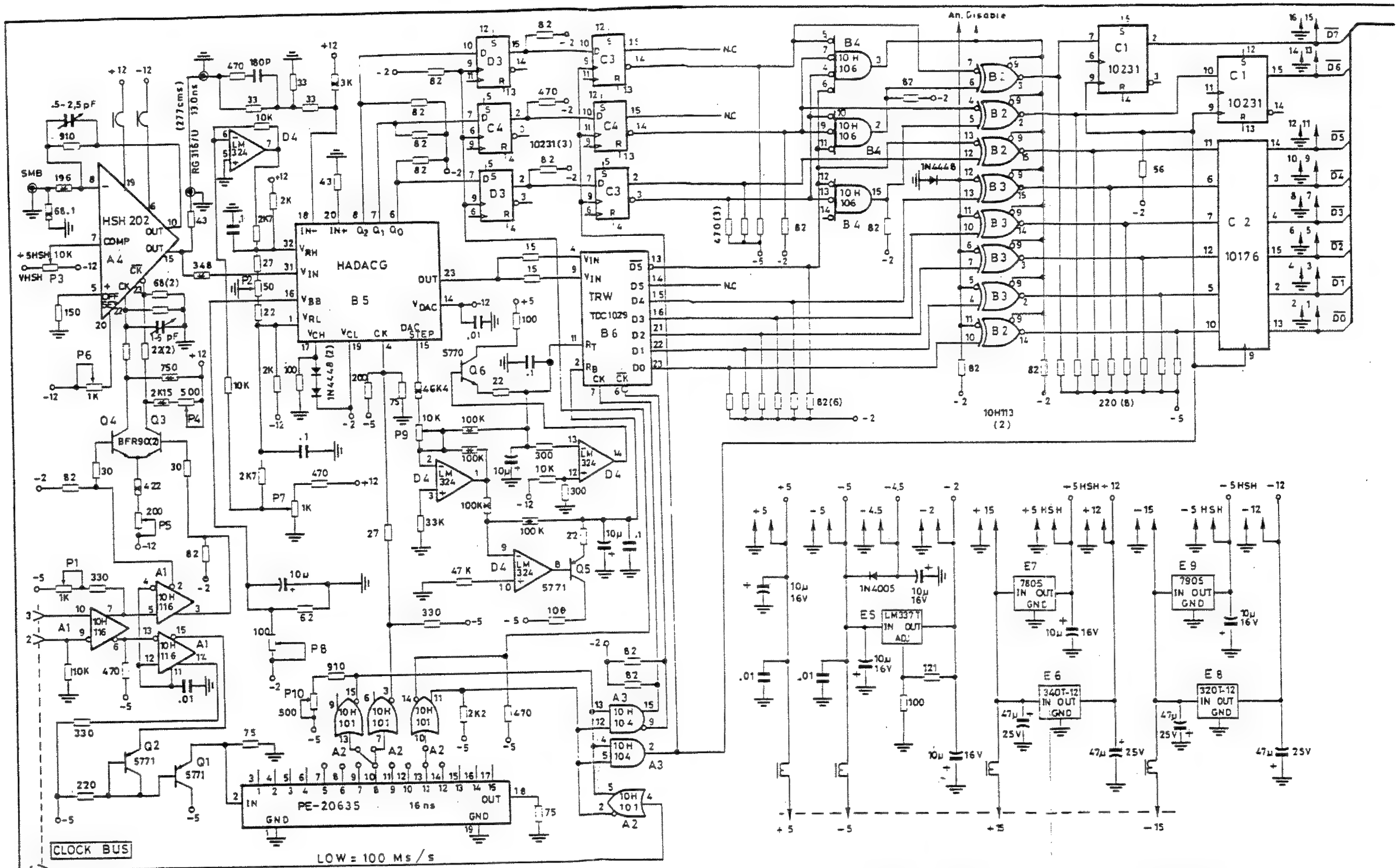
LeCroy parts :	IC :	Désignation :	+5	0V	+15	-15
200 031 028	SN 74 LS 00N	B4	14	7		
200 031 047	SN 74 LS 10N	A3	14	7		
200 031 049	SN 74 LS 74N	B1, D2	14	7		
200 031 051	SN 74 LS 02N	B3, C2	14	7		
200 031 066	SN 74 LS 132N	C1	14	7		
200 031 086	SN 74 LS 08N	A5	14	7		
200 041 044	SN 74 LS 123N	D1	16	8		
200 041 049	SN 74 LS 175N	C4	16	8		
200 041 054	SN 74 LS 153N	C5	16	8		
200 041 155	SN 74 LS 155N	C3	16	8		
200 071 003	SN 74 LS 374	E3, F1, G5, H1	20	10		
200 071 534	74 LS 534	J4	20	10		
200 330 000	74 F 00	A4	14	7		
200 340 074	74 F 74	B2	14	7		
200 340 109	74 F 109	A1	16	8		
200 442 163	74 LS 163	A2	16	8		
200 570 015	AM 25 LS 15	B5	20	10		
205 381 716	2716 - 1	E1, E2	24	12		
205 640 096	74 LS 96	D3, D4, D5, E4, F2, G6, H2, I3, I4,	5	12		
207 262 010	DAC - 10	G2, G4,		1	15	3
208 011 005	LM 310 N	I1, I2,			7	4
208 041 001	DAC - 08	G1, G3, J3		1	13	3
208 041 524	3524	K2		8	12,13 15	
208 110 353	LF 353 N	J1, J2			8	4
208 031 009	LM 319 N	K1		3,6,8	11	



SPARE

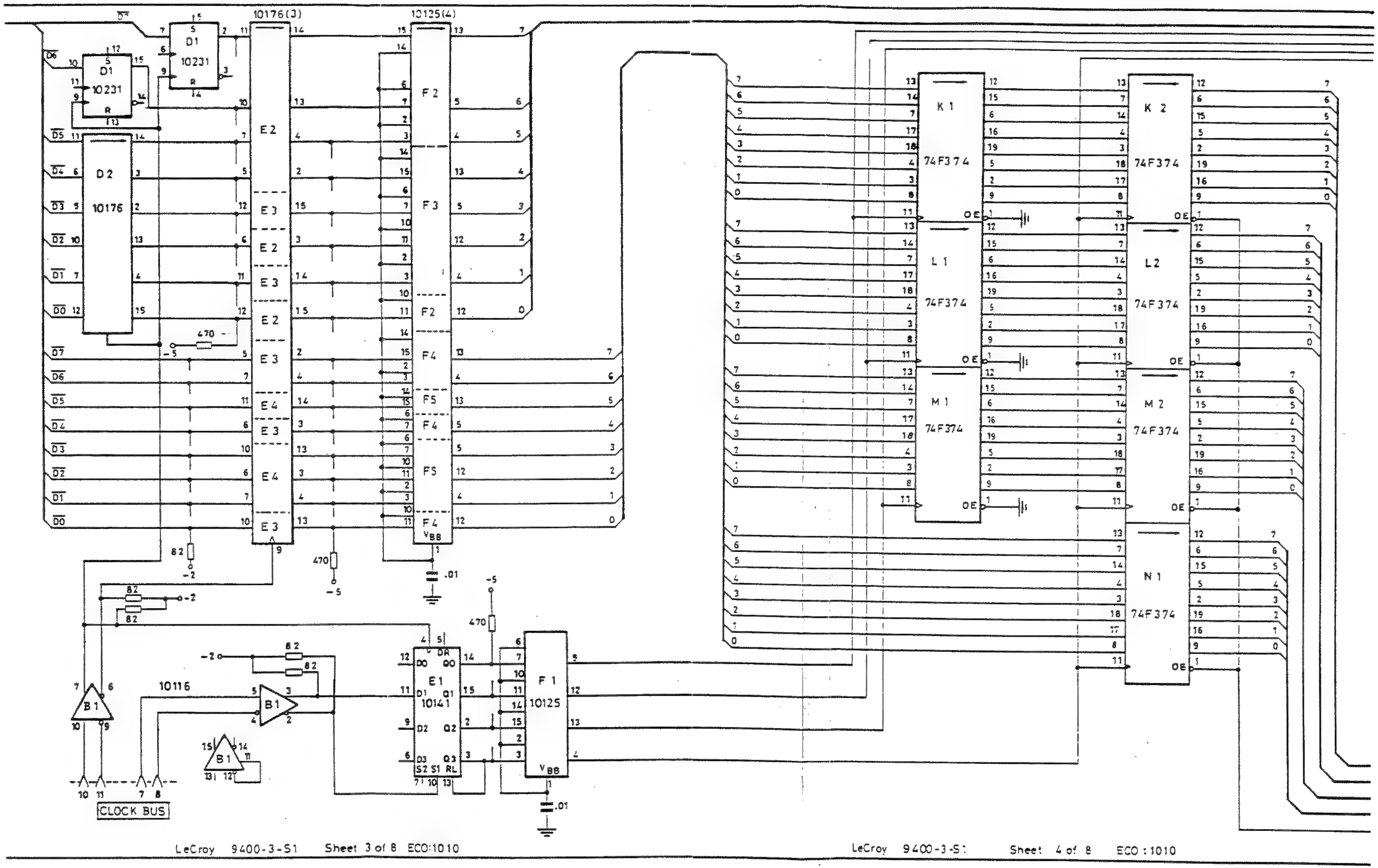
LeCroy RESEARCH SYSTEMS

DRAWN [illegible]	MODEL 9400-2
CHECKED D.AEBISCH	DISPLAY CARD
DATE 25-06-85	SCHEMA
DRAWING NUMBER: 9400-2-S1	SHEET 7 OF 7 — ECO 1014 DATE 15-7-87

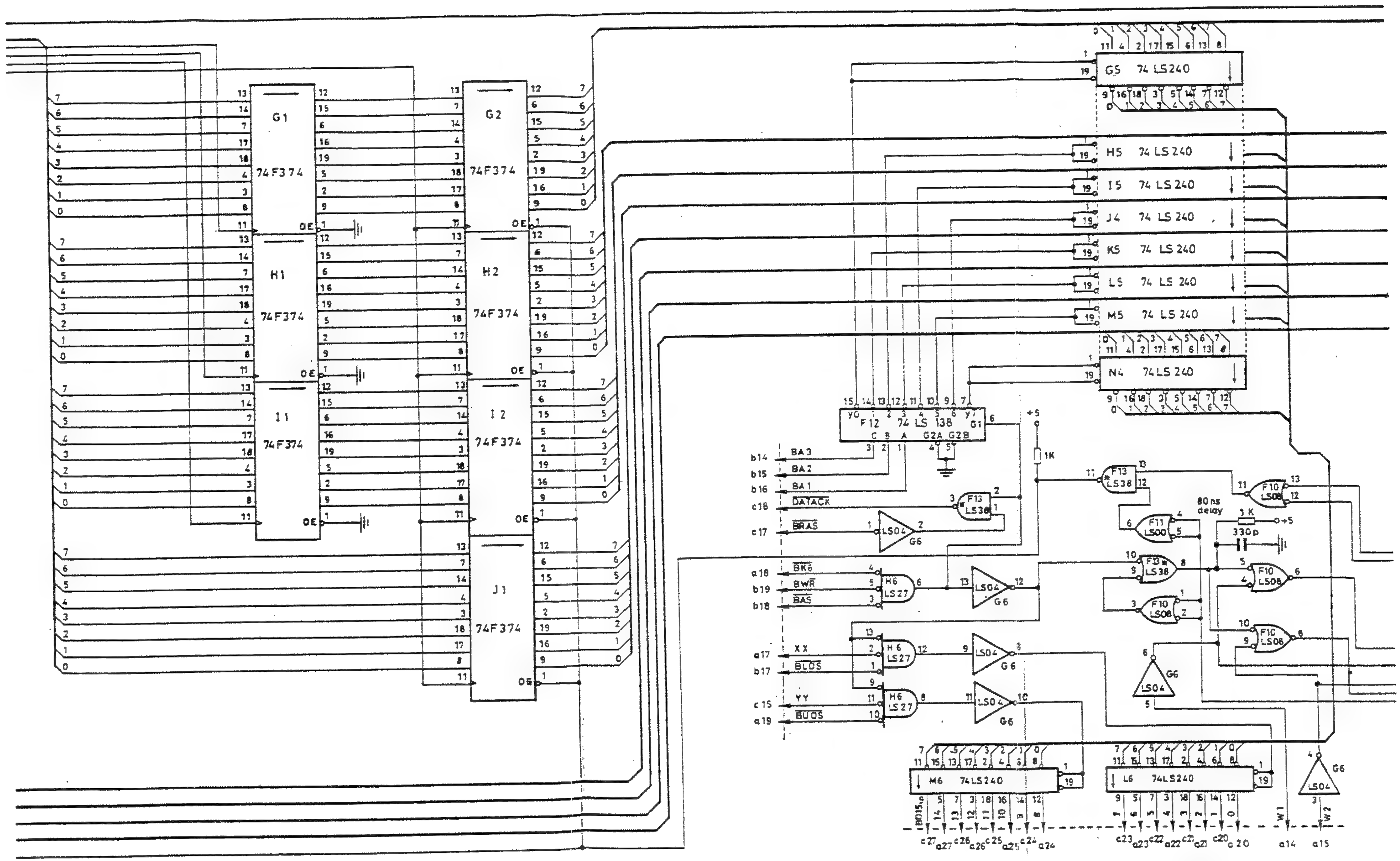


LeCroy 9400-3-S1 Sheet 1 of 8 ECO: 1010

LeCroy 9400-3-S1 Sheet 2 of 8 ECO: 1010

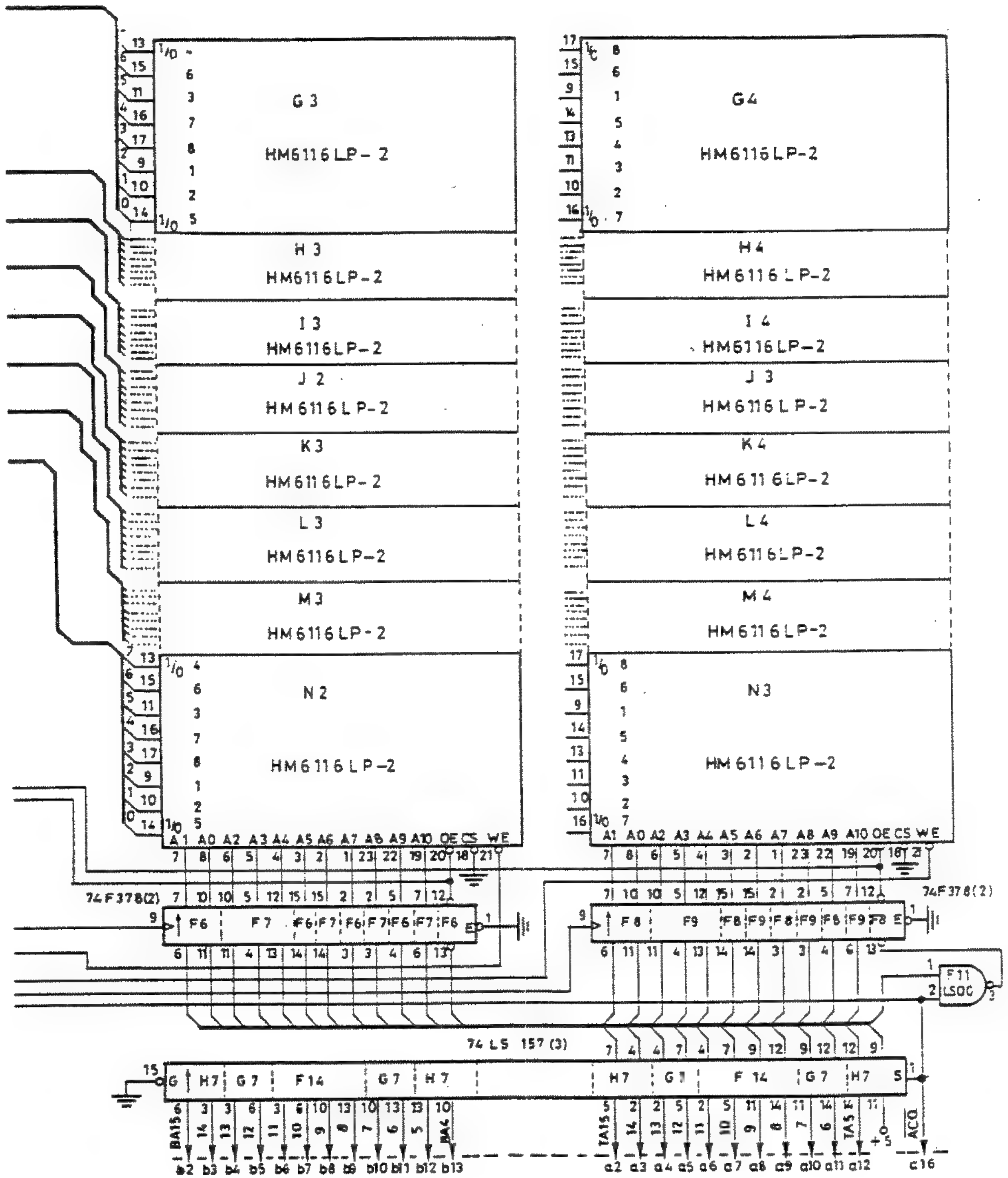


10176(3)
10125(4)
D1
10231
D2
10176
E2
E3
E4
F2
F3
F4
F5
K1
K2
L1
L2
M1
M2
N1
74F374
E1
10141
F1
10125
B1
10116
CLOCK BUS
LeCroy 9400-3-S1 Sheet 3 of 8 ECO:1010
LeCroy 9400-3-S1 Sheet 4 of 8 ECO:1010



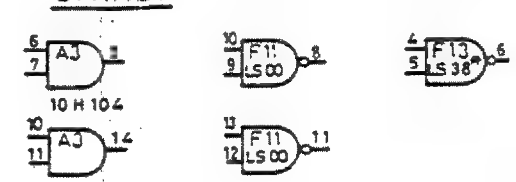
LeCroy 9400-3-S1 Sheet 5 of 8 ECO:1010

LeCroy 9400-3-S1 Sheet 6 of 8 ECO:1010



Le Croy Parts N°	IC	DESIGNATION	-12V	-5V HSH	-5V	-4.5V	GND	+5V	+5V HSH	+12V
200 031 028	SN 74 LS 00N	F11					7	14		
200 031 046	SN 74 LS 04N	G6					7	14		
200 031 057	SN 74 LS 27N	H6					7	14		
200 031 086	SN 74 LS 08N	F10					7	14		
200 032 010	74 LS 38 PC	F13					7	14		
200 041 027	SN 74 LS 157N	F14, G7, H7					8	16		
200 041 062	SN 74 LS 138N	F12					8	16		
200 071 001	SN 74 LS 240	G5, H5, I5, J4, K5, L5, L6 M5, M6, N4					10	20		
200 340 113	MC 10 H 113	B2, B3			8		1.16			
200 340 378	74 F 378	F6, F7, F8, F9,					8	16		
200 341 106	10 H 106	B4			8		1.16			
200 344 101	10 H 101 P	A2			8		1.16			
200 344 104	10 H 104	A3			8		1.16			
200 371 374	74 F 374 PC	G1, G2, H1, H2, I1, I2, J1 K1, K2, L1, L2, M1, M2, N2					10	20		
204 022 002	MC 10176 L	C2, E2, E3, E4, D2,			8		1.16			
204 042 008	MC 10125 P	F1, F2, F3, F4, F5,			8		16	9		
204 042 011	MC 10116 P	B1			8		1.16			
200 042 141	MC 10141	E1			8		1.16			
204 043 231	MC 10231 P	C3, C4, D1, D3, C1			8		1.16			
205 280 116	HM 6116 LP-2	G3, G4, H3, H4, I3, I4, J2 J3, K3, K4, L3, L4, M3, M4, N2, N3					12	24		
207 444 116	10 H 116	A1			8		1.16			
207 281 029	TDC 1029	B6			1,12 18,19 24		3,5,8 10,17 20			
208 130 324	LM 324	D4	11							4
210 060 032	HADAG G	B5	21		29	5	3,9,10 12,13 24,26 28,30	2		22
210 080 202	HSH 202	A4		9			2,11 14,17 24		4	

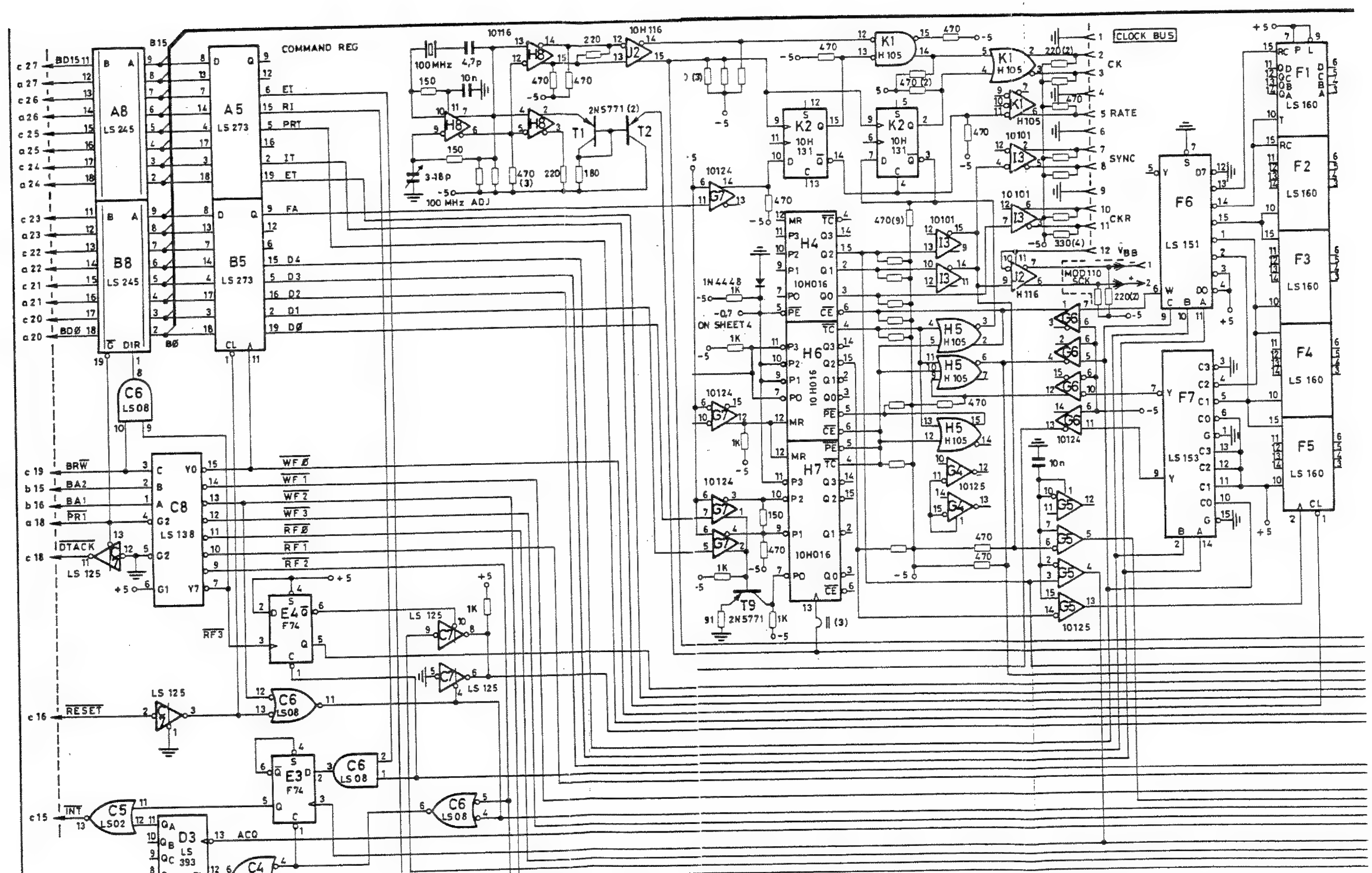
SPARES



RES 1%

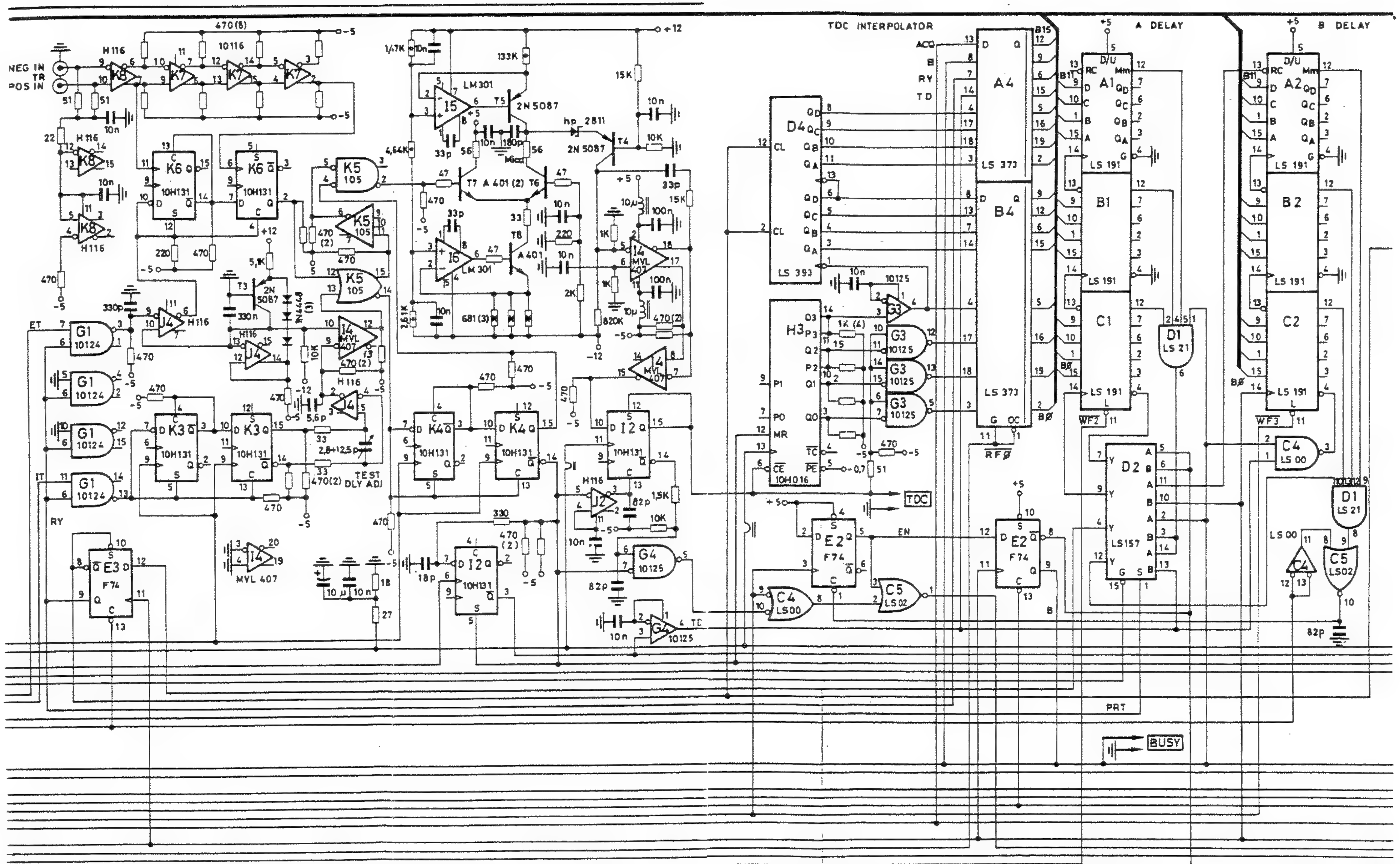
LeCroy RESEARCH SYSTEMS

DRAWN BY/DATE	MODEL 9400-3 ADC SCHEMATIC
CHKD BY/DATE JF-GOUMAZ	
APPROVED BY/DATE 19-12-86	DWG NO- 9400-3-S1 — SIZE
SCALE —	SH. 8 OF 8 ECO NO. 1010 ENG REV APP



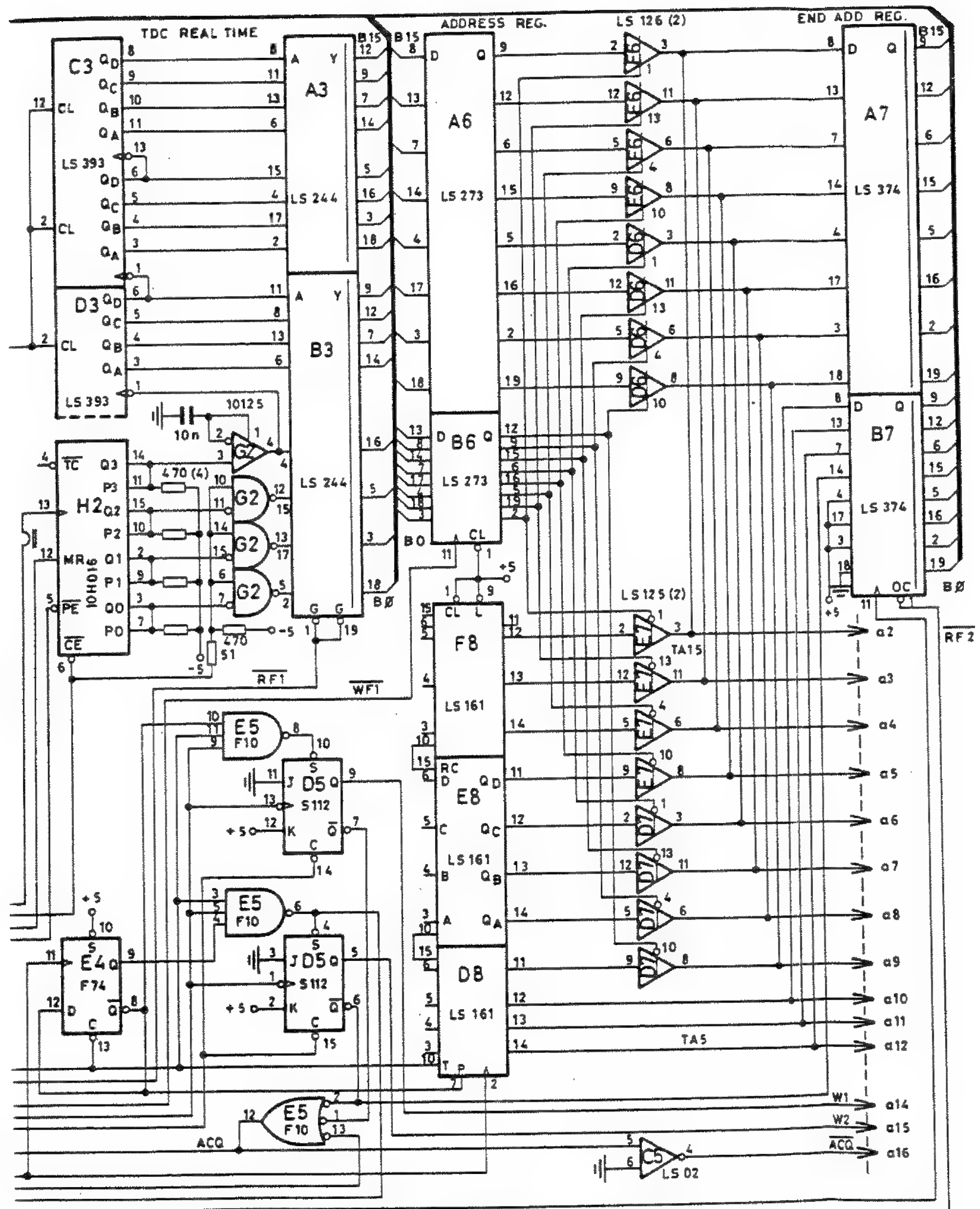
Le Croy 9400-4-S1 Sheet 1 of 7 Eco : 1011

Le Croy 9400-4 -S1 Sheet 2 of 7 Eco : 1011

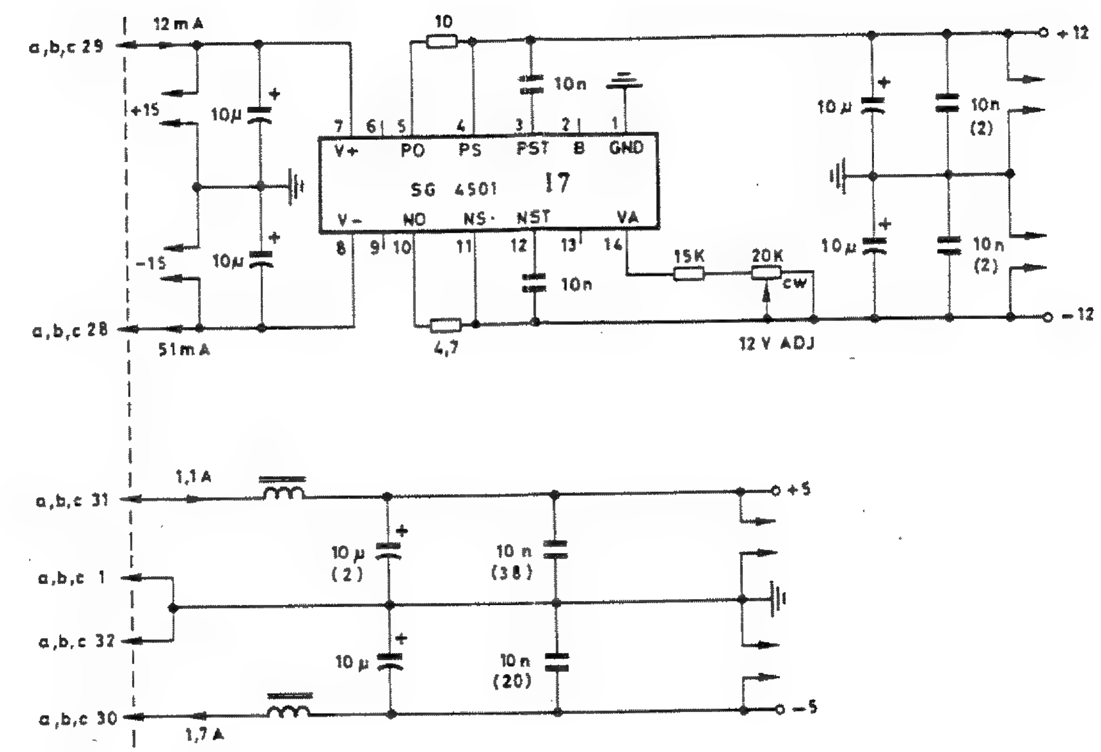


Le Croy 9400-4 - S1 Sheet 3 of 7 Eco: 1011

Le Croy | 9400-4-S1 Sheet 4 of 7 Eco : 1011



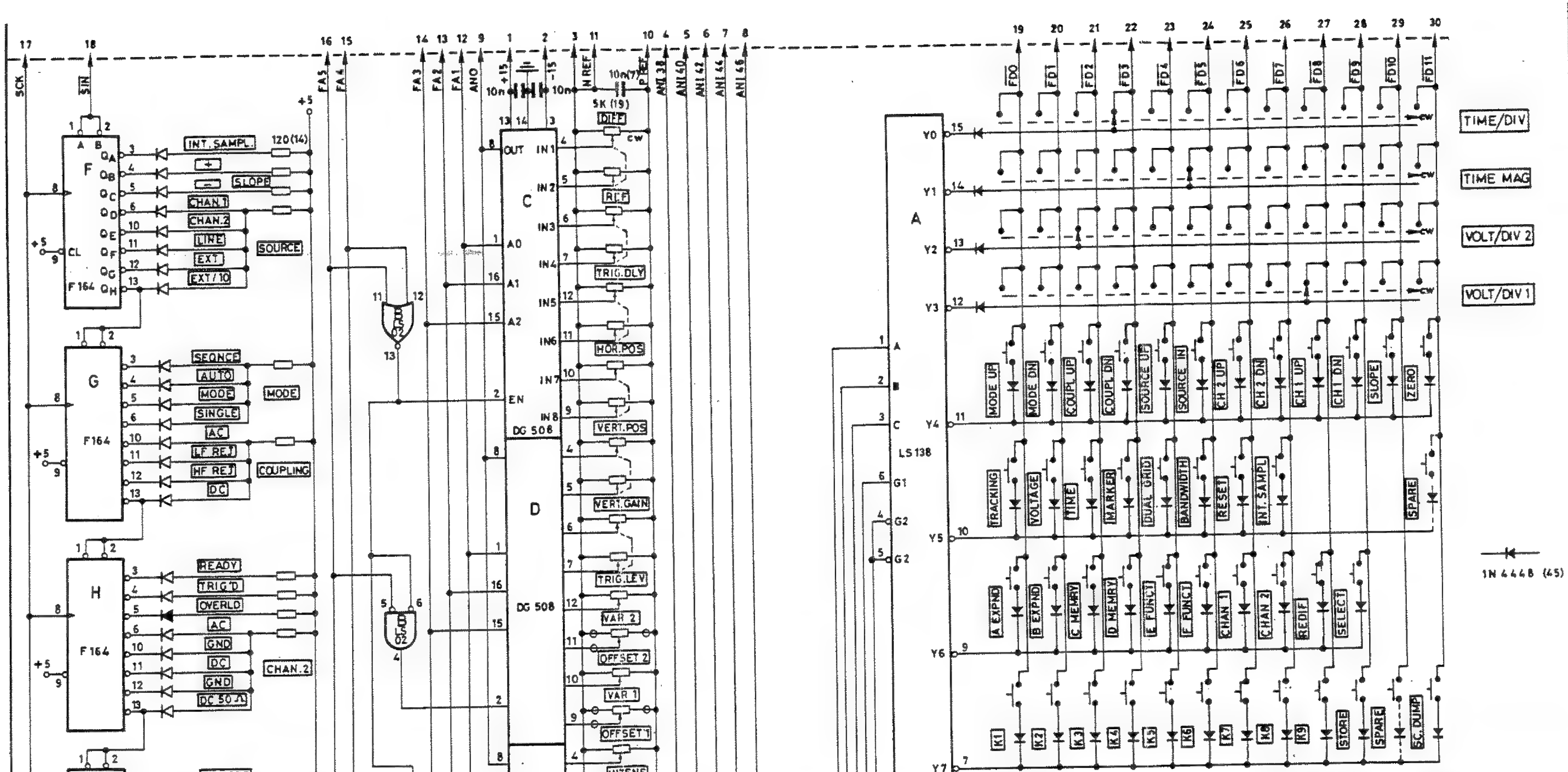
LeCroy 9400-4-S1 Sheet 5 of 7 Eco : 1011



LeCroy 9400-4-S1 Sheet 6 of 7 Eco : 1011

Le Croy part	IC	Designation	-15	-12	-5	GND	+5	+12	+15
200 031 028	74LS00	C4				7	14		
200 031 051	74LS02	C5				7	14		
200 031 086	74LS 08	C6				7	14		
200 330 010	74F 10 PC	E5				7	14		
200 031 072	74LS21	D1				7	14		
200 340 074	74F 74 PC	E2,E3,E4				7	14		
200 041 008	74S 112	D5				8	16		
200 031 089	74LS125	C7,D7,E7				7	14		
200 330 126	74LS126	D6,E6				7	14		
200 041 062	74LS138	C8				8	16		
200 081 007	74LS151	F6				8	16		
200 041 054	74LS153	F7				8	16		
200 041 027	74LS157	D2				8	16		
200 041 073	74LS160	F1,F2,F3,F4,F5				8	16		
200 041 026	74LS161	D8,E8,F8				8	16		
200 041 042	74LS191	A1,A2,B1,B2,C1, C2				8	16		
200 071 007	74LS244	A3,B3				10	20		
200 071 245	74LS245	A8,B8				10	20		
200 071 005	74LS273	A5,A6,B5,B6				10	20		
200 071 373	74LS373	A4,B4				10	20		
200 071 003	74LS374	A7,B7				10	20		
200 031 101	74LS393	C3,D3,D4				7	14		
200 444 016	10H016	H2,H3,H4,H7,H6			8	1,16			
204 042 016	F10101P	I3			8	1,16			
204 042 004	MC10105P	K5			8	1,16			
200 344 105	MC10H105P	H5,K1			8	1,16			
207 444 116	MC10H116P	J2,J4,K8			8	1,16			
204 042 011	MC10116P	H8,K7			8	1,16			
204 042 007	MC10124P	G1,G6,G7			8	16	9		
204 042 008	MC10125P	G2,G3,G4,G5			8	16	9		
200 344 131	MC10H131P	I2,K2,K3,K4,K6			8	1,16			
225 070 407	MVL407	I4			11	1,16	2		
208 011 003	LM301AN	I5				4		7	
208 011 003	LM301AN	I6		4		7			
208 021 501	SG4501J	I7	8	11		1		4	7

LeCroy RESEARCH SYSTEMS			
DRAWN M.A. Bénédic	MODEL 9400-4		
CHECKED J.P. VITTET	TIME BASE		
DATE 4-2-85	SCHEMATIC		
DRAWING NUMBER: 9400-4-S1	SHEET 7 OF 7	ECO 1011	DATE 19-04-88



LeCroy part n°	IC	Désignation	+15	+5	GND	-15
200 031 051	74LS02	B		14	7	
200 041 062	74LS138	A		16	8	
205 630 164	74F164	F,G,H,I		14	7	
207 340 508	DG 508 ACJ	C,D,E	13		14	3

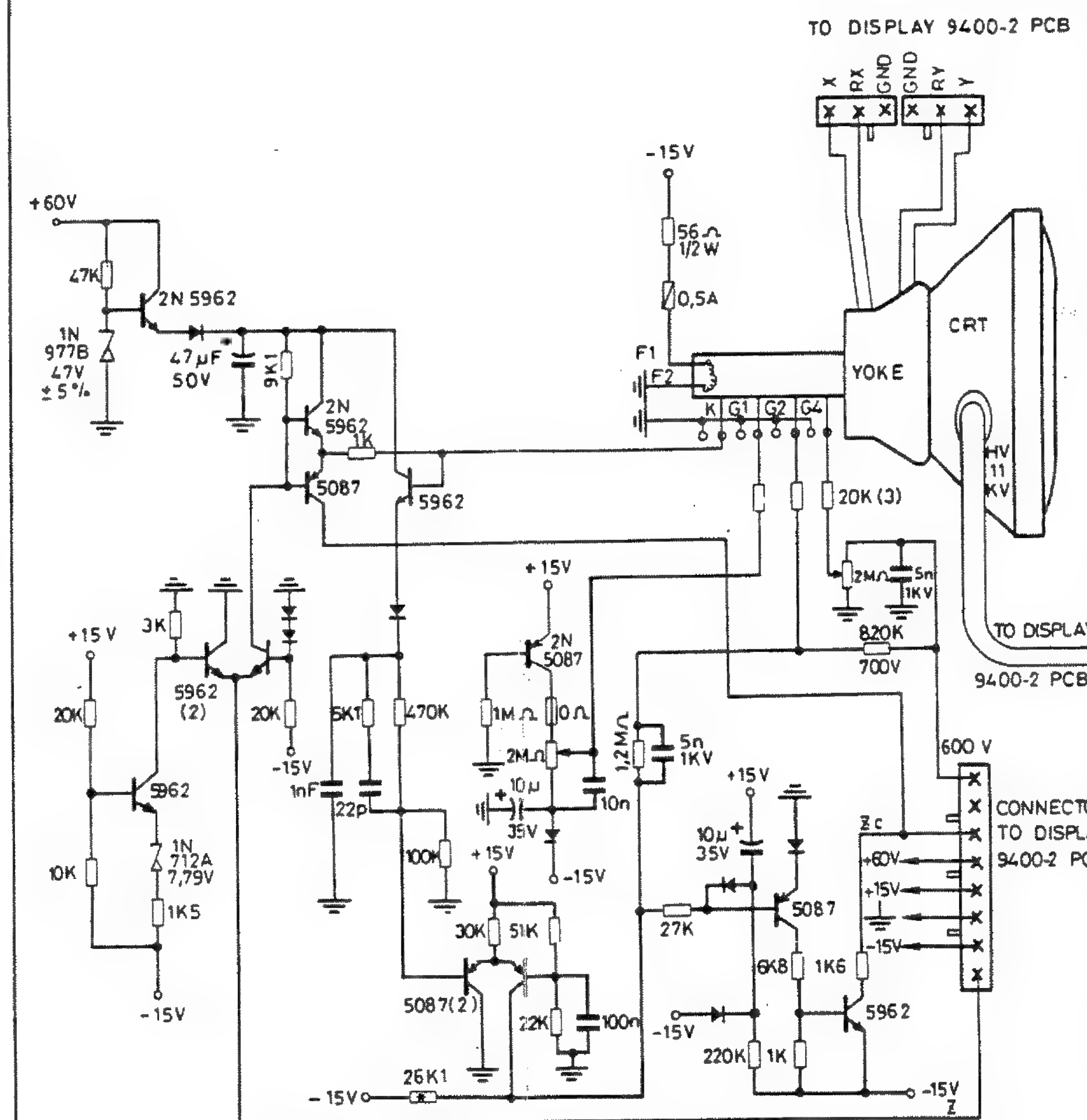
LeCroy RESEARCH SYSTEMS

DRAWN
CHECKED J.P. VITTET
DATE 14-2-85

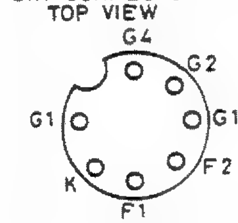
MODEL 9400-5
FRONT PANEL
SCHEMATIC

DRAWING NUMBER: 9400-5-S1 SHEET 2 OF 2 ECO NO 1001 DATE 24-9-85

LeCroy 9400-5-S1 Sheet 1 of 2 Eco: 1001

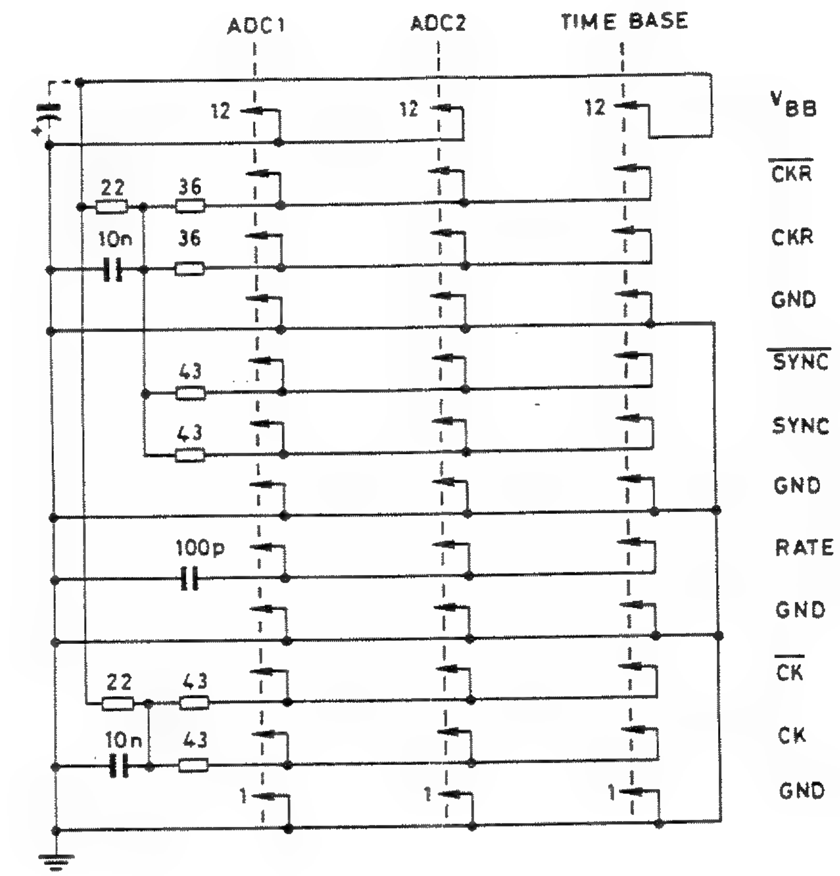


CRT CONNECTOR TOP VIEW

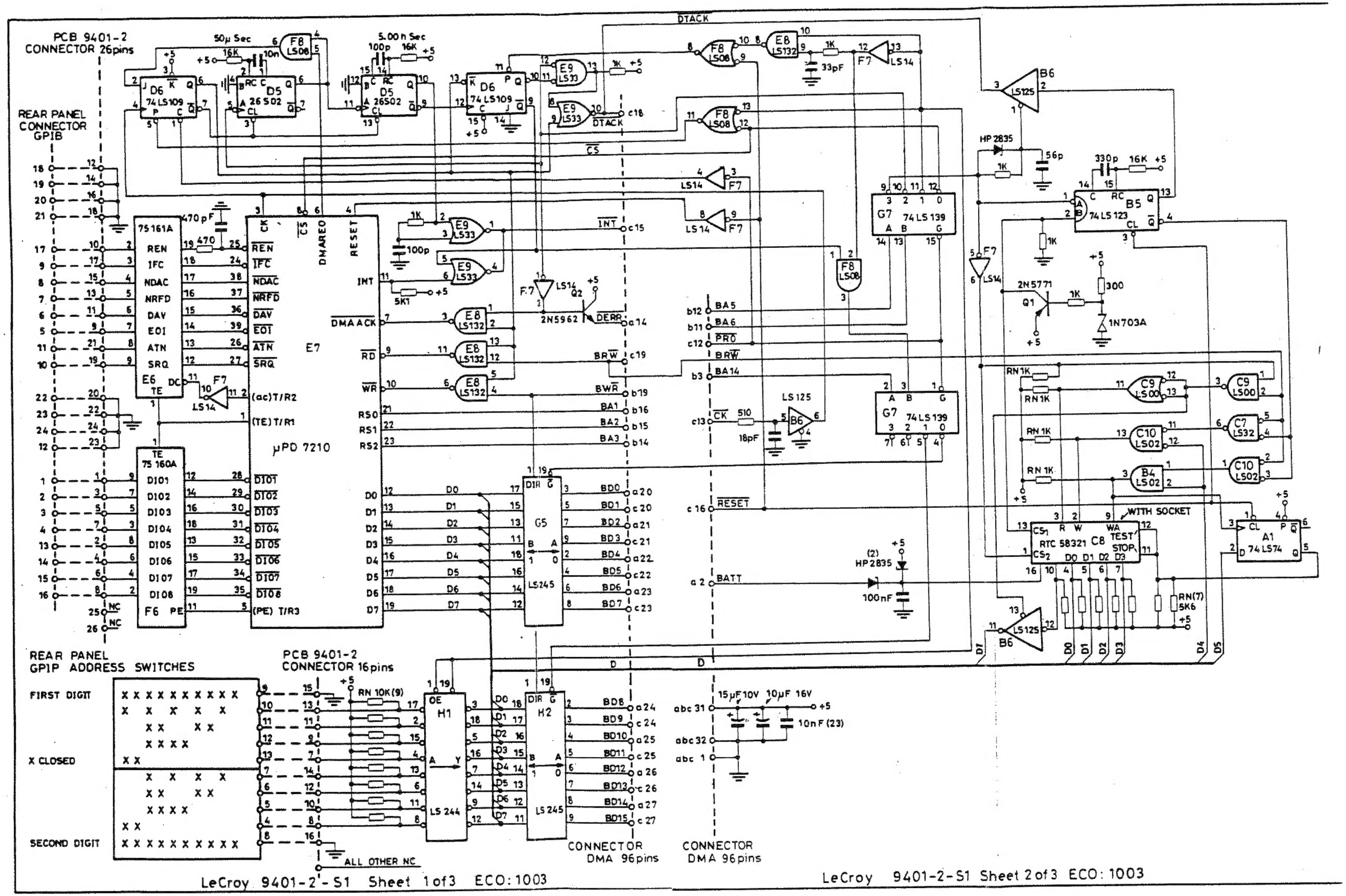


1N 4448

LeCroy RESEARCH SYSTEMS			
DRAWN BY/DATE	MODEL 9400-7		
CHKD BY/DATE D-AEBISCHER	TV FOCUS SCHEMATIC		
APPROVED BY/DATE 28-10-85	DWG NO. 9400-7-S1		SIZE
SCALE -	ECO DATE 31-3-87	SH. 1 OF 1	ECO NO. 1004



LeCroy RESEARCH SYSTEMS			
DRAWN M.A. Viaudic	MODEL 9400-8		
CHECKED J.P. VITTET	CLOCK BUS SCHEMATIC		
DATE 7-2-85			
DRAWING NUMBER: 9400-8-S1	SHEET 1 OF 1	ECO NO 1000	DATE 7-2-85



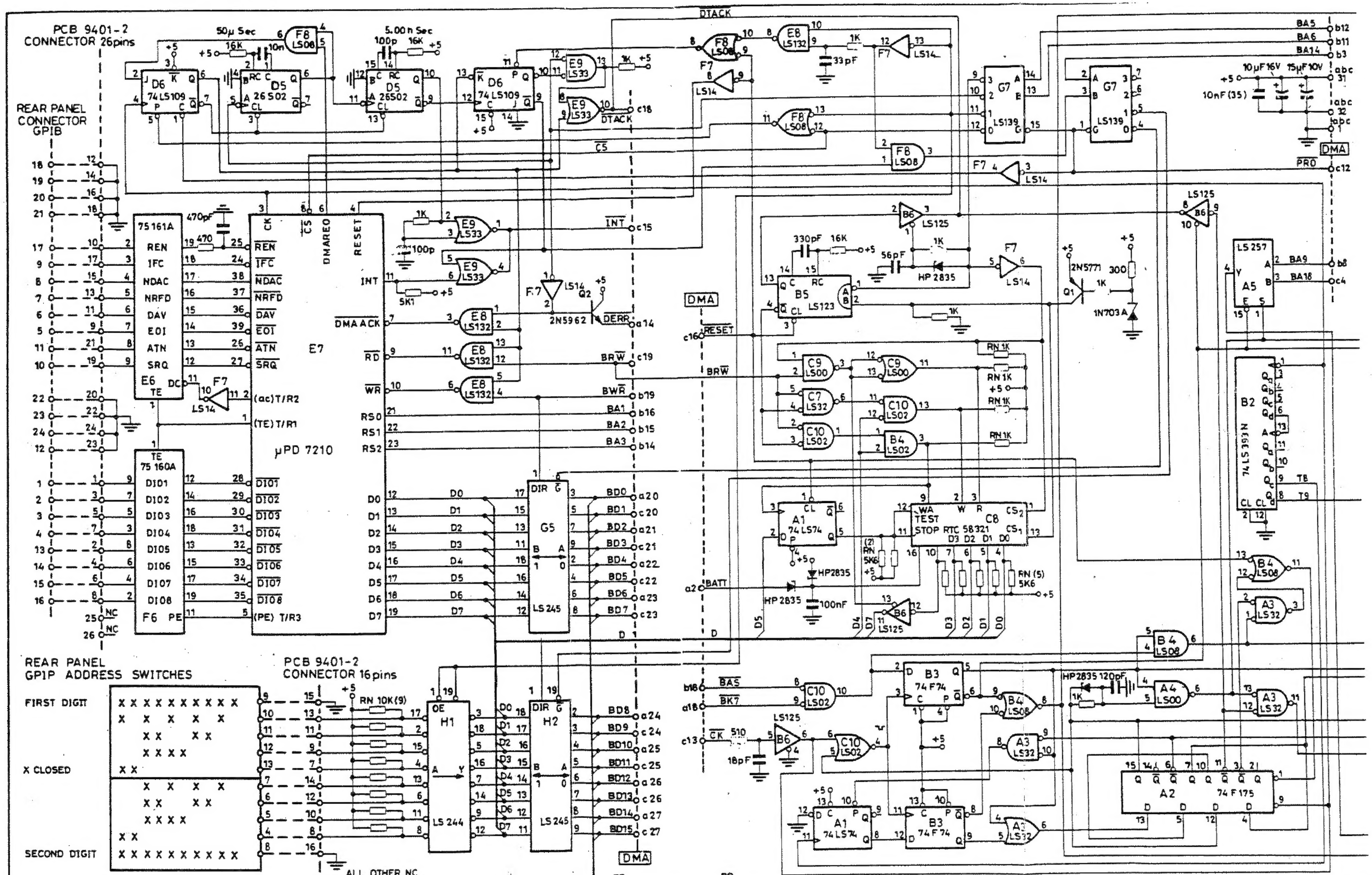
LeCroy 9401-2-S1 Sheet 1of3 ECO:1003

LeCroy 9401-2-S1 Sheet 2of3 ECO:1003

LeCroy parts	IC	Désignation	+5V	0V
200 031 028	SN 74 LS 00 N	C9,	14	7
200 031 049	SN 74 LS 00 N	A1,	14	7
200 031 051	SN 74 LS 02 N	C10,	14	7
200 031 066	SN 74 LS 132 N	E8,	14	7
200 031 073	SN 74 LS 32 N	C7,	14	7
200 031 086	SN 74 LS 08 N	B4,F8,	14	7
200 031 089	SN 74 LS 125 N	B6	14	7
200 031 095	SN 74 LS 14 N	F7,	14	7
200 041 044	SN 74 LS 123 N	B5,	16	8
200 041 066	SN 74 LS 109 N	D6,	16	8
200 041 139	SN 74 LS 139 N	G7,	16	8
200 071 007	SN 74 LS 244 N	H1,	20	10
200 071 245	SN 74 LS 245 N	G5,H2	20	10
200 330 033	SN 74 LS 33 N	E9	14	7
200 441 002	AM 26 S 02 PC	D5,	16	8
200 640 321	RTC 58 321	C8,		8
207 197 210	UPD 72 10	E7,	40	20
207 470 160	SN 75 160 A	F6,	20	10
207 470 161	SN 75 161 AN	E6,	20	10

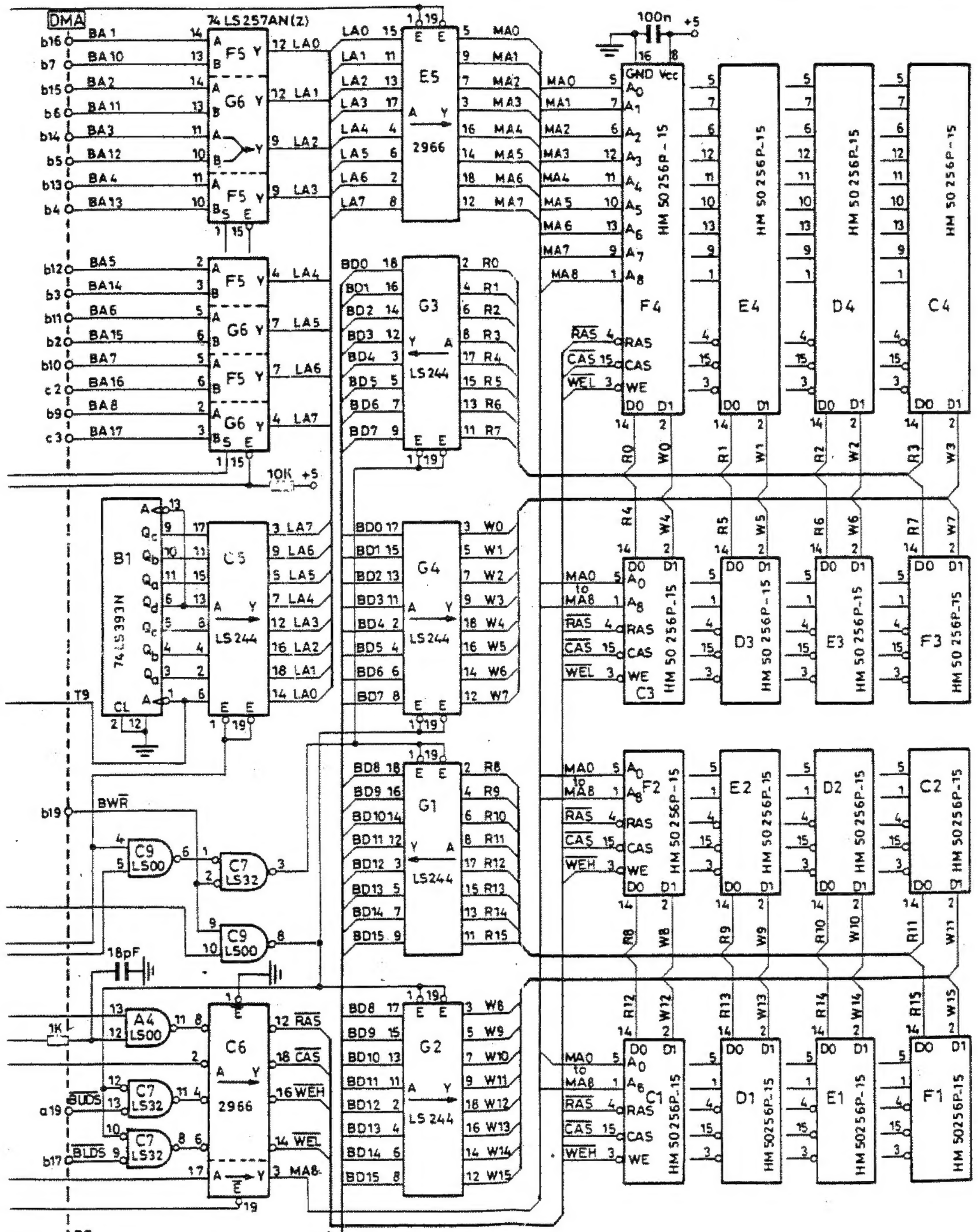
LeCroy RESEARCH SYSTEMS

DRAWN BY/DATE P_PERRIN 21.11.85	MODEL 9401-2 GPIB SCHEMA
CHKD BY/DATE 03.11.86 B-MAURON	
APPROVED BY/DATE 14-07-86	DWG NO. 9401-2-S1 SIZE
SCALE 1:1	SH. 3 OF 3 ECO NO. 1003 ENG. REV APP



LeCroy 9401-2/1-S1 and 9401-2/2-S1 Sheet 1 of 4 ECO: 1004

LeCroy 9401-2/1-S1 and 9401-2/2-S1 Sheet 2 of 4 ECO: 1004



LeCroy 9401-2/1-S1 and 9401-2/2-S1 Sheet 3 of 4 ECO:1004

LeCroy parts	IC	Désignation	+5V	0V
200 031 028	SN 74 LS 00 N	A4,C9	14	7
200 031 049	SN 74 LS 74 N	A1,	14	7
200 031 051	SN 74 LS 02 N	C10,	14	7
200 031 066	SN 74 LS 132 N	E8,	14	7
200 031 073	SN 74 LS 32 N	A3,C7,	14	7
200 031 086	SN 74 LS 08 N	B4,F8,	14	7
200 031 089	SN 74 LS 125 N	B6,	14	7
200 031 095	SN 74 LS 14 N	F7,	14	7
200 031 101	SN 74 LS 393 N	B1,B2,	14	7
200 041 044	SN 74 LS 123 N	B5,	16	8
200 041 066	SN 74 LS 109 N	D6	16	8
200 041 070	SN 74 LS 257 AN	A5,F5,G6,	16	8
200 041 139	SN 74 LS 139 N	G7,	16	8
200 071 007	SN 74 LS 244 N	C5,G1,G2,G3,G4,H1,	20	10
200 071 245	SN 74 LS 245 N	G5,H2,	20	10
200 072 966	AM 2966 PC	C6,E5,	20	10
200 330 033	SN 74 LS 33 N	E9,	14	7
200 340 074	SN 74 F 74	B3,	14	7
200 341 175	SN 74 F 175 P	A2,	16	8
200 441 002	AM 26 S 02 PC	D5,	16	8
200 640 321	RTC 58 321	C8,		8
205 240 256	HM 50 256 P-15	C1,C2,C3,C4,D1,D2,D3,D4,E1, E2,E3,E4,F1,F2,F3,F4,	8	16
207 197 210	UPD 7210	E7,	40	20
207 470 160	SN 75 160 A	F6,	20	10
207 470 161	SN 75 161 AN	E6,	20	10

LeCroy RESEARCH SYSTEMS

DRAWN BY/DATE P_PERRIN 18.12.85	MODEL 9401-2/1
CHKD BY/DATE 3.11.86 B-MAURON	MODEL 9401-2/2
	GPIB+MEMORY SCHEMA
APPROVED BY/DATE 14-07-86	DWG NO: 9401-2/1-S1 9401-2/2-S1
SCALE 1:1	SH. 4 OF 4 ECO NO. 1004